(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 565 125 A1**

(12) EUROPEAN PATENT APPLICATION

(21) Application number: **93105927.3**

(51) Int. Cl.5: **G02F 1/136**

(22) Date of filing: **13.04.93**

(30) Priority: **10.04.92 JP 90506/92**

(43) Date of publication of application:
13.10.93 Bulletin 93/41

(84) Designated Contracting States:
DE FR GB NL

(71) Applicant: **MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.**
1006, Oaza Kadoma
Kadoma-shi, Osaka-fu, 571(JP)

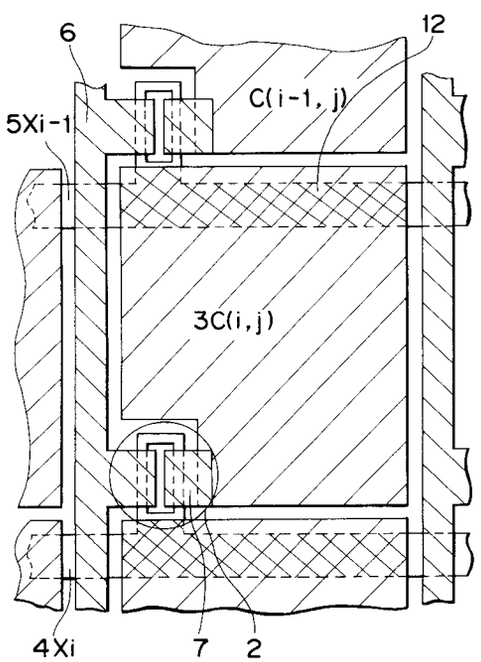
(72) Inventor: **Takeda, Mamoru**
44-16, Nasuzukuri-Higashimachi
Hirakata-shi, Osaka-fu(JP)
Inventor: **Kobayashi, Ikunori**
2-1-10, Horiage-Midorimachi
Sakai-shi, Osaka-fu(JP)

(74) Representative: **Eisenführ, Speiser & Partner**
Martinistrasse 24
D-28195 Bremen (DE)

(54) Liquid crystal display panel.

(57) A liquid crystal display panel which includes a plurality of signal lines Yj (6) (j = 1-N: total signal line number N) and a plurality of scanning lines Xi (5) (i = 1-M) arranged in a matrix pattern of NxM, and thin film transistors (2) for switching signal inputs between a display pixel electrode (3) C (i, j) and signal wiring Yj, disposed to correspond to respective intersections of the signal lines and the scanning lines, and auxiliary capacitance Cadd formed in electrically parallel relation with the display pixel electrode C (i, j) composed of liquid crystal. The auxiliary capacitance Cadd is formed between the scanning line Xi-1 controlling the display pixel electrode C(i-1, j) at a previous stage of the display pixel electrode C (i, j) and display pixel electrode C (i, j), and disposed in such a positional relation that the display pixel electrode C (i, j) completely covers the scanning line Xi-1 at the previous stage in a direction of its line width in terms of a cross sectional construction. By the above arrangement, variation of display pixel signal due to leaking electric field from the gate line may be reduced.

Fig.1(a)



EP 0 565 125 A1

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention generally relates to a display device and more particularly, to a liquid crystal display panel employing active elements.

Conventionally, as a transistor array for a liquid crystal display device used for the above purpose, there has been provided an arrangement as shown in Figs. 2(a) and 2(b), and disclosed, for example, in a paper SID 89 DIGEST p.114 "Rear-Projection TV using High-Resolution a-Si TFT-LCD". More specifically, the array substrate as referred to above includes gate electrode 4 for scanning lines X1-XM, source electrode 6 for signal lines Y1-YN, and further, thin film transistors (referred to as TFT hereinafter) 2 formed corresponding to respective intersections, with drain electrode 7 of the respective TFT being connected to pixel electrode 3. Liquid crystal 13 is inserted between a substrate 1 constituting the TFT and a confronting electrode 14, and independent pixels are formed between the pixel electrode 3 and confronting ground electrode 16 provided on the confronting substrate 14, with the liquid crystal 13 functioning as a capacitance equivalently. There are many cases where an auxiliary capacitance 12 is added in electrically parallel relation thereof depending on necessity in order to improve holding of the signal voltage. For constituting such auxiliary capacitance, it has been recent trend to form the auxiliary capacitance 12 between the scanning lines 5Xi-1 at a previous stage and said display pixel electrode 3 in order to reduce the number of masks.

However, in the case where the liquid crystal display mode is driven by a normally white mode (referred to as N.W. mode hereinafter) in which the display is made black during applying of voltage and it is made white during non-applying of voltage, due to occurrence of non-uniformity in the electric field within the pixels, there has been such a problem that consequent non-uniformity takes place in the orientation of liquid crystal molecules within the image area, thus resulting in lowering of the display quality arising from visible irregularity of the display.

Still referring to Figs. 2(a) and 2(b) showing the conventional TFT-LCD of the previous stage capacitance type, problems taking place in the planar and sectional constructions in the known arrangement will be described hereinafter.

In the conventional arrangement formed with the previous stage auxiliary capacitance 12, the display pixel electrode 3C (i, j) do not perfectly cover the scanning electrode 5Xi-1 at the previous stage in the direction of the line width, and thus, edge portion of the previous stage electrode 5Xi-1 located close to said display pixel electrode 3C (i, j) is exposed. The exposure of the scanning electrode 5Xi-1 in terms of plane through the insulative layer results in the local lowering of transmission factor due to non-uniformity of signal potential within the pixels arising from leakage of the signal potential of the gate into the pixels. More specifically, in the above known arrangement, on the assumption, for example, that the signal applied to the pixel 3C (i, j) is at 4V, potential of gate electrode 4Xi and 5Xi is at -9V as an off potential, and potential of a confronting substrate 14 is at 0V, the potential distribution in the liquid crystal 13 constituting the pixels 3C (i, j) will be represented as shown in Fig. 3, and thus, non-uniformity of electric field distribution within the pixels 3C (i, j) becomes larger, thereby forming distribution within one pixel face in a transmittance characteristic of light.

Accordingly, it has been necessary to hide the display from the pixel edge as much as 8μm in total, i.e., about 4μm from the edge of the pixel electrode 3 as the non-uniformity portion of the signal potential, and also, about 4μm as a margin for combining a black matrix disposed at the confronting substrate 14 and the pixel electrode 3. Therefore, there has been such a problem that display aperture ratio of the pixel is lowered as the density becomes higher.

2. Description of the Prior Art

SUMMARY OF THE INVENTION

Accordingly, an essential object of the present invention is to provide a liquid crystal display panel which is so arranged that display potential thereof is not adversely affected by an electric field from the gate electrode of a thin film transistor (referred to as TFT hereinafter), thereby to improve display quality of a thin film transistor-liquid crystal display (referred to as TFT-LCD hereinafter).

Another object of the present invention is to provide a liquid crystal display panel of the above described type which is simple in construction and stable in functioning at high reliability, and can be readily manufactured on a large scale at low cost.

In accomplishing these and other object, according to one aspect of the present invention, the liquid crystal display panel has a pattern configuration in which a pixel electrode 3C (i, j) formed, through an inter-layer insulation, with respect to a gate scanning electrode or scanning line 5Xi-1 at the previous stage, completely covers said gate scanning electrode 5Xi-1 in a direction of width thereof.

More specifically, according to one preferred embodiment of the present invention, there is provided a liquid crystal display panel which includes

a plurality of signal lines Yj (j = 1-N: total signal line number N) and a plurality of scanning lines Xi (i = 1-M) arranged in a matrix pattern of NxM, and thin film transistors for switching signal inputs between a display pixel electrode C (i, j) and signal wiring Yj, disposed to correspond to respective intersections of said signal lines and said scanning lines, and auxiliary capacitance Cadd formed in electrically parallel relating with the display pixel electrode C(i, j) composed of liquid crystal. The auxiliary capacitance Cadd is formed between the scanning line Xi-1 controlling the display pixel electrode C (i-1, j) at a previous stage of said display pixel electrode C (i, j) and said display pixel electrode C (i, j), and disposed in such a positional relation that said display pixel electrode C (i, j) completely covers said scanning line Xi-1 at the previous stage in a direction of its line width in terms of a cross sectional construction.

By the arrangement according to the present invention as described above, since the pixel electrode 3C (i, j) completely covers the scanning electrode 5Xi-1 at the previous stage, the gate electrode 5Xi-1 is hidden by the pixel electrode 3C (i, j) as observed in terms of a plane, and leakage of potentials of the gate electrodes 4 and 5 onto the pixel electrode 3C (i, j) is suppressed. Accordingly, it becomes possible to prevent the non-uniformity of the display potential within the display electrode 3C (i, j) due to leaking electric field of the gate potential. Moreover, since the width of the black matrix 15 provided on the confronting electrode 14 may be reduced by the amount equivalent to the non-uniformity of signal as compared with the conventional arrangement, the display portion is to be hidden by 4μm which is the combining margin between the black matrix 15 and the pixel 3C, and thus, the display aperture ratio of the pixel can be improved by that extent. By way of example, on the assumption that the pixel pitch is 100μm vertically and 100μm horizontally, and the display electrode portion is 80μm longitudinally and 80μm laterally, the display pixel portion formed with black matrix in the conventional arrangement was 72μm longitudinally and 72μm laterally, with the display pixel aperture ratio of 52%. On the contrary, in the construction according to the present invention, the display pixel portion is 76μm longitudinally and 76μm laterally, with aperture ratio at 58%, thus showing an improvement of as much as 6% over the conventional construction. The advantage that the width of the black matrix may be made narrower, contributes to the improvement of the aperture ratio as the pixels become higher in density.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other objects and features of the present invention will become apparent from the following description taken in conjunction with the preferred embodiment thereof with reference to the accompanying drawings, in which;

Fig. 1(a) is a fragmentary top Plane view of a TFT-LCD according to one preferred embodiment of the preferred embodiment of the present invention,

Fig. 1(b) is a fragmentary side sectional view on an enlarged scale, of the TFT-LCD of Fig. 1,

Fig. 2(a) is a fragmentary top plane view of a conventional TFT-LCD having a previous stage capacitance,

Fig. 2(b) is a fragmentary side sectional view on an enlarged scale of the conventional TFT-LCD of Fig. 2(a),

Fig. 3 is a schematic cross sectional diagram for explaining non-uniformity of potential distribution in the pixel within liquid crystal for the conventional arrangement,

Fig. 4 is a schematic fragmentary cross section showing a first step for forming the TFT array according to one preferred embodiment of the present invention,

Fig. 5 is a cross section similar to Fig. 4, which particularly shows a second step therefor,

Fig. 6 is a cross section similar to Fig. 4, which particularly shows a third step therefor,

Fig. 7 is a fragmentary cross sectional view showing a TFT array according to a second embodiment of the present invention,

Fig. 8 is also a fragmentary cross sectional view similar to Fig. 7, which particularly shows a third embodiment of the present invention,

Fig. 9(a) is a top plane view similar to Fig. 1, which particularly shows a planer positional relation of a black matrix formed on the TFT-LCD in the embodiment of the present invention, with respect to the pixel electrode, and

Fig. 9(b) is a schematic fragmentary side sectional view taken along the line IX(b)-IX(b) in Fig. 9(a), showing a side sectional positional relation of the black matrix formed on the TFT-LCD in the embodiment of the present invention, with respect to the pixel electrode.

DETAILED DESCRIPTION OF THE INVENTION

Before the description of the present invention proceeds, it is to be noted that like parts are designated by like reference numerals throughout the accompanying drawings.

Referring now to the drawings, the liquid crystal display device according to the present invention will be described hereinafter.

Figs. 1(a) and 1(b) show the construction of an array for a TFT liquid crystal display device according to one preferred embodiment of the present invention.

As shown in Figs. 1(a) and 1(b), by adopting a construction to completely cover the gate electrode 5Xi-1 at a previous stage with pixel electrode 3C (i, j), leakage of electric field from the gate electrode 5Xi-1 can be prevented by shielding, and thus, uniformity of potential within the pixel C (i, j) may be improved. In this case, the gate electrode 4 of the TFT 2 for driving the display electrode 3C (i, j) is connected to scanning line 4Xi, and the display pixel 3C (i, j) forms an auxiliary capacitance 12 with respect to the scanning line 5Xi-1 at a previous stage through the gate insulative layer 8.

The planer and side sectional constructions as shown in Figs. 1(a) and 1(b) can be achieved by following processes as described hereinbelow. For a first step, a substrate including a transparent substrate 1, and gate electrode 4Xi (i = 1-M), 5Xi-1, a gate insulative layer 8 formed by P-CVD method, etc., which are formed on said substrate 1, and a semi-conductor layer 9 with a channel protective layer 10 and another semi-conductor layer 9' doped with impurities for ohmic contact further formed on said semi-conductor layer 9 with a channel protective layer 10 is prepared as shown in Fig. 4. In a second step, when a transparent layer which serves as the pixel electrode 3C (i, j) is formed, it is so arranged that the gate electrode 5Xi-1 at the previous stage is completely covered thereby, so as to form said pixel electrode 3C (i, j) and its auxiliary electrode 12 Cadd as illustrated in Fig. 5 . Further, for a third step as shown in Fig. 6, source electrode 6 and drain electrode 7 are formed on the substrate, thereby to form the TFT array in a matrix pattern. Moreover, in order to improve the reliability of the TFT 2, SiNx18 deposited by P-CVD method or the like is formed on said substrate with the pixel portion opened thereon.

As is seen from Figs. 1(a) and 1(b), in the positional relation in the cross section, between the pixel electrode 3 forming the auxiliary capacitance 12 and the scanning line 5Xi-1 at the previous stage, the pixel electrode 3 completely covers the scanning line 5Xi-1 in the direction of its line width, different from the conventional arrangement.

In a TFT array according to a second embodiment of the present invention as shown in Fig. 7, in the structure of the source electrode 6 and the drain electrode 7, the pixel electrode 3C (i, j) is positioned at the upper layer from the source electrode 6 and the drain electrode 7 through the insulative layer 18, with the gate electrode 5Xi-1 at the previous stage being completely covered by the drain electrode 7. Moreover, the pixel electrode 3C (i, j) is connected with the drain electrode 7 through contact holes 19 formed in the insulative layer 18 located at the lower layer of the pixel electrode 3C (i, j).

In a TFT array according to a third embodiment of the present invention as shown in Fig. 8, in the positional relation in the cross section, of the pixel electrode 3C (i, j), the source electrode 6, and the drain electrode 7, said pixel electrode 3C (i, j) is located at a lower layer than said source electrode 6 and the drain electrode 7. The pixel electrode 3 and the drain electrode 7 are connected through contact holes 19 formed in the insulative layer 8 provided on said pixel electrode. In this case, an edge portion of the gate electrode 5Xi-1 at the previous stage near the pixel electrode 3C (i,j) with respect to the direction of line width is covered by the drain electrode 7 connected with the pixel electrode 3C (i, j) or the gate electrode 5Xi-1 is completely covered thereby in its line width direction.

Moreover, in any of the foregoing embodiments, the black matrix may be formed by utilizing the black matrix 15 provided on the confronting substrate 14 holding the liquid crystal 13 with respect to the TFT array substrate, and part of the gate electrode 5Xi-1 covered by the auxiliary electrode 12, by which arrangement, since the gate portion 20 not covered by the black matrix 15 on the confronting substrate 14 is covered by the pixel electrode 3C (i, j), it is a region not affected by the gate electric field. Thus, transmission light is shielded by the gate electrode to serve as the black matrix, and further, owing to the fact that the electric field within the pixels is not affected by the gate electric field, the electric field of the transmission pixel portion may be made uniform.

As is clear from the foregoing description, according to the arrangement of the present invention, the non-uniformity of potential within the pixels and lowering of the aperture ratio which are the problems in the display quality for the TFT-LCD can be remarkably improved by covering the gate electrode with the pixel electrode. For example, when the black matrix width is held constant, in the case of 100μm square pitch pixel, the width of the black matrix at 28μm in the conventional arrangement may be reduced to 24μm according to the present invention, while in the aperture ratio at 52% can be improved to 58%. Moreover, in the case of 50μm square pitch, 19% in the conventional example may be improved to 27% according to the present invention. Therefore, the arrangement of the present invention displays more effect as the pixel density becomes higher. Furthermore, since the simple construction is adopted to form the auxiliary capacitance with respect to the scanning line, the TFT array may be constituted without increasing the number of masks, and thus, it be-

comes possible to improve the display quality not requiring particular cost increase.

Although the present invention has been fully described by way of example with reference to the accompanying drawings, it is to be noted here that various changes and modifications will be apparent to those skilled in the art. Therefore, unless otherwise such changes and modifications depart from the scope of the present invention, they should be construed as included therein.

Claims

1. A liquid crystal display panel which comprises a plurality of signal lines Yj (j = 1-N: total signal line number N) and a plurality of scanning lines Xi (i = 1-M) arranged in a matrix pattern of NxM, and thin film transistors for switching signal inputs between a display pixel electrode C (i, j) and signal wiring Yj, disposed to correspond to respective intersections of said signal lines and said scanning lines, and auxiliary capacitance Cadd formed in electrically parallel relation with the display pixel electrode C (i, j) composed on liquid crystal, said auxiliary capacitance Cadd being formed between the scanning line Xi-1 controlling the display pixel electrode C (i-1, j) at previous stage of said display pixel electrode C (i, j) and said display pixel electrode C (i, j), and disposed in such a positional relation that said display pixel electrode C (i, j) completely covers said scanning line Xi-1 at the previous stage in a direction of its line width in terms of a cross sectional construction.

2. A liquid crystal display panel as claimed in Claim 1, wherein for determining transmission light of the thin film transistor liquid crystal display panel, there are provided black matrixes formed on a confronting substrate, and black matrixes for shielding the transmission light through employment of part of gate electrode at the side of the thin film transistor array covered by the pixel electrode.

3. A liquid crystal display panel as claimed in Claim 1, wherein the display panel electrode C (i, j) in the thin film transistor liquid crystal display panel has a construction that said auxiliary capacitance is formed in such a positional relation that the scanning line Xi-1 at the previous stage is completely covered in a direction of line width thereof by the drain electrode of said thin film transistor, and said drain electrode and said display pixel electrode are connected through contact holes formed in an insulative layer positioned at a lower layer of said pixel electrode.

4. A liquid crystal panel as claimed in Claim 1, wherein the auxiliary capacitance is formed by covering edge portion near the display pixel with respect to the direction of the line width of the scanning line Xi-1 at the previous stage or by completely covering scanning line width, with the drain electrode of the thin film transistor, said drain electrode being connected to the display pixel electrode through contact holes formed in an insulative layer positioned on an upper layer of the display pixel electrode.

Fig.1(a)

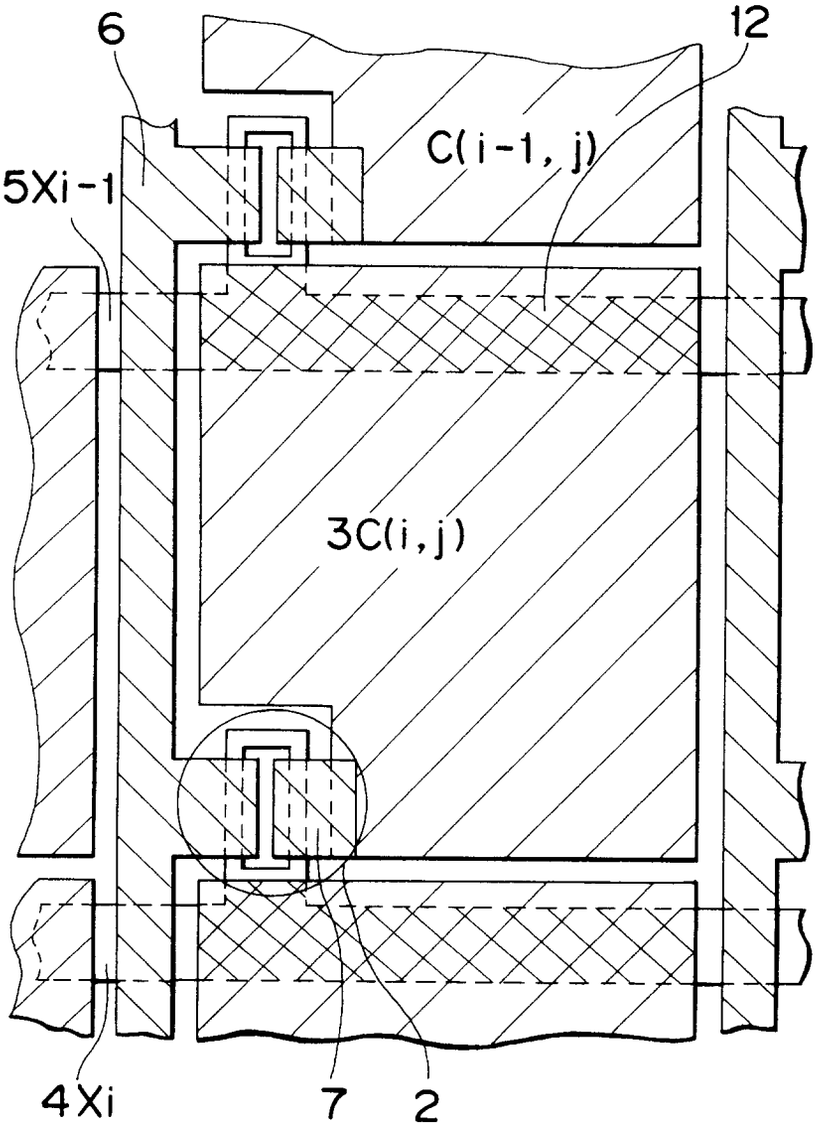


Fig. 1(b)

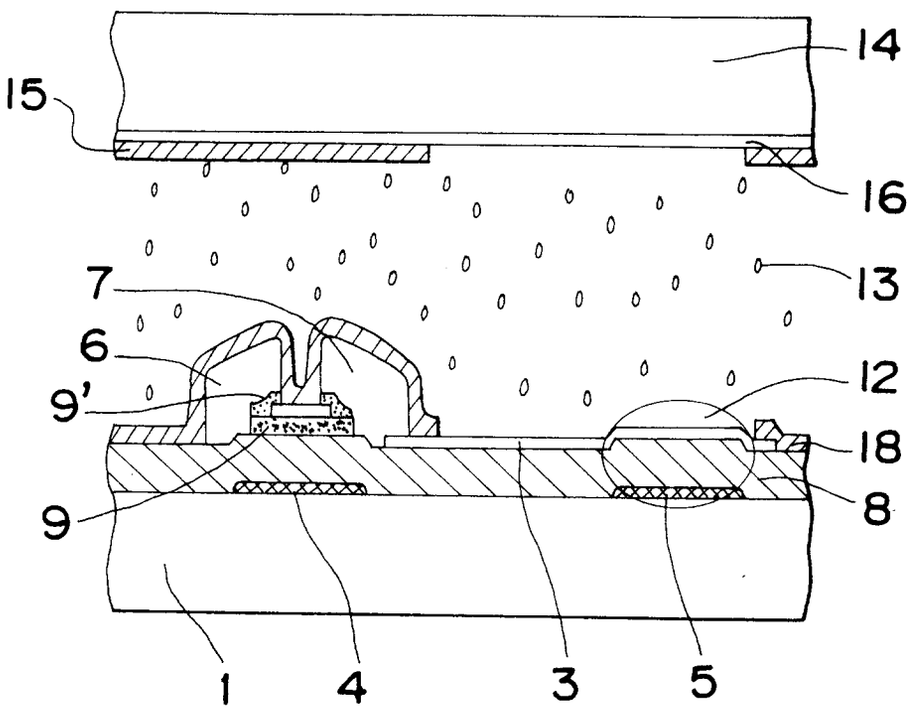


Fig.2(a) PRIOR ART

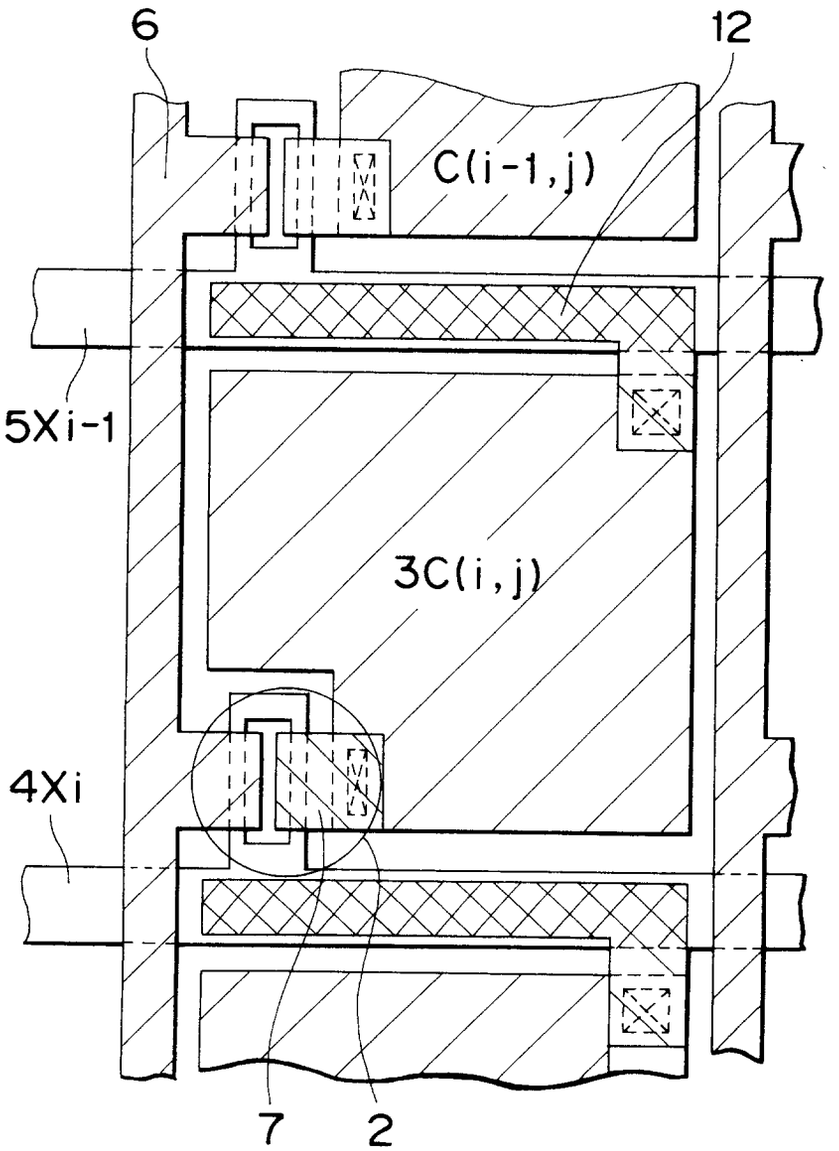


Fig. 2(b) PRIOR ART

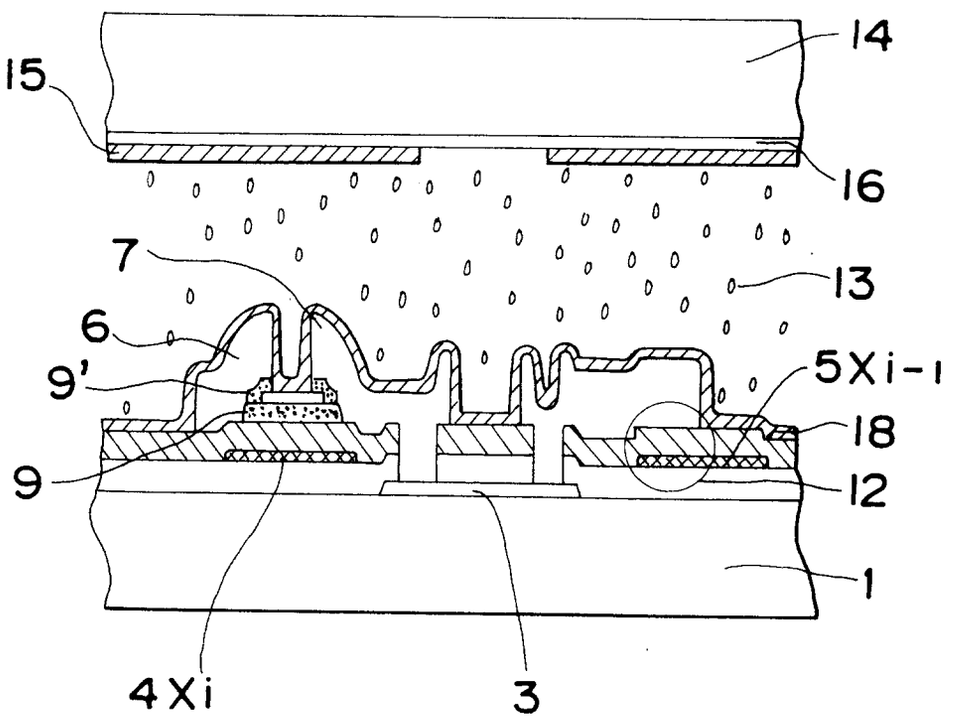


Fig.3 PRIOR ART

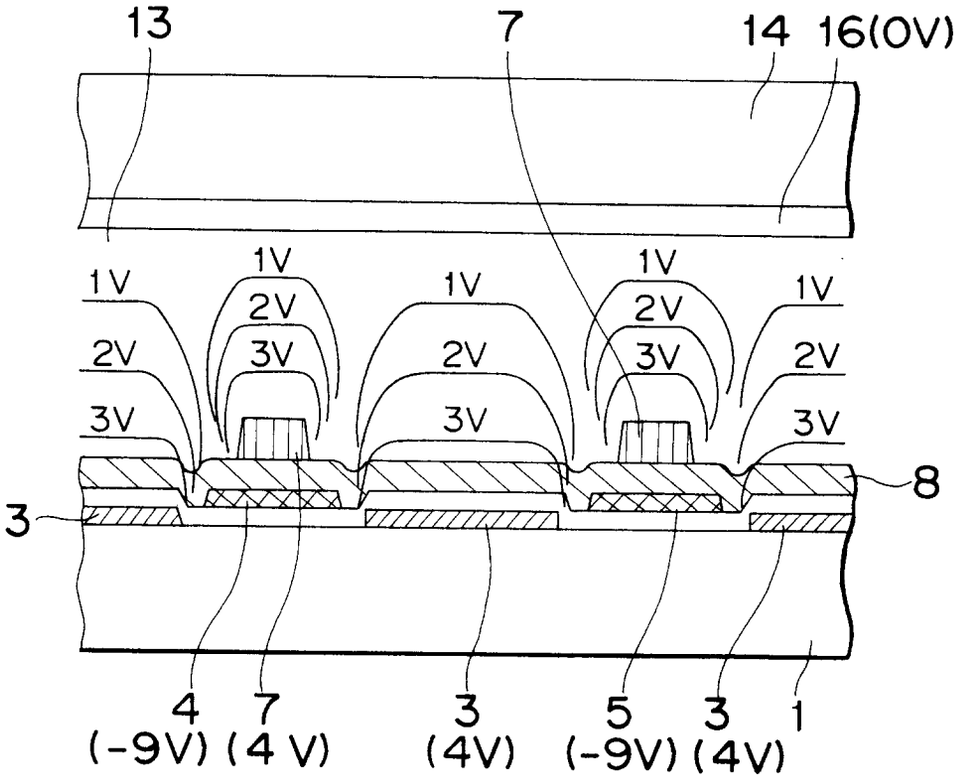


Fig.4

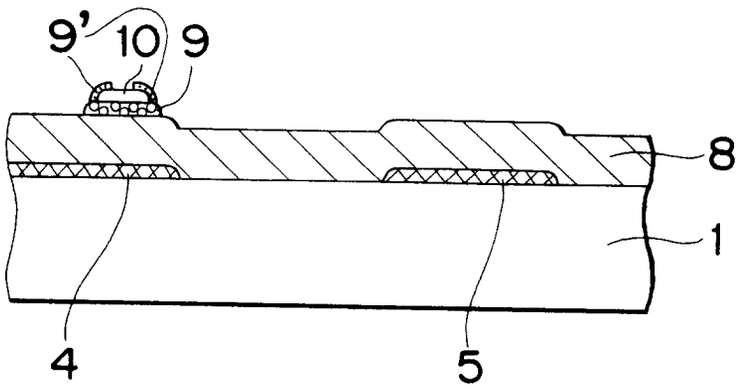


Fig.5

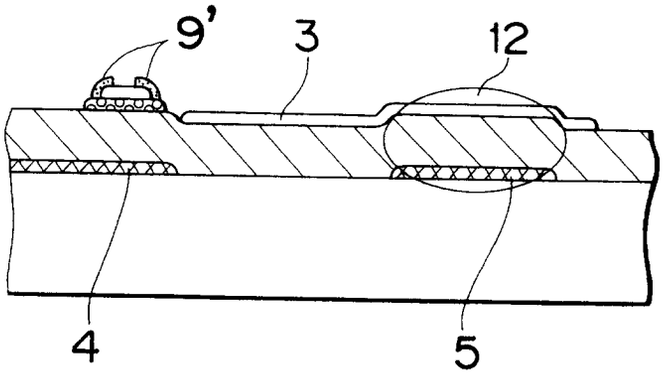


Fig.6

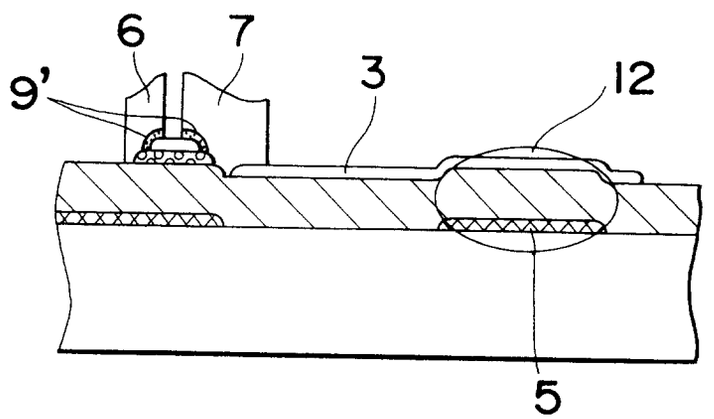


Fig.7

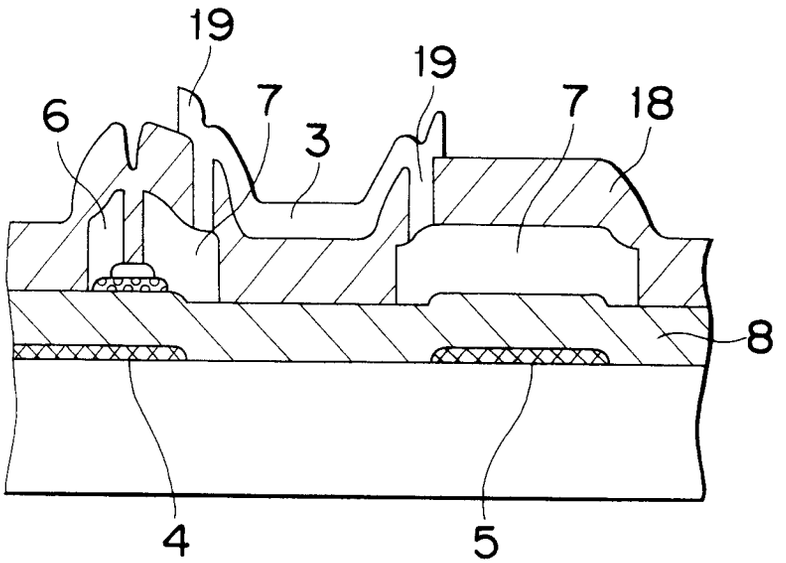


Fig.8

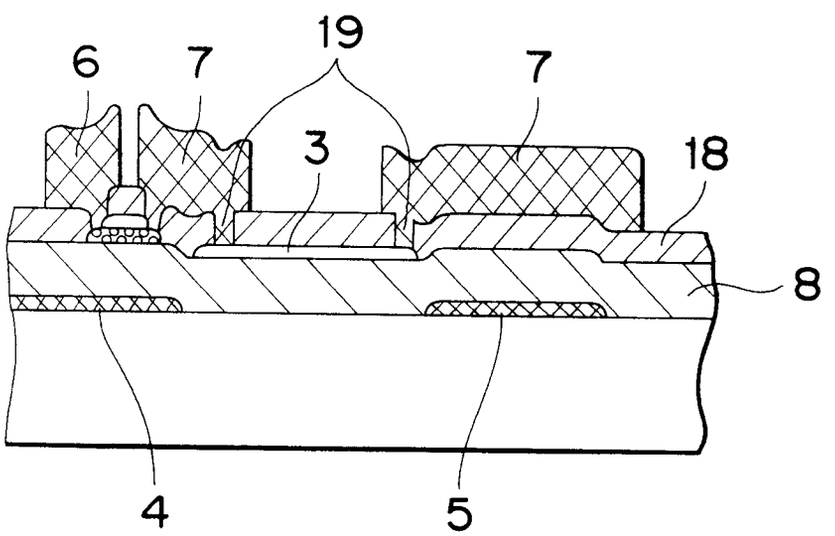


Fig.9(a)

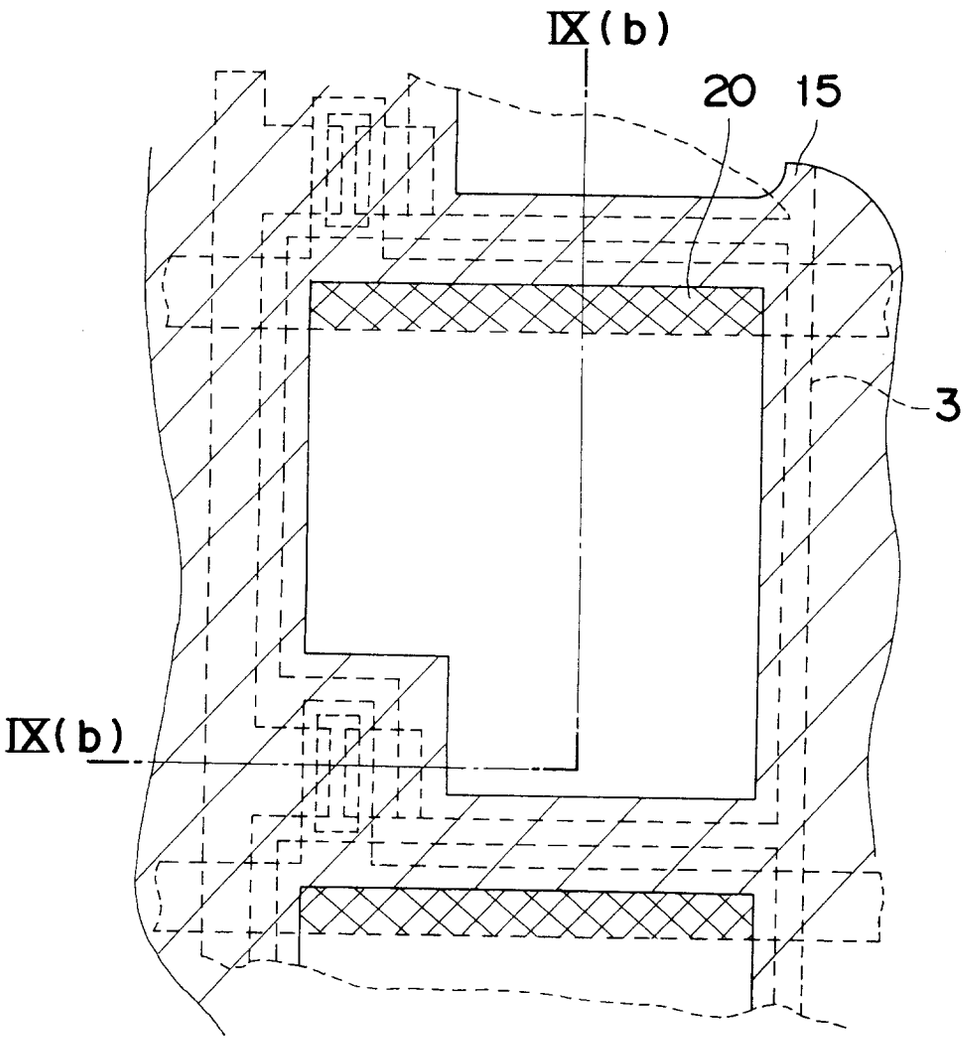
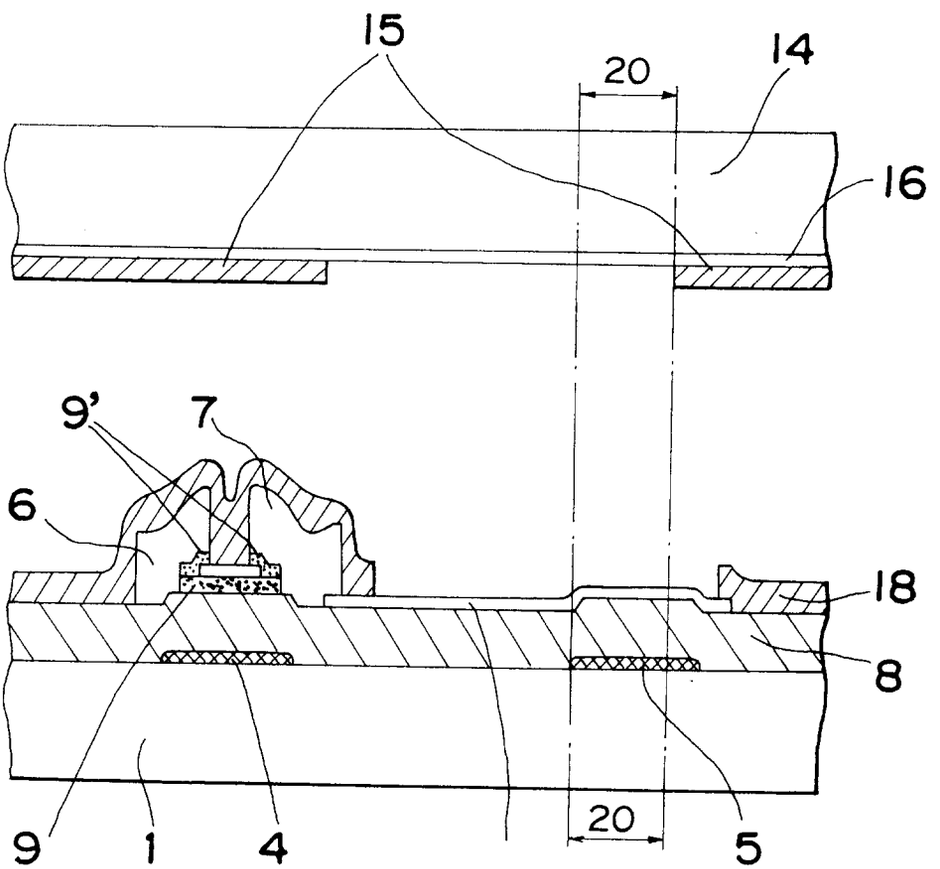


Fig. 9(b)



European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 93 10 5927

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X	EP-A-0 288 011 (HITACHI) * figure 8; example 2 *	1	G02F1/136
D,A	SID INTERNATIONAL SYMPOSIUM, DIGEST OF TECHNICAL PAPERS 1989, PLAYA DEL REY, US pages 114 - 117 , XP000076848 I.KOBAYASHI ET AL. 'Rear-Projection TV Using High-Resolution a-Si TFT-LCD' * Section 'Structure of LCD Panel Module' * figure 3 *	1-4	
A	SID INTERNATIONAL SYMPOSIUM, DIGEST OF TECHNICAL PAPERS 1991, PLAYA DEL REY, US pages 215 - 218 M.TSUMURA ET AL. 'High-Resolution 10.3-in.-Diagonal Multicolor TFT-LCD' * page 215, right column, last paragraph - page 216, left column, paragraph 2; figure 2 *	1,2	
			TECHNICAL FIELDS SEARCHED (Int. Cl.5)
			G02F

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	16 JULY 1993	WONGEL H.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P0401)