EUROPEAN PATENT APPLICATION

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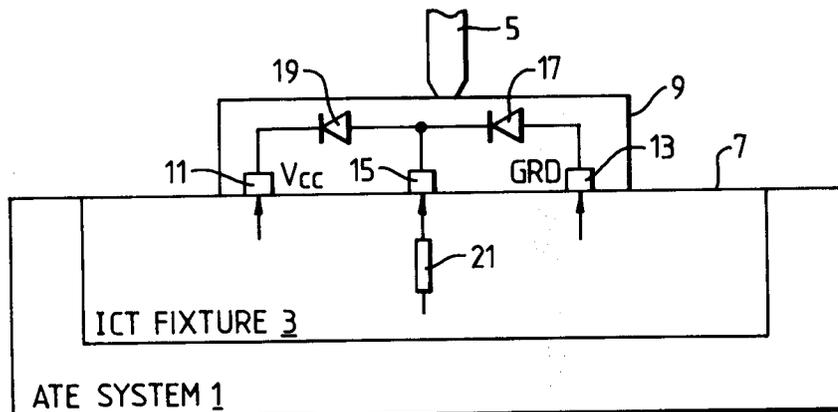GEC Patent Department
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(54) Method of testing continuity of a connection between an IC and a PCB.

(57) A method of testing the electrical conductivity of a connection between an integrated circuit device (9) and a circuit board (7) to which the device (9) is connected, said device (9) including a current path between a further connection (13) thereto and the connection (15) to be tested, said method comprising the steps of, whilst the circuit is inoperative: applying via said board (7) a potential of a first amount to said further connection (13); applying via said board (7) a potential of a second different amount to the connection (15) being tested; and utilising probe means (5) positioned adjacent said device (9) to sense indirectly current in said current path, the presence of current indicating that the connection (15) being tested is conductive.

Fig.1.

This invention relates to a method of testing the electrical conductivity of a connection between an integrated circuit device and a circuit board to which the device is connected.

A known method of testing such a connection comprises the application of potentials to circuit nodes of the circuit board and the monitoring of the responses of the circuit to these potentials. The potentials are generated by an automatic test equipment (ATE) central control system and applied to the circuit nodes by an in-circuit test (ICT) fixture of the equipment which supports the circuit board. The fixture comprises a so called bed of nails which contact the circuit nodes. The responses of the circuit picked-up by the bed of nails are passed to the central control system. The control system has full knowledge of the circuit board and the devices connected thereto and therefore knows what responses to expect to various patterns of potentials it generates. The control system is thus able to detect any bad connections between the devices and the board.

A disadvantage with this method is that it requires a detailed knowledge of the board and the devices connected thereto. The relevant information may not be available. Another disadvantage with this method is the lengthy time it takes to write the test program run by the central control system, which program defines the various patterns of potentials to be applied and the responses to be expected thereto.

Another known method uses the ATE system and ICT fixture mentioned above to test for the presence of a diode of the device under test connected between the pin under test and a ground supply pin of the device. The diode is part of voltage protection circuitry of the device provided for the pin under test. A voltage is applied to the pin under test to forward bias the diode, and the voltage between the pin under test and ground, i.e. the voltage dropped across the diode, is measured by the ATE system. If the characteristic forward voltage drop is measured the pin connection under test is good.

A disadvantage with this method is seen in the case where a pin of another device, similarly protected by means of a diode as the diode of the device under test, is on the same circuit node as the pin under test. If the connection of the pin under test is bad but the connection of the pin of the other device is good, the characteristic forward voltage drop will still be measured, and therefore the bad connection of the pin under test not detected.

According to the present invention there is provided a method of testing the electrical conductivity of a connection between an integrated circuit device and a circuit board to which the

device is connected, said device including a current path between a further connection thereto and the connection to be tested, said method comprising the steps of, whilst the circuit is inoperative: applying via said board a potential of a first amount to said further connection; applying via said board a potential of a second different amount to the connection being tested; and utilising probe means positioned adjacent said device to sense indirectly current in said current path, the presence of current indicating that the connection being tested is conductive.

A method of testing the electrical conductivity of a connection between an integrated circuit device and a circuit board to which the device is connected in accordance with the present invention will now be described, by way of example, with reference to the accompanying drawings, in which:-

Figure 1 is a schematic illustration of an equipment for carrying out the method, a circuit board connected thereto, and a CMOS device connected to the board;

Figure 2 shows the position of a probe of the equipment relative to the CMOS device of Figure 1;

Figure 3 is a schematic diagram showing in greater detail than it is shown in Figure 1 a part of the equipment of Figure 1;

Figure 4 is a further illustration of the equipment showing in particular probes thereof and a frame structure for holding the probes in position;

Figure 5 is a circuit diagram of the circuitry of each of the probes of the equipment; and

Figure 6 illustrates various voltage waveforms present in use of the equipment.

Referring to Figure 1, the equipment comprises an ATE central control system 1, an ICT fixture 3, a plurality of inductive probes 5 only one of which is shown in Figure 1, and a frame structure for holding the probes in position (not shown in Figure 1). A circuit board 7 is supported by and connected to fixture 3. A CMOS device 9 is connected to board 7. Device 9 includes V_{cc} 11 and ground 13 supply pin connections and signal pin connection 15. Signal pin 15 is protected by CMOS device signal pin voltage protection circuitry comprising lower 17 and upper 19 clamp diodes. Fixture 3 includes a resistor 21.

Control system 1 generates potentials for application to circuit nodes of board 7. The potentials are applied by fixture 3 which comprises a so called bed of nails which contact the circuit nodes.

Use of the equipment to test the electrical conductivity of signal pin connection 15 to board 7 will now be described.

The grounds of board 7 and ATE system 1 are not connected, i.e. board 7 is not powered up by system 1, in effect therefore board 7 floats. Poten-

tials of approximately 5V are applied to V_{cc} pin 11 and ground pin 13. A train of voltage pulses, as shown in Figure 6 at (i), of known frequency is applied via resistor 21 to pin under test 15. The potential varies between 5V and 0V.

When the potential applied to pin 15 is 5V no current flows in device 9. Assuming pin connection 15 is good, when the potential applied is 0V lower clamp diode 17 is forward biassed, upper clamp diode 19 reverse biassed. Thus, current will flow in the path between pins 13 and 15 via diode 17. It is to be noted that it is assumed here that ground pin connection 13 is good. Resistor 21 serves to limit the flow of current. If pin connection 15 is not good no current will flow in device 9.

Inductive probe 5 shown in Figure 1, positioned over device 9 picks up any current flow in device 9 and thereby provides an indication of whether or not pin connection 15 is good. As shown in Figure 2 the probe 5 is positioned over the internal silicon wafer 23 of CMOS device 9 to sense current flow in device 9. Figure 2 also shows the internal bond wires 25 and pin connections of device 9, of which pin connections pins 11, 13 and 15 of Figure 1 are three.

Referring also to Figure 3, ATE system 1 comprises a software controller 27, a power supply 29, transistor switches 31 capable of supplying 5V or 0V, and a matrix of relays 33. As mentioned previously, ICT fixture 3 comprises a bed of nails 35 which contact circuit nodes of circuit board 7 (not shown in Figure 3), and resistor 21 (see also Figure 1). Resistor 21 is connected between nails F and G which are not in use, i.e. do not contact circuit nodes of board 7.

The operation of the part of the equipment shown in Figure 3 to apply the train of voltage pulses to pin connection 15 (see Figure 1) via resistor 21 will now be described.

Assume nail D contacts the relevant circuit node for pin 15 of device 9. Relays a and b are closed by controller 27 connecting resistor 21 via pole 37 to nail D. The application of the train of voltage pulses to nail D is achieved by controller 27 repeatedly turning the transistor switch 31 allocated to nail G on and off to provide a voltage alternating between 5V and 0V. Applying the train of voltage pulses to another nail for the purpose of testing another pin of device 9 or the pin of another device on circuit board 7 is simply achieved by opening relay b and closing the relay on pole 37 under the nail to which the pulses are to be applied. Thus, the application of the train of pulses to another pin is achieved by opening the relay on pole 37 under the present pin and closing the relay on pole 37 under the next pin. For example, to transfer the train from nail D to nail C relay b is opened and relay c is closed, from nail C to nail B

relay c is opened and relay d is closed.

Referring also to Figure 4, shown therein is the aforementioned frame structure 43 which holds each of the plurality of probes 5 in position over its respective device 9 for the testing of the pin connections to circuit board 7 of the device 9. Structure 43 is secured to ICT fixture 3. Probes 5 are connected by wires 45 to unused nails of fixture 3. By means of relays (not shown in Figure 3) provided in respect of these unused nails system 1 selects the appropriate probe 5. System 1 then samples the voltage provided thereby, for more detail on this see below.

Referring also to Figures 5 and 6, the circuitry of each probe 5 comprises a damped tuned circuit 47, an amplifier 49, an envelope detector 51, and a supply decoupling capacitor 53. Tuned circuit 47 comprises an inductor 55, a capacitor 57 and a resistor 59. Amplifier 49 comprises a transistor 61, resistors 63, 65, 67 and a capacitor 69. Envelope detector 51 comprises a transistor 71, resistors 73, 75, 77, and capacitors 79, 81.

Tuned circuit 47 inductively detects current in the respective device 9. Voltage waveform (i) in Figure 6, referred to previously, represents the train of voltage pulses applied to pin connection 15 (see Figure 1). Voltage waveform (ii) represents the signal provided by circuit 47 as it detects current flow in device 9 between ground pin 13 and pin 15 via diode 17. It is to be noted from waveform (ii) that on the voltage applied to pin 15 being switched to 5V the voltage provided by circuit 47 drops whereas on the voltage applied being switched to 0V the voltage provided rises. The signal provided by circuit 47 passes to amplifier 49 and enters the base of transistor 61 biased by resistors 63, 65. Capacitor 69 provides an AC ground reference for the signal from detector circuit 47. Resistor 67 provides a collector load for transistor 61. Voltage waveform (iii) represents the amplified inverted output signal of amplifier 49.

The signal provided by amplifier 49 passes to envelope detector 51 where it is AC coupled to transistor 71 via capacitor 79. Transistor 71 is biased via resistors 73, 75. The DC base voltage on transistor 71 can be varied by changing the potential of a bias voltage applied at input 83. On the positive going slopes of the signal provided by amplifier 49 (waveform (iii)) capacitor 81 charges quickly while on the negative going slopes capacitor 81 decays slowly through resistor 77. With the passage of time the charge on capacitor 81 increases exponentially. Voltage waveform (iv) represents the change in the output voltage V_{out} of envelope detector 51 with time.

A predetermined test time is set which starts with the beginning of the application of the train of voltage pulses to pin under test 15. On expiry of

this time ATE system 1 samples voltage V_{out}. If the sampled voltage is above a threshold voltage set by system 1 pin connection 15 is good otherwise it is not.

The bias voltage applied at 83 (the probe bias) is set so that background noise, especially that from the circuit tracks on the board, is ignored. The worst case for the current sensing is where a device adjacent and connected to the device being tested draws all of the applied current when the device being tested is open circuit. So that the test is reliable, the probe bias is set so that current in the adjacent device is ignored but current in the device being tested is detected. In practice, of course, an adjacent connected device can never draw all of the applied current due to its internal diode voltage reducing the current in the node of application connecting the two devices.

It is to be appreciated that the equipment described by way of example need not include frame structure 43 and plurality of probes 5, but need include only a single probe to be manually, or by means of a computer controlled positioning system, positioned over the device being tested under the instruction of ATE system 1.

It is also to be appreciated that the coupling of the current sensing probe to the device under test need not be inductive. An alternative indirect form of coupling is capacitive.

It is further to be appreciated that the present invention applies generally to the testing of the pin connections of integrated circuit devices, both digital and analogue. All that is required is that the device include a current path between the pin connection to be tested and another pin connection of the device. This other pin connection need not be a supply pin connection as in the case described by way of example. An example of another type of device that may be tested is a TTL device. TTL devices have the lower clamp diode as shown in Figure 1 in their circuitry but not necessarily the upper clamp diode. The same current path as used in the CMOS device of Figure 1 may therefore be used in TTL devices.

It is also further to be appreciated that the invention finds particular application in testing surface mount devices. This is because open circuit connections of such devices are difficult if not impossible to detect with the naked eye. A further reason is that open circuit connections are common with such devices. The invention also, of course, applies to devices with standard leads, i.e. leads which pass through the circuit board and are soldered on the underside thereof.

Claims

1. A method of testing the electrical conductivity of a connection between an integrated circuit device (9) and a circuit board (7) to which the device (9) is connected, said device (9) including a current path between a further connection (13) thereto and the connection (15) to be tested, said method comprising the steps of, whilst the circuit is inoperative: applying via said board (7) a potential of a first amount to said further connection (13); applying via said board (7) a potential of a second different amount to the connection (15) being tested; and utilising probe means (5) positioned adjacent said device (9) to sense indirectly current in said current path, the presence of current indicating that the connection (15) being tested is conductive.

2. A method according to Claim 1 wherein said further connection (13) is a supply connection to said device (9) and said current path is in a voltage protection network of said device (9) for protecting the connection (15) being tested.

3. A method according to Claim 2 wherein said protection network includes a diode (17) connected between said supply connection (13) and the connection (15) being tested, said current path being via said diode (17).

4. A method according to Claim 1 or Claim 2 or Claim 3 wherein said device (9) is a digital device.

5. A method according to any one of the preceding claims wherein said device (9) is a CMOS or TTL device.

6. A method according to any one of the preceding claims wherein the potential applied to the connection (15) being tested is periodically switched between said second amount and said first amount, said probe means (5) thereby picking-up an oscillating current signal.

7. A method according to Claim 6 wherein said probe means (5) has an inductive pick-up.

8. A method according to Claim 7 wherein said probe means (5) comprises: a tuned circuit (47), an inductor (55) of which provides the inductive pick-up; an amplifier (49) for amplifying the signal provided by the tuned circuit (47); and an envelope detector (51) for receiving the amplified signal and providing an output voltage, the value of which after a pre-

determined time indicates whether the connection (15) being tested is conductive.

9. A method according to any one of the preceding claims wherein the potential applied to the connection (15) being tested is applied by way of a resistor (21) which serves to limit current flow.

10. A method according to any one of the preceding claims wherein: the potentials applied to said further connection (13) and the connection being tested (15) are generated by a central control system (1) of an automatic test equipment; and the potentials are applied by means of a in-circuit test fixture (3) of the test equipment, which fixture (3) supports said circuit board (7) and comprises a plurality of nails (35) which contact circuit nodes on said board (7).

11. A method according to Claim 10 when dependent on Claim 9 wherein said resistor (21) is connected between two further nails (F,G) of said fixture (3) which do not contact circuit nodes on said board (7).

12. A method according to Claim 10 or Claim 11 wherein the automatic test equipment further comprises a frame structure (43) fixed relative to said fixture (3) which holds said probe means (5) in position adjacent said device (9).

13. A method according to any one of Claims 1 to 11 wherein said probe means (5) is positioned adjacent said device (9) manually.

14. A method according to any one of Claims 1 to 11 wherein said probe means (5) is postioned adjacent said device (9) by means of computer controlled positioning system.

Fig.1.

Fig.2.
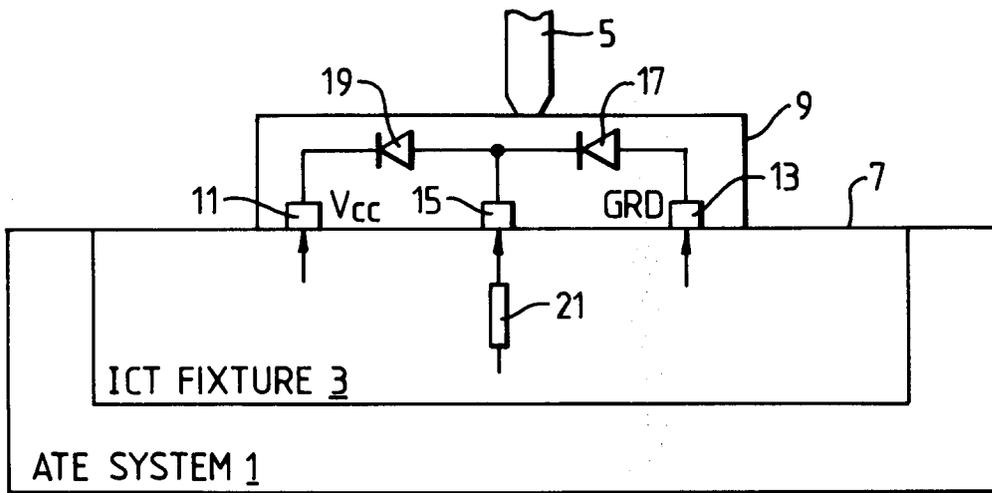
Fig.3.
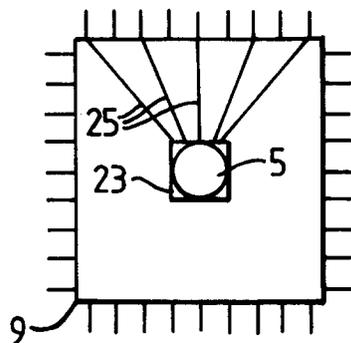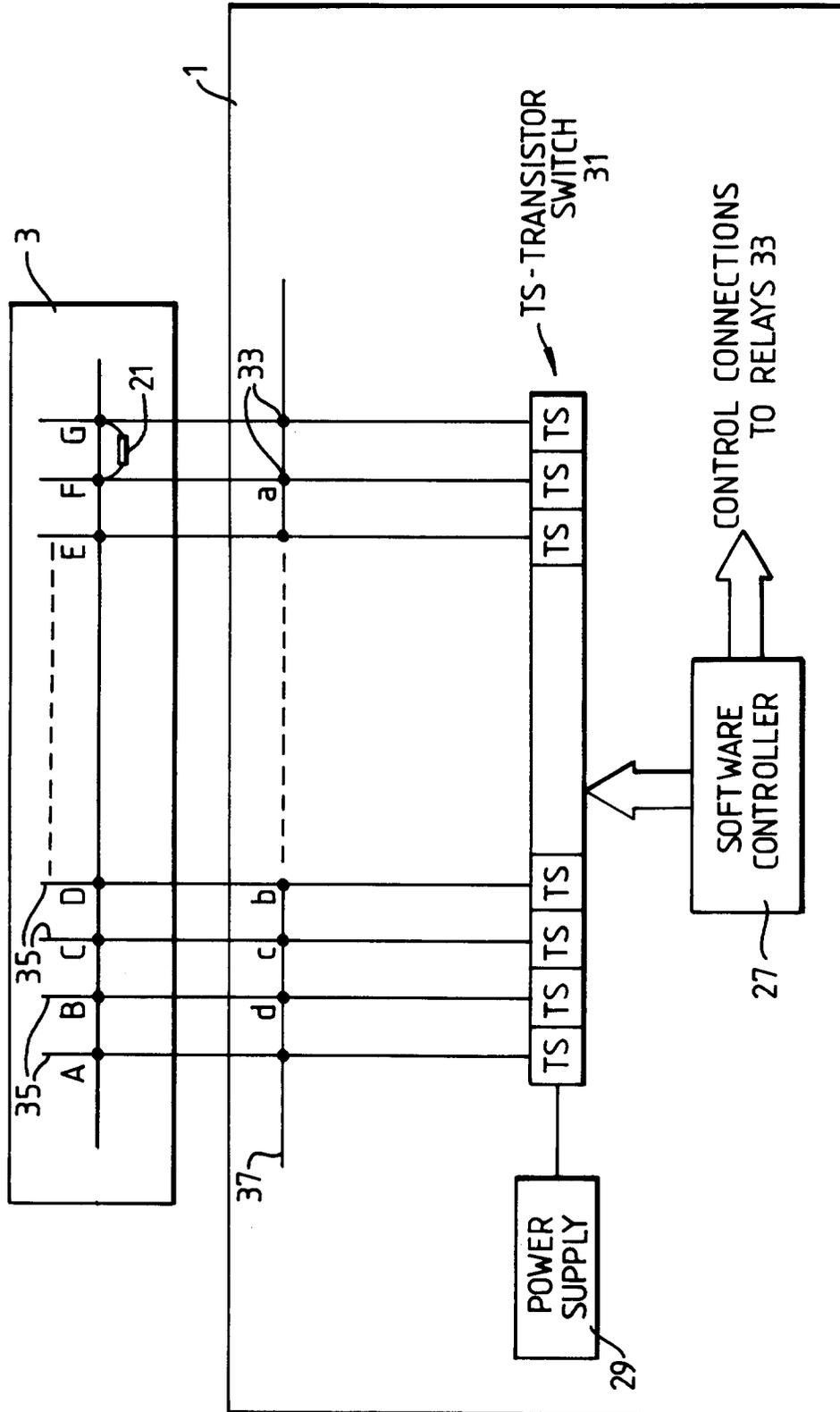

TS-TRANSISTOR SWITCH
31

CONTROL CONNECTIONS TO RELAYS 33

SOFTWARE CONTROLLER
27

POWER SUPPLY
29

Fig.4.

Fig.5.

Fig.6.

(i) TRAIN OF VOLTAGE PULSES APPLIED TO PIN UNDER TEST.

(ii) SIGNAL PROVIDED BY CIRCUIT 47

(iii) SIGNAL PROVIDED BY AMPLIFIER 49

(iv) OUTPUT V_{OUT} OF ENVELOPE DETECTOR 51

THRESHOLD VOLTAGE

QUIESCENT LEVEL
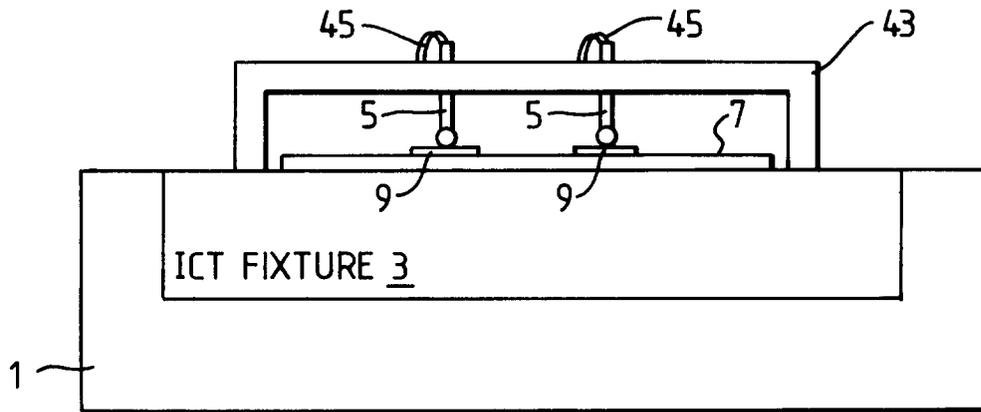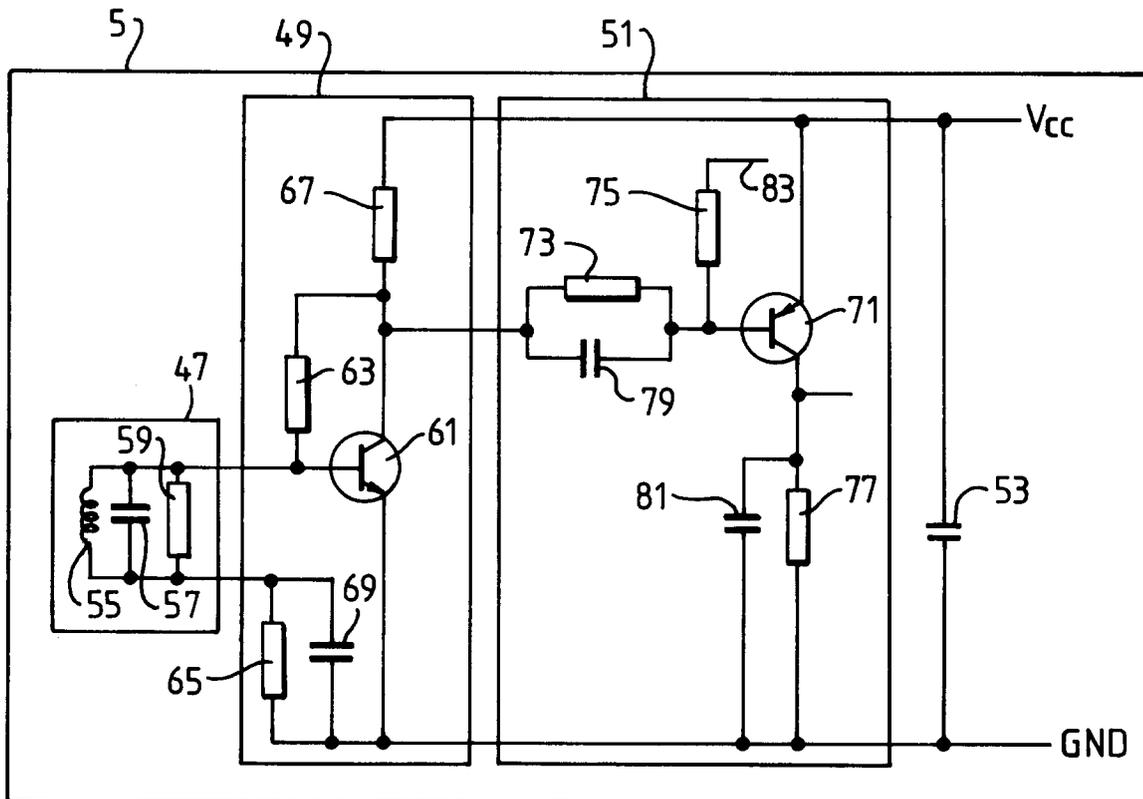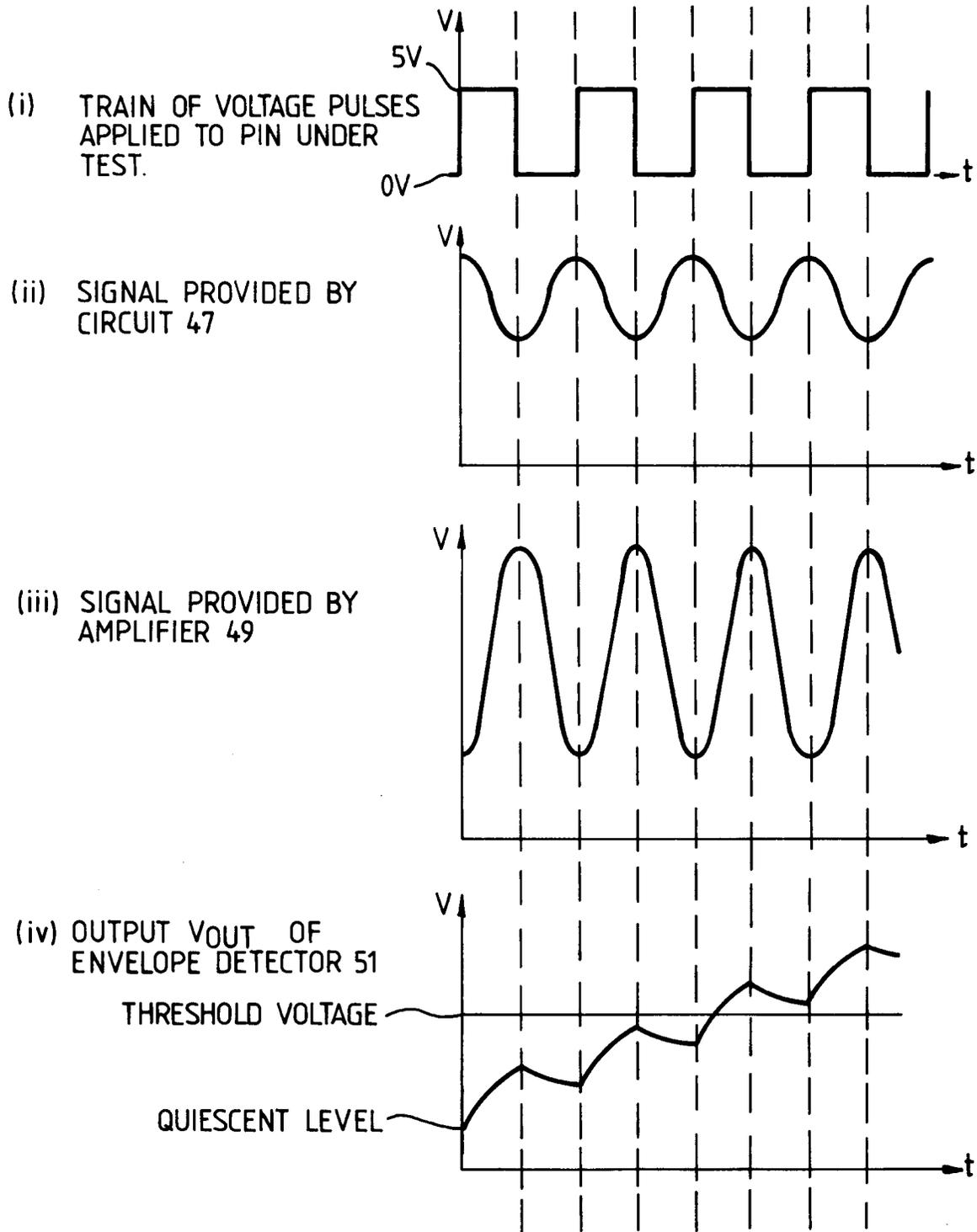
DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
Y	EP-A-0 177 210 (GEC AVIONICS) * page 4, line 35 - page 5, line 2 * * page 6, line 9 - line 18; figures 1-4,7 * ---	1-6,10, 13	G01R31/04 G01R31/315 G01R31/28
Y	EP-A-0 306 656 (SIEMENS) * column 1, line 53 - column 2, line 42; figures 1,2 * ---	1-6,10, 13	
A	DE-A-3 729 500 (SIEMENS) * column 1, line 50 - line 65; figure 1 * ---	4,7,8	
A	AU-A-1 725 976 (L M ERICSSON) * claim 1; figures 1,2 * -----	7,8	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

G01R

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	13 SEPTEMBER 1993	IWANSSON K.G.

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