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(54) **Optical semiconductor device and fabrication method therefor**

Optische Halbleitervorrichtung und ihr Herstellungsverfahren

Dispositif semi-conducteur optique et son procédé de fabrication

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EP 0 576 009 B1

Description

This invention relates to integrated circuits and, more specifically, to an optical semiconductor device having, integrally formed therein, a photo diode and a bipolar transistor.

A conventional optical semiconductor device is disclosed in, for example, JP-A 1-205564. With reference to Fig. 11, P-type semiconductor substrate 1 has epitaxially grown thereon a P-type epitaxial layer 2. An N-type epitaxial layer 3 is epitaxially grown on P-type epitaxial layer 2. A plurality of P⁺-type separating areas 4 separate N-type epitaxial layer 3, and contiguous upper portions of P-type epitaxial layer 2 into isolated islands. A first island forms a photo diode 9. A second island forms an NPN transistor 10.

Photo diode 9 includes an N⁺-type diffusion area 5 in its upper surface. An N⁺-type buried layer 6 spans a substantial part of the interface between epitaxial layers 2 and 3 in the island forming NPN transistor 10. The portion of N-type epitaxial layer 3 in NPN transistor 10 functions as the collector thereof. A P-type base area 7 is disposed in an upper surface of NPN transistor 10. An N⁺-type emitter area 8 is disposed in an upper surface of P-type base area 7. An N⁺-type collector contact area 12 is disposed in an upper surface of NPN transistor 10 outside P-type base area 7.

Photo diode 9 is biased to form a PN junction between P-type epitaxial layer 2 and N-type epitaxial layer 3. N⁺-type diffusion area 5 serves as a cathode of photo diode 9. P⁺-type separating area 4 serves as an anode of photo diode 9.

An accelerating electric field is formed in NPN transistor 10 by an auto-doped layer 11 in P-type epitaxial layer 2 which becomes autodoped by diffusion of P-type carriers from substrate 1 during epitaxial growth and heat treatment. Auto-doped layer 11 retards the movement of carriers originating below the depletion region.

To obtain a high speed response of photo diode 9, the depletion region is widened to restrain the movement of carriers occurring outside the depletion region. In the structure of the prior-art device in Fig. 11, auto-doped layer 11 overlaps P-type epitaxial layer 2. This overlap results in an increased concentration of impurities and an enlargement of the depletion region.

Epitaxial growth requires processing in a closed vessel into which gasses are fed to grow the desired layers, and to introduce the desired amount of impurities. During growth of P-type epitaxial layer 2, the closed vessel becomes contaminated with the P-type impurities. If an attempt is made to grow N-type epitaxial layer 3 in the same closed vessel used to grow P-type epitaxial layer 2, the P-type contaminants in the vessel enter N-type epitaxial layer 3 in such amounts that it is difficult or impossible to attain the desired properties in N-type epitaxial layer 3.

As a consequence of the contamination of the vessel by P-type impurities during epitaxial growth of P-type

epitaxial layer 2, the device must be removed physically from the vessel after P-type epitaxial layer 2 is formed, and placed in a clean vessel for growth of N-type epitaxial layer 3. The requirement for removing and reinstalling the workpiece during processing interferes with production since the same epitaxial growing device cannot be used for all steps to produce the prior art device.

An optical semiconductor device according to the preamble of claim 1 is disclosed in JP-A-5660054.

EP-A-0 501 316, which is a document under Article 54 (3) EPC, discloses a first epitaxial layer of high resistivity and a second epitaxial layer of comparatively low resistivity, wherein the layers have different conductivity types. Furthermore, an offset layer is provided in the substrate to offset the impurities of the substrate in this region.

Accordingly, it is an object of the present invention to provide an integrated photo diode and a transistor which overcomes the drawbacks of the prior art.

It is a further object of the invention to provide an integrated photo diode and a transistor in which epitaxial layers can be formed in the same vessel without requiring removal between the growing of layers.

It is a still further object of the invention to provide an integrated circuit having a photo diode and a transistor in which the photo diode cathode and the transistor emitter are formed of the same material in the same process steps.

It is another object of the invention to provide an integrated circuit having a photo diode and a transistor in which the activation of the photo diode is speeded up by the presence of a depletion layer.

These objects are achieved by an optical semiconductor device as defined in claims 1 and 3, respectively; claim 2 is related to a further development of the invention.

The above, and other objects, features and advantages of the present invention will become apparent from the following description read in conjunction with the accompanying drawings, in which like reference numerals designate the same elements.

Fig. 1 is a cross section of an optical semiconductor device useful for understanding the present invention.

Figs. 2(A), 2(B), 3(A), 3(B), 4, 5, 6, 7, 8, 9 are cross sections to which reference will be made in describing the steps of the process for producing the optical semiconductor device of Fig. 1.

Fig. 10 is a cross section of an optical semiconductor according to an embodiment of the present invention.

Fig. 11 is a cross section of an optical semiconductor device according to the prior art.

Referring to Fig. 1, a photo diode 21 and an NPN transistor 22 are integrated into a single device. A P-type single crystal silicon semiconductor substrate 23 has a lower concentration of impurities than is normally used in an ordinal bipolar integrated circuit, hereinafter IC, resulting in a resistivity of 40 to 60 ohm.cm. A conventional IC has a resistivity of about 2-4 ohm.cm in its

semiconductor substrate. A first epitaxial layer 24 is epitaxially grown by vapor deposition on substrate 23 to a thickness of 15-20 microns.

A second epitaxial layer 25 is also grown by vapor deposition on first epitaxial layer 24 to a thickness of 4-6 microns.

The resistivity of first epitaxial layer 24 is initially from 1000 to 1500 ohm.cm at the time of growth, but changes to 200 to 1500 ohm.cm. due to diffusion of impurities thereinto during subsequent heat treatment. First epitaxial layer 24 forms a central diffusion area. The resistivity of this layer in a conventional IC is 1.0-2.0 ohm.cm.

Portions of first and second epitaxial layers 24 and 25 are electrically isolated from each other by a vertical P⁺-type separating area 26 into a section for photo diode 21 and a section for NPN transistor 22. P⁺-type separating area 26 is formed of a first separating area 27, a second separating area 28 and a third separating area 29, overlapping each other, and thereby being electrically connected together (only the left-most separating area 26 is shown with areas 27, 28 and 29 separately identified). First separating area 27 is diffused above and below the interface between substrate 23 and first epitaxial layer 24. Second separating area 28 is diffused above and below the interface between first epitaxial layer 24 and second epitaxial layer 25. Third separating area 29 is diffused downward from a surface of second epitaxial layer 25. Separating areas 27, 28 and 29 overlap to become joined into single separating area 26 that divides epitaxial layers 24 and 25 into isolated island areas.

An N⁺-type diffusion area 31, which acts as cathode of photo diode 21, is formed on a portion of the surface of second epitaxial layer 25 of photo diode 21. The surface of second epitaxial layer 25 is covered by an oxidized membrane 32 which is etched to produce a plurality of contact holes, through which an aluminum cathode contact 33 contacts N⁺-type diffusion area 31. An aluminum anode contact 34 extends through a contact hole in oxidized membrane 32 to contact the upper surface of separating area 26 which serves as a low-resistivity anode for photo diode 21.

An N⁺-type buried layer 35 spans a substantial part of the interface between first and second epitaxial layers 24 and 25 of NPN transistor 22. An N-type collector layer 36 above N⁺-type buried layer 35 is doped with phosphorus. N-type collector layer 36 has a resistivity greater than the portion of second epitaxial layer 25 in which it is formed. A P-type base area 37 is formed in the surface of NPN transistor 22. An N⁺-type emitter area 38 is formed in the surface of P-type base area 37. An N⁺-type collector contact area 39 of NPN transistor 22 is formed on the surface of NPN transistor 22 outside base area 36.

An aluminum emitter contact 40 passes through oxidized membrane 32 to contact N⁺-type emitter area 38. An aluminum base contact 40' passes through oxidized

membrane 32 to contact base area 37. An aluminum collector contact 40" passes through oxidized membrane 32 to contact N⁺-type collector contact area 39. Aluminum electrodes 31, 34, 40, 40', and 40" are connected into a circuit (not shown) by conventional aluminum wiring (not shown).

The resulting device includes photo diode 21 capable of functioning as an optical signal input unit integrated with NPN transistor 22 which, together with the other circuit elements, can be used as part of a signal processing circuit.

An IC having the foregoing structure can be produced by the following process:

Referring to Fig. 2(A), P-type silicon semiconductor substrate 23 is doped to a resistivity of 40 to 60 ohm.cm.

Referring to Fig. 2(B), P-type silicon semiconductor substrate 23 is heated in an oxygen atmosphere to develop an insulating oxide membrane on its upper surface. The oxide membrane is coated with a negative photo resist membrane. The photo resist membrane is baked, exposed and chemically etched to expose a corresponding pattern in the upper surface of substrate 23. Boron is ion-implanted through the pattern to form three spaced-apart first separating areas 27.

Referring now to Fig. 3(A), the oxide membrane is removed, and substrate 23 is washed. Substrate 23 is then placed in an epitaxial growing device (not shown) and heated by a lamp or a high frequency electromagnetic wave to a temperature of approximately 1,140°C. SiH₂Cl₂ gas is introduced into a reaction tube, thus growing first epitaxial layer 24 of intrinsic material to a thickness of 15-20 microns. A small amount of autodoping of first epitaxial layer 24 takes place during growth by diffusion of boron P-type impurities from substrate 23, first separating area 27, and the rear side of wafer to yield a first epitaxial layer 24 having a relatively high resistivity of 200-1500 ohm.cm.

Referring to Fig. 3(B), the substrate is heated in an oxygen atmosphere to produce an insulating oxide membrane. The oxide membrane is coated with a negative photo resist membrane. The photo resist membrane is baked, exposed and chemically etched to expose a corresponding pattern in the upper surface of first epitaxial layer 24 to diffuse a portion of the antimony into the surface of first epitaxial layer 24 to produce a precursor of N⁺-type buried layer 35. At this time, first separating area 27 is also diffused upward and downward.

Referring to Fig. 4, a further resist membrane is coated over oxide membrane, dried, exposed and etched to produce a selective mask, thereby exposing portions of the surface of first epitaxial layer 24.

Boron is ion-implanted to form a precursor of three second separating areas 28 of separating area 26. The resist membrane is removed, and the device is heat treated to diffuse second separating areas 28 from 6 to 8 microns downward and to diffuse first separating area 27 from 8 to 10 microns upward until they overlap to become a single entity.

Referring to Fig. 5, oxide layer is removed, and second epitaxial layer 25 is epitaxially grown to a thickness of 4 to 6 μm (microns) atop the surface of first epitaxial layer 24. During this process step, second separating areas 28, and N⁺-type buried layer 35 diffuse upward partway into newly-applied second epitaxial layer 25.

Referring to Fig. 6, the device is heated in an oxygen containing atmosphere to produce a further oxide membrane on the surface of second epitaxial layer 25. The oxide membrane is coated with a negative photo resist membrane. The photo resist membrane is baked, exposed and chemically etched to expose a corresponding pattern in the upper surface of second epitaxial layer 25. Phosphorus is ion-implanted through the resist pattern to a concentration of 10^{12} atoms per cm^2 at about 80 KeV to form a precursor of N-type collector layer 36.

Referring to Fig. 7, the device is heat treated at about 1100-1200° C for 2 to 3 hours to diffuse the phosphorus forming N-type collector layer 36 about 3 to 5 microns downward and N⁺-type buried layer 35 diffuses upward until these two layer are joined. First separating area 27 and second separating area 28 are also diffused upward and downward during this heat treatment.

Referring to Fig. 8, the device is heated in an oxygen atmosphere to produce an insulating oxide membrane, thus coated with a negative photo resist membrane. The photo resist membrane is baked, exposed and chemically etched to expose a corresponding pattern in the upper surface of second epitaxial layer 25. Boron is ion-implanted through the pattern to form precursors of third separating areas 29. Further heat treatment diffuses the boron downward to a thickness of 2-3 microns to form third separating areas 29, and also diffuses second separating areas 28 upward until these areas join. At this point, the three separating areas 27, 28 and 29 overlap to form single separating areas 26 that divide epitaxial layers 24 and 25 into isolated island areas.

Referring to Fig. 9, a resist pattern is processed to form a mask for the implantation of boron to produce P-type base area 37. Next, phosphorus diffuses to produce N⁺-type diffusion area 31, N⁺-type emitter area 38 and N⁺-type collector contact area 39 in the surface of the device.

Returning now to Fig. 1, aluminum electrodes 33, 34, 40, 40', and 40'' pass through openings in oxidized membrane 32 to provide external contact to N⁺-type diffusion area 31, the center P⁺-type separating area 26, N⁺-type emitter area 38, P-type base area 37 and N⁺-type collector contact area 39, respectively.

Photo diode 21 of the IC having the foregoing structure has the following features:

Cathode contact 33 and anode contact 34 are reverse biased at V_{cc} (+5V) and GND, respectively. This bias produces a depletion layer extending from the interface between P-type second epitaxial layer 25 and N⁺-type diffusion area 31 into epitaxial layers 24 and 25.

Epitaxial layers 24 and 25 have high resistivity.

A light with a frequency of 800 nm passes into photo diode 21 to a depth of more than 20 μm (microns). The light generates carriers inside photo diode 21 to produce a photocurrent therein.

The carriers are generated inside the depletion layer and a corresponding number of carriers are generated outside depletion layer. The carriers inside the depletion layer move very quickly because of the low resistivity in this region. The carriers outside the depletion layer move slowly because of the higher resistivity in this region.

In this invention, since the depletion layer extends almost completely through both epitaxial layers 24 and 25, almost all of the carriers are generated within the depletion layer so that the response of photo diode 21 is very fast.

Moreover, N⁺-type diffusion area 31, forming the cathode of photo diode 21, is very thin, being limited in depth to from about 0.3 to 1.0 μm (microns). Such a thin emitter is not capable of generating a large number of carriers. Because of the high concentration of impurities in first and second epitaxial layers 24 and 25, the carriers generated therein disappear quickly or move rapidly into N⁺-type diffusion area 31. As a result, little delay current is produced by carrier diffusion.

The deep diffusion area formed by the center P⁺-type separating area 26 provides a very low-resistance anode electrode.

NPN transistor 22 of the IC having the foregoing structure has the following features:

The concentration of impurities in N-type collector layer 36 of second epitaxial layer 25 is suitable to provide transistor action.

The heat treated period required to diffuse N-type collector area 36 downward into contact with N⁺-type buried layer 35 is limited because of the two epitaxial layers. Only a portion of second epitaxial layer 25 must be converted to an N-type area.

Epitaxial layers 24 and 25 are very lightly P-doped, whereby they have relatively high resistivity. The P doping of epitaxial layers 24 and 25 is so light that a processing vessel can be used for subsequent N-type epitaxial growth without pollution of the vessel by the P-type impurities of epitaxial layers 24 and 25. Also, the light P doping permits easy control of resistivity.

The prior art device of Fig. 11 has the problem that boron diffuses upward during heat treatment from the heavily P-doped substrate 1 to the epitaxial layer 2 above it, so as to produce auto-doped layer 11. Auto-doped layer 11 prevents the extension of depletion layer to substrate 1.

Referring again to Fig. 1, the low P doping of substrate 23, to about 40 to 60 ohm.cm, and the even lower doping of first epitaxial layer 24, to about 1000 to 1500 ohm.cm (with a final resistivity of 200 to 1500 ohm.cm) decreases the problem of an autodoped layer extending into first epitaxial layer 24. The very low P doping of sub-

strate 23, and the relatively low P doping of first epitaxial layer reduces the autodoping layer and permits the depletion layer to extend substantially the entire distance to the surface of substrate 23.

The high resistivity of substrate 23 and the decrease in the auto-doped layer would cause the resistance at anode contact 34 to increase if the design of the prior art in Fig. 11 were used. However, in the embodiment of the present invention in Fig. 1, the increase in resistance at anode contact 34 is prevented by extending P+-type separating area 26 all the way down into substrate 23.

Referring now to Fig. 10, an embodiment of the invention includes an offsetting layer 41 of N-type impurities ion-implanted into the surface of substrate 23 of photo diode 21 to offset the concentration of impurities in the surface of substrate 23. Offsetting layer 41 permits the depletion layer to extend all the way to the surface of substrate 23. The N-type impurities forming offsetting layer 41 may be ion-implanted into substrate 23 only below the island forming photo diode 21. However, for processing simplicity, it is acceptable for the N-type impurities to be implanted over the entire surface of substrate 23, including below islands for both photo diode 21 and NPN transistor 22. The diffusion of N-type impurities does not exceed the depth to which first separating area 27 extends. Thus, the inclusion of offsetting layer 41 does not increase the resistance at anode electrode 34.

Phosphorus is ion-implanted to a concentration of 1 to 5×10^{11} atoms per cm^2 to form the precursor of offsetting layer 41. After implantation, the phosphorus is diffused by heat treatment to yield a resistivity varying from 40-60 ohm.cm to more than 200 ohm.cm. Offsetting layer 41 is diffused to a depth of 2-10 microns. First separating area 27 extends downward to a depth of 7 to 15 microns in substrate 23. Separating area 27 extends below offsetting layer 41, and thus blocks sideways migration of carriers from offsetting layer 41. The N-type impurities in offsetting layer 41 diffuse upward into the neighboring region of first epitaxial layer 24 where they offset P-type carriers auto-doped upward into first epitaxial layer 24 from substrate 23.

Claims

1. An optical semiconductor device having a photo diode (21) and a transistor (22) comprising:

a semiconductor substrate (23) of a first conductivity type;
a first epitaxial layer (24) of intrinsic semiconductor material grown on a surface of said semiconductor substrate (23);
a second epitaxial layer (25) of intrinsic semiconductor material grown on the surface of said first epitaxial layer (24);

a separating area (26) of said first conductivity type dividing said first and second epitaxial layers into at least first and second island areas;
a diffusion area (31) in the surface of said second epitaxial layer (25) of said first island area;
a buried layer (35) of said second conductivity type at the interface between said first and second epitaxial layers in said second island area;
a collector layer (36) of said second conductivity type in said second island area extending from the surface of said second epitaxial layer to said buried layer (35);
a base area (37) of said first conductivity type in the surface of said collector layer in said second island area;
and an emitter area (38) of said second conductivity type in the surface of said base area;

characterized in that

said semiconductor substrate (23) has a resistivity of 40 to 60 ohm · cm;
said first and second epitaxial layers (24,25) have resistivities of more than 200 ohm · cm;
said collector layer (36) has a resistivity of less than both said resistivities of said first and second epitaxial layers;
said diffusion area is of said second conductivity type;
and that an offsetting layer (41) containing impurities of said second conductivity type to offset the concentration of impurities in the surface of said substrate is provided in the surface of said semiconductor substrate (23) at least below said first island.

2. An optical semiconductor device according to claim 1, wherein said separating area (26) extends into said semiconductor substrate (23), exceeding the distance at which said offsetting layer extends into said semiconductor substrate (23).
3. An optical semiconductor device having a photo diode (21) and a transistor (22) comprising:

a semiconductor substrate (23) of a first conductivity type;
a first epitaxial layer (24) grown on a surface of said semiconductor substrate (23);
a second epitaxial layer (25) grown on the surface of said first epitaxial layer (24);
a separating area (26) of said first conductivity type dividing said first and second epitaxial layers into at least first and second island areas;
a diffusion area (31) in the surface of said second epitaxial layer (25) of said first island area;
a buried layer (35) of said second conductivity type at the interface between said first and sec-

ond epitaxial layers in said second island area;
 a collector layer (36) of said second conductivity type in said second island area extending from the surface of said second epitaxial layer to said buried layer (35);
 a base area (37) of said first conductivity type in the surface of said collector layer in said second island area;
 and an emitter area (38) of said second conductivity type in the surface of said base area;

characterized in that

said first and second epitaxial layers are of said first conductivity type;
 said semiconductor substrate (23) has a resistivity of 40 to 60 ohm · cm;
 said first and second epitaxial layers (24,25) have resistivities of more than 200 ohm · cm;
 said collector layer (36) has a resistivity of less than both said resistivities of said first and second epitaxial layers;
 said diffusion area is of said second conductivity type;
 and that an offsetting layer (41) containing impurities of said second conductivity type to offset the concentration of impurities in the surface of said substrate is provided in the surface of said semiconductor substrate (23) at least below said first island.

Patentansprüche

1. Optische Halbleitervorrichtung mit einer Fotodiode (21) und einem Transistor (22) mit:

einem Halbleitersubstrat (23) eines ersten Leitfähigkeitstyps,
 einer ersten Epitaxieschicht (24) eines intrinsischen Halbleitermaterials, das auf der Oberfläche des Halbleitersubstrats (23) aufgewachsen ist,
 einer zweiten Epitaxieschicht (25) aus intrinsischem Halbleitermaterial, das auf der Oberfläche der ersten Epitaxieschicht (24) aufgewachsen ist,
 einem Trennbereich (26) des ersten Leitfähigkeitstyps, der die erste und die zweite Epitaxieschicht in zumindest erste und zweite Inselbereiche aufteilt,
 einem Diffusionsbereich (31) in der Oberfläche der zweiten Epitaxieschicht (25) des ersten Inselbereichs,
 einer Versenkschicht (35) des zweiten Leitfähigkeitstyps an der Schnittfläche zwischen der ersten und der zweiten Epitaxieschicht in dem zweiten Inselbereich,

einer Kollektorschicht (36) des zweiten Leitfähigkeitstyps in dem zweiten Inselbereich, die sich von der Fläche der zweiten Epitaxieschicht zur Versenkschicht (35) erstreckt,
 einem Basisbereich (37) des ersten Leitfähigkeitstyps in der Oberfläche der Kollektorschicht in dem zweiten Inselbereich,
 und einem Emittierbereich (38) des zweiten Leitfähigkeitstyps in der Fläche des Basisbereichs,

dadurch **gekennzeichnet**, daß

das Halbleitersubstrat (23) einen spezifischen Widerstand von 40 bis 60 Ω cm aufweist, die erste und die zweite Epitaxieschicht (24, 25) spezifische Widerstände von mehr als 200 Ω cm aufweisen,
 die Kollektorschicht (36) einen spezifischen Widerstand von weniger als sowohl die erste als auch die zweite Epitaxieschicht aufweist, der Diffusionsbereich von dem zweiten Leitfähigkeitstyp ist,
 und daß eine Offsetschicht (41), die Störstoffe des zweiten Leitfähigkeitstyps enthält, um die Konzentration der Störstoffe in der Oberfläche des Substrates auszugleichen, in der Oberfläche des Halbleitersubstrats (23) zumindest unterhalb der ersten Insel vorgesehen ist.

2. Optische Halbleitervorrichtung nach Anspruch 1, wobei der Trennbereich (26) sich in das Halbleitersubstrat (23) erstreckt und den Abstand überschreitet, in dem sich die Offsetschicht in das Halbleitersubstrat (23) erstreckt.

3. Optische Halbleitervorrichtung mit einer Fotodiode (21) und einem Transistor (22) mit:

einem Halbleitersubstrat (23) eines ersten Leitfähigkeitstyps,
 einer ersten Epitaxieschicht (24), die auf der Oberfläche des Halbleitersubstrats (23) aufgewachsen ist,
 einer zweiten Epitaxieschicht (25), die auf der Oberfläche der ersten Epitaxieschicht (24) aufgewachsen ist,
 einem Trennbereich (26) des ersten Leitfähigkeitstyps, der die erste und die zweite Epitaxieschicht in zumindest einen ersten und einen zweiten Inselbereich aufteilt,
 einem Diffusionsbereich (31) in der Oberfläche der zweiten Epitaxieschicht (25) des ersten Inselbereichs,
 einer Versenkschicht (35) des zweiten Leitfähigkeitstyps an der Schnittfläche zwischen der ersten und der zweiten Epitaxieschicht in dem zweiten Inselbereich,

einer Kollektorschicht (36) des zweiten Leitfähigkeitstyps in dem zweiten Inselbereich, die sich von der Oberfläche der zweiten Epitaxieschicht zur Versenkschicht (35) erstreckt, einem Basisbereich (37) des ersten Leitfähigkeitstyps in der Oberfläche der Kollektorschicht in dem zweiten Inselbereich, und einem Emitterbereich (38) des zweiten Leitfähigkeitstyps in der Oberfläche des Basisbereichs,

dadurch **gekennzeichnet**, daß

die erste und die zweite Epitaxieschicht vom ersten Leitfähigkeitstyp sind,
das Halbleitersubstrat (23) einen spezifischen Widerstand von 40 bis 60 Ω cm aufweist,
die erste und die zweite Epitaxieschicht (24, 25) spezifische Widerstände von mehr als 200 Ω cm aufweisen,
die Kollektorschicht (36) einen spezifischen Widerstand von weniger als beide spezifischen Widerstände der ersten und der zweiten epitaktischen Schicht aufweist,
der Diffusionsbereich von dem zweiten Leitfähigkeitstyp ist und daß eine Offsetschicht (41), die Störstoffe des zweiten Leitfähigkeitstyps enthält, um die Konzentration von Störstoffen in der Oberfläche des Substrates auszugleichen, in der Oberfläche des Halbleitersubstrats (23) zumindest unterhalb der ersten Insel vorgesehen ist.

Revendications

1. Dispositif semi-conducteur optique comportant une photodiode (21) et un transistor (22) comprenant :

un substrat semi-conducteur (23) d'un premier type de conductivité ;
une première couche épitaxiale (24) de matériau semi-conducteur intrinsèque développée sur une surface dudit substrat semi-conducteur (23) ;
une seconde couche épitaxiale (25) de matériau semi-conducteur intrinsèque développée sur la surface de ladite première couche épitaxiale (24) ;
une zone de séparation (26) dudit premier type de conductivité divisant lesdites première et seconde couches épitaxiales au moins en première et seconde zones d'îlots ;
une zone de diffusion (31) dans la surface de ladite seconde couche épitaxiale (25) de ladite première zone d'îlot ;
une couche enterrée (35) dudit second type de conductivité à l'interface entre lesdites première

re et seconde couches épitaxiales dans ladite seconde zone d'îlot ;
une couche collectrice (36) dudit second type de conductivité dans ladite seconde zone d'îlot s'étendant de la surface de ladite seconde couche épitaxiale à ladite couche enterrée (35) ;
une zone de base (37) dudit premier type de conductivité dans la surface de ladite couche collectrice dans ladite seconde zone d'îlot ; et
une zone d'émetteur (38) dudit second type de conductivité dans la surface de ladite zone de base ;

caractérisé en ce que

ledit substrat semi-conducteur (23) a une résistivité de 40 à 60 ohms.cm ;
lesdites première et seconde couches épitaxiales (24, 25) ont des résistivités supérieures à 200 ohms.cm ;
ladite couche collectrice (36) a une résistivité inférieure auxdites deux résistivités desdites première et seconde couches épitaxiales ;
ladite zone de diffusion est dudit second type de conductivité ;
et en ce qu'une couche de décalage (41) contenant des impuretés dudit second type de conductivité pour décaler la concentration des impuretés dans la surface dudit substrat est prévue dans la surface dudit substrat semi-conducteur (23) au moins en dessous dudit premier îlot.

2. Dispositif semi-conducteur optique selon la revendication 1, dans lequel ladite zone de séparation (26) s'étend dans ledit substrat semi-conducteur (23), dépassant la distance à laquelle ladite couche de décalage s'étend dans ledit substrat semi-conducteur (23).

3. Dispositif semi-conducteur optique comportant une photodiode (21) et un transistor (22) comprenant :

un substrat semi-conducteur (23) d'un premier type de conductivité ;
une première couche épitaxiale (24) développée sur une surface dudit substrat semi-conducteur (23) ;
une seconde couche épitaxiale (25) développée sur la surface de ladite première couche épitaxiale (24) ;
une zone de séparation (26) dudit premier type de conductivité divisant lesdites première et seconde couches épitaxiales au moins en première et seconde zones d'îlots ;
une zone de diffusion (31) dans la surface de ladite seconde couche épitaxiale (25) de ladite première zone d'îlot ;

une couche enterrée (35) dudit second type de conductivité à l'interface entre lesdites première et seconde couches épitaxiales dans ladite seconde zone d'îlot ;

une couche collectrice (36) dudit second type de conductivité dans ladite seconde zone d'îlot s'étendant de la surface de ladite seconde couche épitaxiale à ladite couche enterrée (35) ;
une zone de base (37) dudit premier type de conductivité dans la surface de ladite couche collectrice dans ladite seconde zone d'îlot ;
et une zone d'émetteur (38) dudit second type de conductivité dans la surface de ladite zone de base ;

15

caractérisé en ce que

lesdites première et seconde couches épitaxiales sont dudit premier type de conductivité ;

ledit substrat semi-conducteur (23) a une résistivité de 10 à 60 ohms.cm ;

20

lesdites première et seconde couches épitaxiales (24, 25) ont des résistivités supérieures à 200 ohms.cm ;

ladite couche collectrice (36) a une résistivité inférieure auxdites deux résistivités desdites première et seconde couches épitaxiales ;
ladite zone de diffusion est dudit second type de conductivité ;

25

et en ce qu'une couche de décalage (41) contenant des impuretés dudit second type de conductivité pour décaler la concentration des impuretés dans la surface dudit substrat est prévue dans la surface dudit substrat semi-conducteur (23) au moins en dessous dudit premier îlot.

30

35

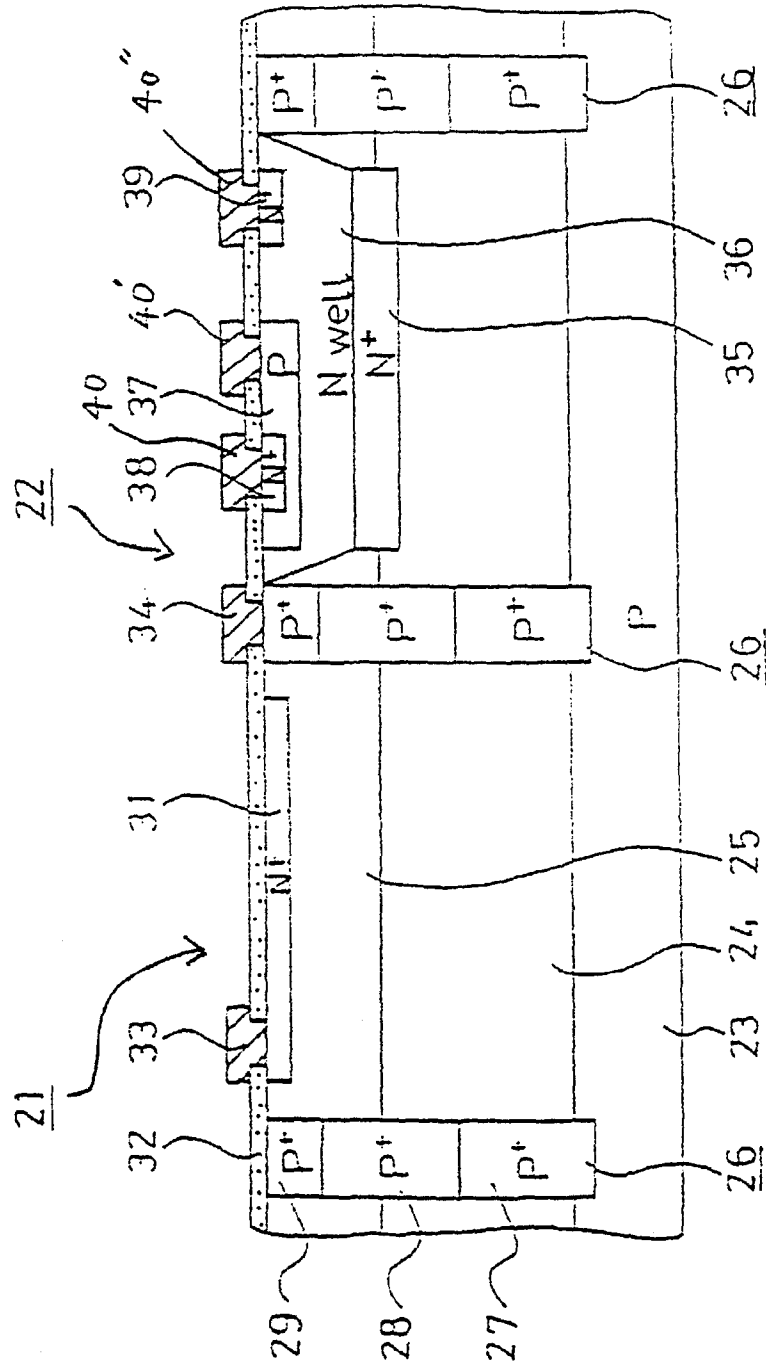
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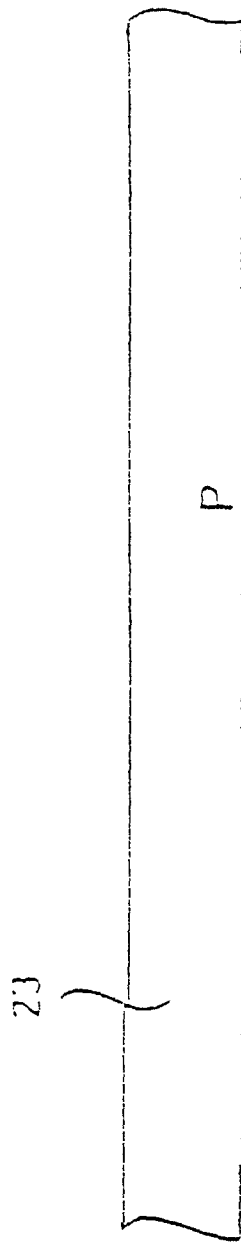


Fig. 2(a)

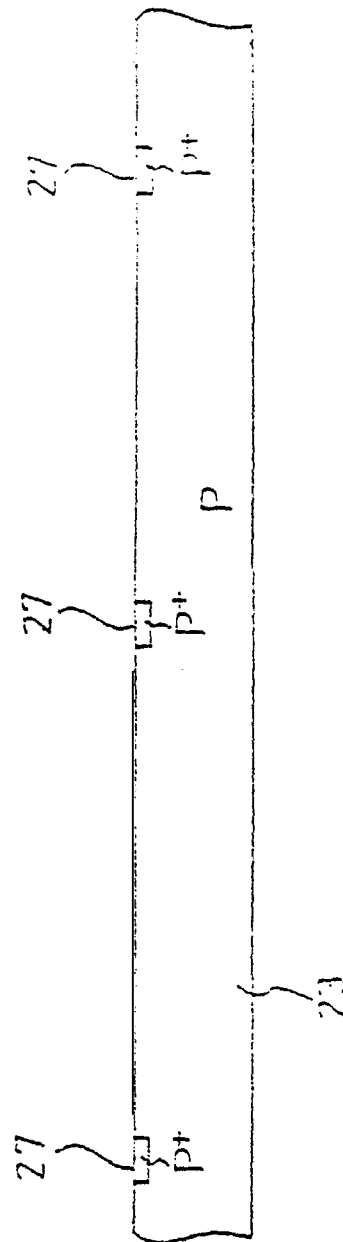


Fig. 2(b)

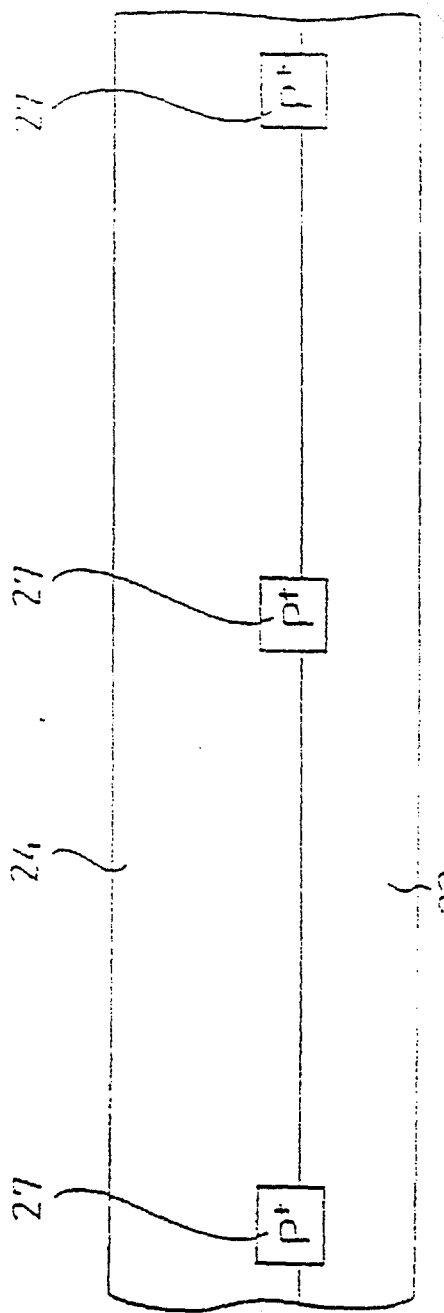


Fig. 3(a)

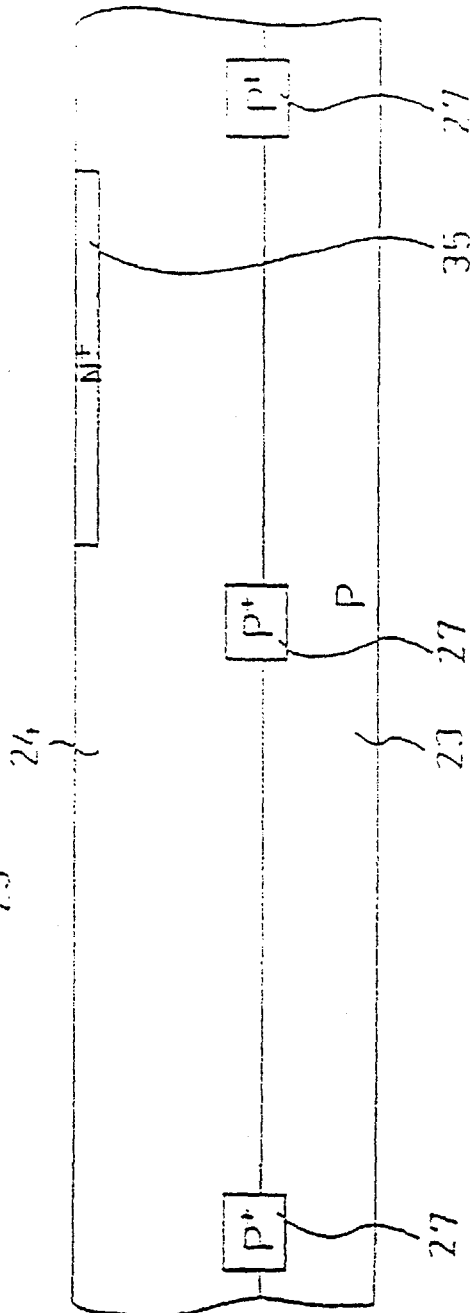


Fig. 3(b)

Fig. 4

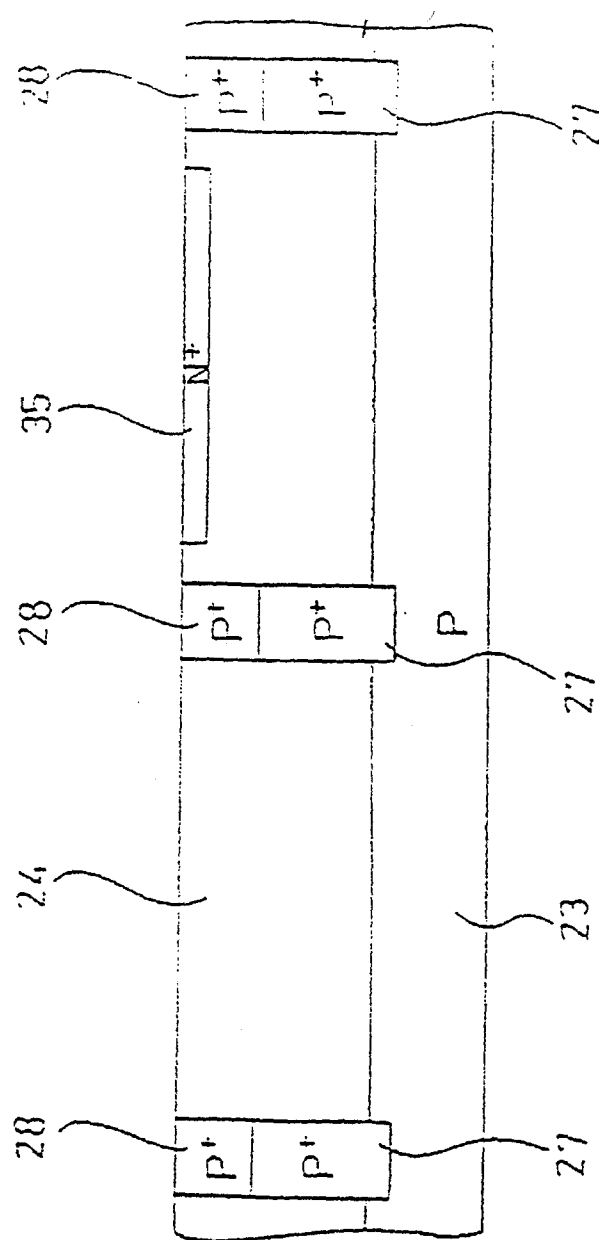


Fig. 5

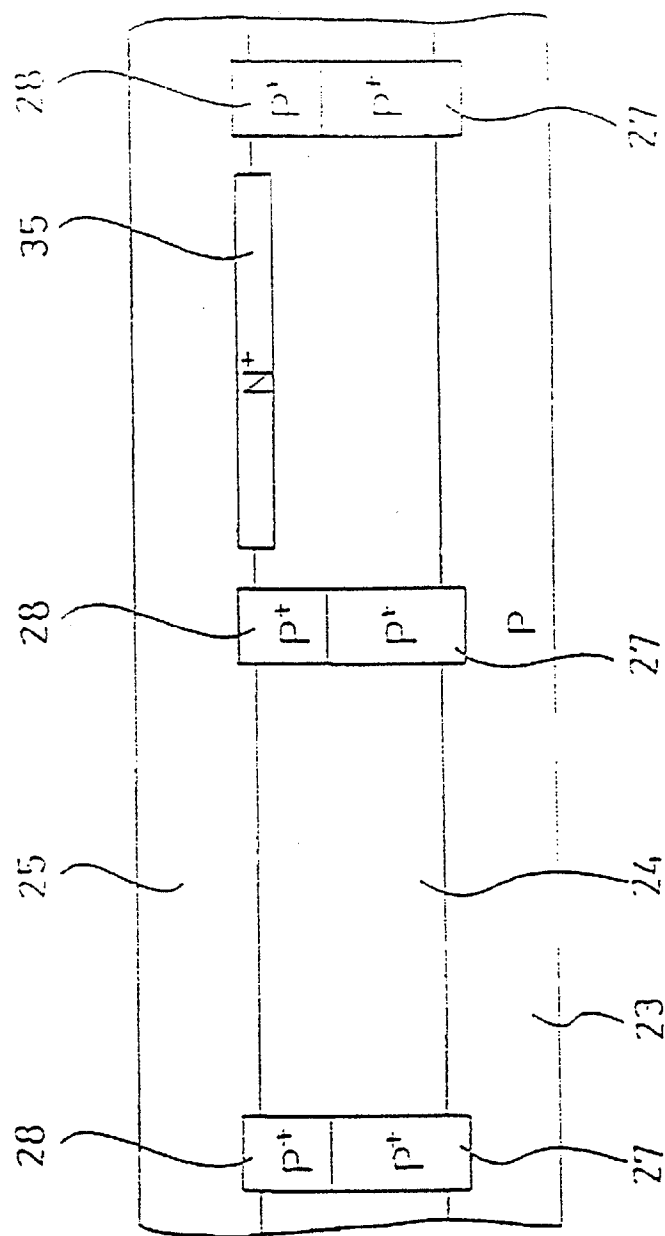


Fig. 6

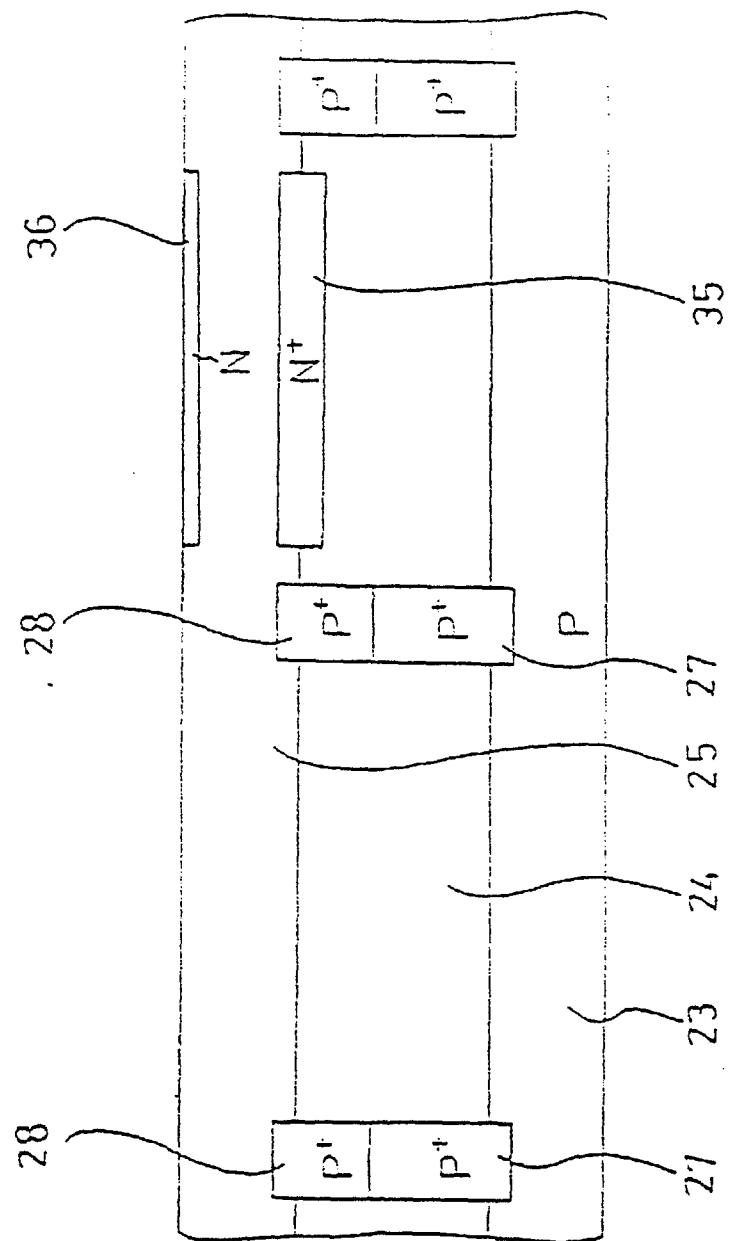


Fig. 7

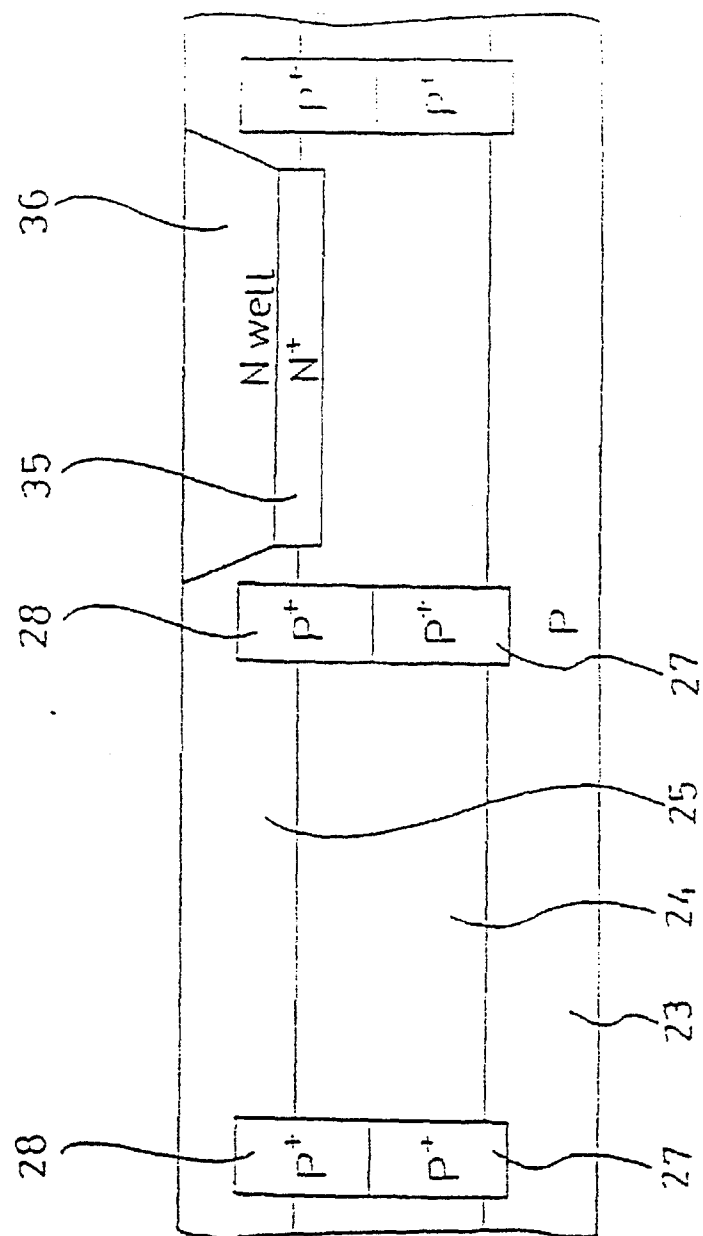


Fig. 8

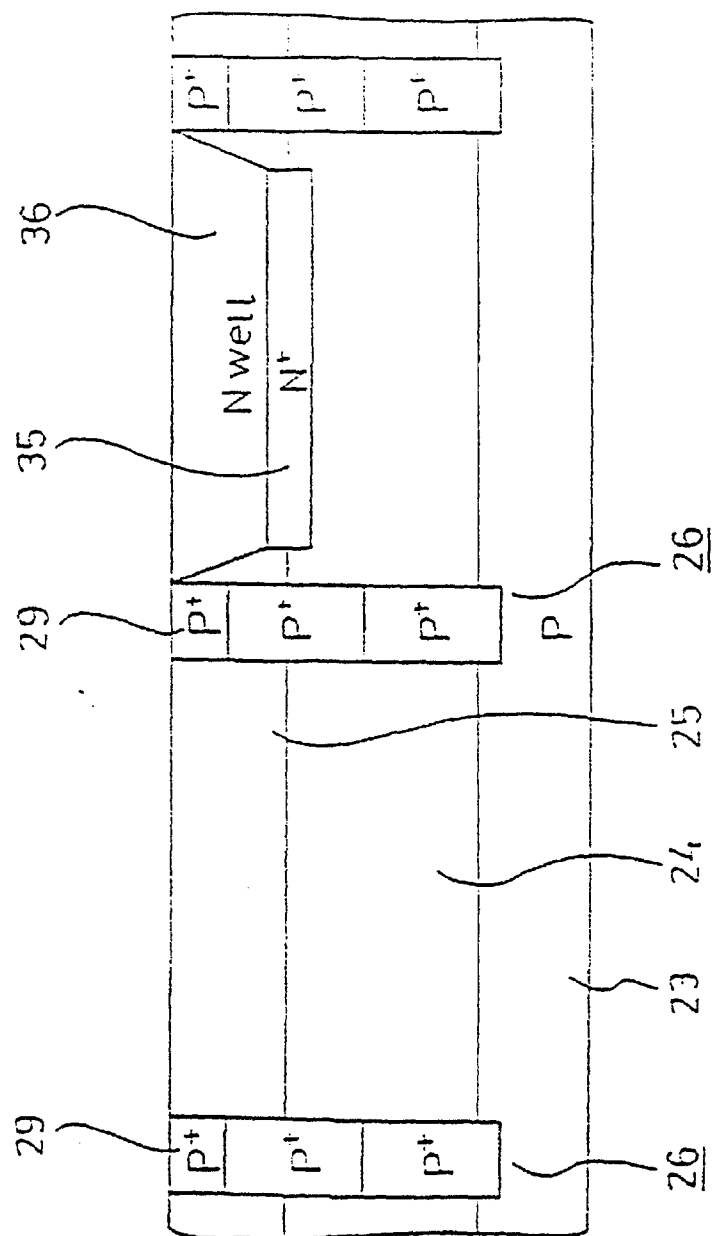


Fig. 9

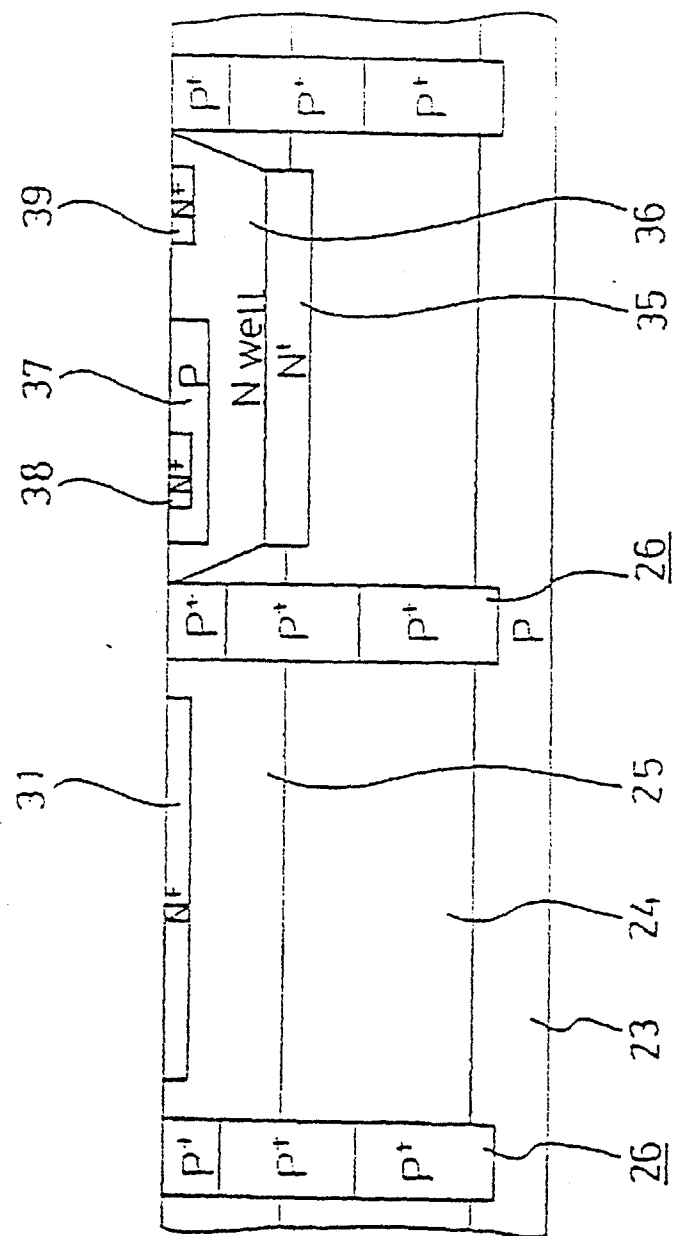


Fig. 10

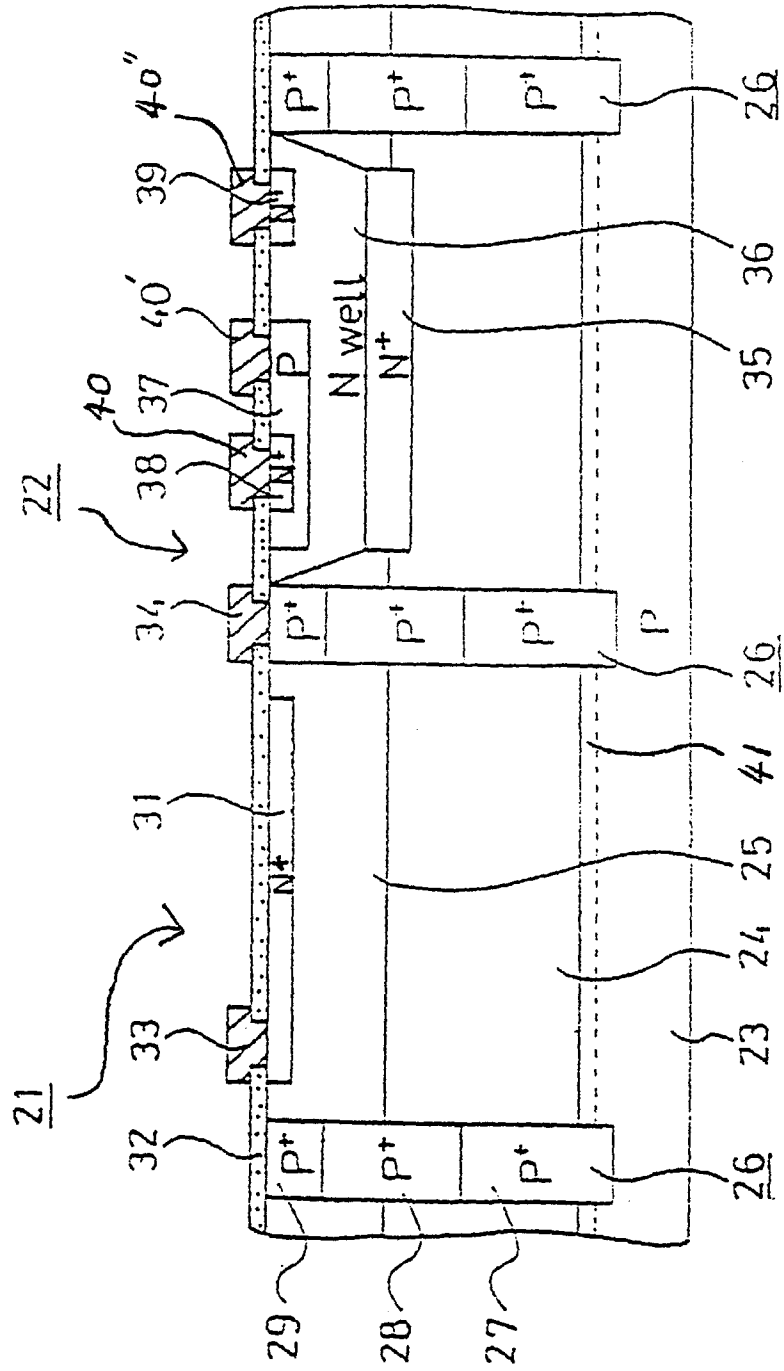


Fig. 11 **PRIOR**
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