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(54) Current generating circuit.

(57) The current generating circuit is independent from power supply fluctuations and temperature variations. It includes the series connection of a main current source MCR which generates a reference current Iref from a reference voltage Vref generated by a voltage source VRS, and a current mirror CM. VRS uses Iref to generate Vref and consequently an auxiliary current source ACS is needed to start-up the current generating circuit. ACS includes a current source CS and a regulating stage RS to disable CS after start-up.

RS includes a branch M2-R2 wherein a current equal to Iref flows and disables CS based on the value of Iref.

CM realizes the distribution of Iref over an integrated circuit (not shown) and to VRS.

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The present invention relates to a current generating circuit which includes a main current source able to generate a constant steady-state reference current from a steady-state reference voltage provided by a voltage source.

Such a circuit is well known in the art, a current mirror circuit often being used to, for instance, provide the steady-state reference current to different stages of operational amplifiers of analog integrated circuits.

The steady-state reference voltage used in the current generating circuit has to be independent from fluctuations of the power supply and of temperature and to this end the voltage source generating such a steady-state reference voltage generally uses a stable, supply and temperature independent current source. However, this has a negative impact on the lay-out complexity of an integrated circuit in which that current generating circuit is used and on the necessary chip area when the above current-source has to be incorporated on the integrated circuit.

The above mentioned voltage source is for instance a band gap reference source, different embodiments of which are described in chapter A4.3.2 of the book "Analysis and design of analog integrated circuits" by Paul R. Gray and Robert G. Meyer and edited by John Wiley & Sons in 1977.

An object of the invention is to provide a current generating circuit of the above type, but which is less complex and needs less area to be integrated on chip

This object is achieved due to the fact that it further includes an auxiliary current source and an output circuit to which said auxiliary and main current sources, at start-up, supply respective decreasing and increasing currents and which supplies current to said voltage source, said voltage source accordingly providing an increasing voltage at said start-up and said increasing voltage and current reaching said steady-state reference voltage and current respectively.

The stable and, supply and temperature, independent current needed by the voltage source, is thus provided by the current generating circuit. As a result the circuit needs the auxiliary current source to start-up. The current provided by this source has however not to be very accurate or supply and temperature independent and is thus relatively simple to realize, provided of course that its working is disabled after start-up, at the latest when the nominal working point of the current generating circuit is reached, i.e. the point where it generates the steady-state reference current.

Characteristic features of the current generating circuit according to the invention are that said output circuit is connected in series with the parallel connection of said main current source and said auxiliary current source which includes a current source generating said decreasing current at the junction point of said output circuit and said main current source, thereby realizing an output of said auxiliary current source, and a regulating stage also connected to said junction point to control said current source in such a way that it is disabled at the latest when said steady-state reference current is reached by said current generating circuit, that said regulating stage includes a branch in which the current generated by said current generating circuit is mirrored, that said regulating stage includes in said branch, between a first and a second power terminal, a cascade connection of a PMOS transistor and a resistor, the gate of said PMOS transistor being connected to said output of said auxiliary current source and the interconnection of said PMOS transistor and said resistor being connected to the base of a first npn transistor the emitter of which is connected to said second power terminal and that said current source includes a second npn transistor the collector of which is connected to said output of said auxiliary current source and the emitter of which is coupled to said second power terminal via a second resistor, and a cascade connection between said first and said second power terminal of a third and a fourth resistor, the junction point of which is connected to the base of said second npn transistor and the collector of said first npn transistor.

In the auxiliary current source realized in this way the regulating circuit controls the current source to generate the decreasing current and disables the source when a predetermined value is exceeded i.e. at the latest when the steady-state reference current is generated by the current generating circuit. It does so based on the current flowing in the mentioned branch.

Another characteristic of the current generating circuit according to the invention is that said main current source includes the cascade connection of a grounded resistor and an npn transistor at the base of which a base voltage derived from said increasing and said steady-state reference voltage is applied at start-up and nominal working respectively and that said base voltage is applied to the base of said npn transistor via a pnp transistor the emitter of which is connected to the base of said npn transistor, said increasing and steady-state reference voltage being applied to the base of said pnp transistor at start-up and nominal working respectively, thereby making the current generating circuit temperature independent.

The above mentioned and other objects and features of the invention will become more apparent and the invention itself will be best understood by referring to the following description of an embodiment taken in conjunction with the accompany-

ing drawing which represents a current generating circuit according to the invention.

The current generating circuit shown in the figure has two voltage supply terminals V1 and V2 which provide a negative and a positive voltage respectively and a ground terminal. It includes a current mirror circuitry CM which is connected between V1 and V2 in series, on the one hand with a main current source MCR, and on the other hand with an auxiliary current source ACS, the common junction point of CM, MCR and ACS being indicated by JP. The current mirror circuit CM is further connected to a reference voltage circuit VRS whose output controls the main current reference source MCR.

The current mirror circuitry includes a diode connected PMOS transistor M1 and a plurality of PMOS transistors such as M3, M4, M5 whose source-to-gate paths are connected in parallel between V1 and JP.

The main current source MCR generates at nominal working a steady-state reference current Iref which is mirrored in transistors M1, M3, M4 and M5 of CM. M3 and M4 feed a not shown integrated circuit, whereas M5 supplies IREF to the voltage source VRS which in response generates a steady-state reference voltage Vref at nominal working. Voltage reference sources such as VRS which derive a steady-state reference voltage from a steady-state current are well known in the art and VRS is therefore not described in detail. Such a voltage reference source is for instance a band gap reference source as described in the above mentioned book.

MCR includes between V1 and V2 the series connection of a resistor R6 and the emitter-to-collector path of a pnp transistor Q1 whose base is controlled by the output Vref of VRS. The emitter of Q1 is connected to the base of an npn transistor Q2. A diode D1, the collector-to-emitter path of transistor Q2 and a resistor R1 are connected between JP and ground.

ACS has a current source part CS and a regulating stage part RS. RS includes a PMOS transistor M2 the source-to-drain path of which is connected in series with a resistor R2 between V1 and V2 and the drain of which controls the base of an npn transistor Q3. In CS the collector-to-emitter path of Q3 shunts resistor R4 of a resistive voltage divider R3, R4 comprising resistors R3 and R4 which are connected in series between V1 and V2. The tapping point of R3, R4 is connected to the base of an npn transistor Q4 whose collector-to-emitter path is connected in series with resistor R5 between JP and V2.

Typical values for the elements of the current biasing circuit are R1 = 80k, R2 = 46k, R3 = 200k, R4 = 65k, R5 = 10k; R6 = 100k, size M1 = M2, Vref = 2.41V, V1 = 9.5V, V2 = -5.5V.

Making reference to the figure the following is a description of the operation of the current generating circuit it being supposed that the reference current Iref is split up in a main current Im flowing in MCR and in an auxiliary current Ia flowing in ACS.

Since MCR relies on the availability of Vref to generate Iref, whilst VRS needs Iref to generate Vref, an additional circuit is needed to start-up the current generating circuit. This start-up is realized by the auxiliary current source ACS.

At start-up a current starts flowing from V1 to V2 through resistors R3 and R4 of CS, thus establishing on the base of Q4 a voltage which is sufficiently positive to make it conductive. As a result a current Ia equal to Iref flows from V1 to V2 through M1, Q4 and R5 in series. Indeed Im equals zero since Vref is zero so that Iref is equal to Ia which is generated by CS.

Since M1 and M2 constitute a current mirror circuit, Iref also flows through R2 and consequently following equation is valid at start-up:

$$Ia = Iref = VBE(Q3)/R2$$

where VBE(Q3) is the base-emitter voltage of Q3.

Thanks to the current Iref thus realized at start-up, Vref can be generated by VRS and its value increases from 0V to a maximum steady-state Vref. As a consequence Q1 and therefore also Q2 start conducting and Im increases from 0 micro-A to a maximum steady-state Iref whilst Ia decreases from the above determined value, i.e. VBE(Q3)/R2 to zero.

Indeed, Iref has a constant value equal to VBE(Q3)/R2 as long as Im is smaller than VBE(Q3)/R2 because Q3 acts as a regulating device controlling Ia by controlling the voltage level of the interconnection point between R3 and R4, in such a way that Iref equals VBE(Q3)/R2. This implies that Ia has to decrease when Im increases. When Im exceeds a predetermined value so that Iref exceeds VBE(Q3)/R2, Q3 fully conducts and thereby shunts resistor R4 due to which transistor Q4 is blocked. Thus Im becomes equal to Iref.

In this way CS realizes the start-up of the supply circuit and is disabled by RS when Iref exceeds a predetermined value; i.e. VBE(Q3)/R2.

The zero value of Ia during normal operation is mandatory because the generation of Ia is not as accurate as that of Im, and also because Ia is more sensitive to disturbances of the power supply and to temperature variations.

On the contrary, the current generating circuit as described above is power supply and temperature independent since Vref is supply and temperature independent and also thanks to Q1 and Q2

which in combination indeed compensate for variations of their base-to-emitter voltage caused by temperature changes.

The diode D1 between MCR and ACS is used in case of integration on chip to avoid the creation of a parasitic transistor and thus also the flow of parasitic currents from Q2 to the auxiliary current source during start-up.

It has to be noted that for the earlier specified typical values of the circuit elements the predetermined value of Iref at which Q3 regulates during startup equals 15 micro-A provided that VBE(Q3) equals 0.7V, whilst the maximum or nominal value of Iref equals Vref/R1 = 30 micro-A.

It has also to be noted that Vref is specified with respect to ground. For this reason the branch of MCR generating Iref, i.e. the branch with Q2 and R1, is also grounded.

While the principles of the invention have been described above in connection with specific apparatus, it is to be clearly understood that this description is made only by way of example and not as a limitation on the scope of the invention.

Claims

1. Current generating circuit which includes a main current source (MCR) able to generate a constant steady-state reference current (Iref) from a steady-state reference voltage (Vref) provided by a voltage source (VRS), characterized in that it further includes an auxiliary current source (ACS) and an output circuit (CM) to which said auxiliary (ACS) and main (MCR) current sources at start-up, supply respective decreasing (Ia) and increasing (Im) currents and which supplies current (Iref) to said voltage source (VRS), said voltage source accordingly providing an increasing voltage (Vref) at said start-up and said increasing voltage (Vref) and current (Im) reaching said steady-state reference voltage and current respectively.

2. Current generating circuit according to claim 1, characterized in that said auxiliary current source (ACS) is disabled when said current generating circuit reaches said steady-state reference current (Iref).

3. Current generating circuit according to claim 1, characterized in that said output circuit (CM) is connected in series with the parallel connection of said main current source (MCR) and said auxiliary current source (ACS) which includes a current source (CS) generating said decreasing current (Ia) at the junction point of said output circuit (CM) and said main current source (MCR), thereby realizing an output of said auxiliary current source, and a regulating stage (RS) also connected to said junction point to control said current source in such a way that it is disabled at the latest when said steady-state reference current is reached by said current generating circuit.

4. Current generating circuit according to claim 3, characterized in that said regulating stage (RS) includes a branch in which the current generated by said current generating circuit is mirrored.

5. Current generating circuit according to claim 4, characterized in that said regulating stage (RS) includes in said branch, between a first (V1) and a second (V2) power terminal, a cascade connection of a PMOS transistor (M2) and a resistor (R2), the gate of said PMOS transistor (M2) being connected to said output of said auxiliary current source (ACS) and the interconnection of said PMOS transistor (M2) and said resistor (R2) being connected to the base of a first npn transistor (Q3) the emitter of which is connected to said second power terminal (V2).

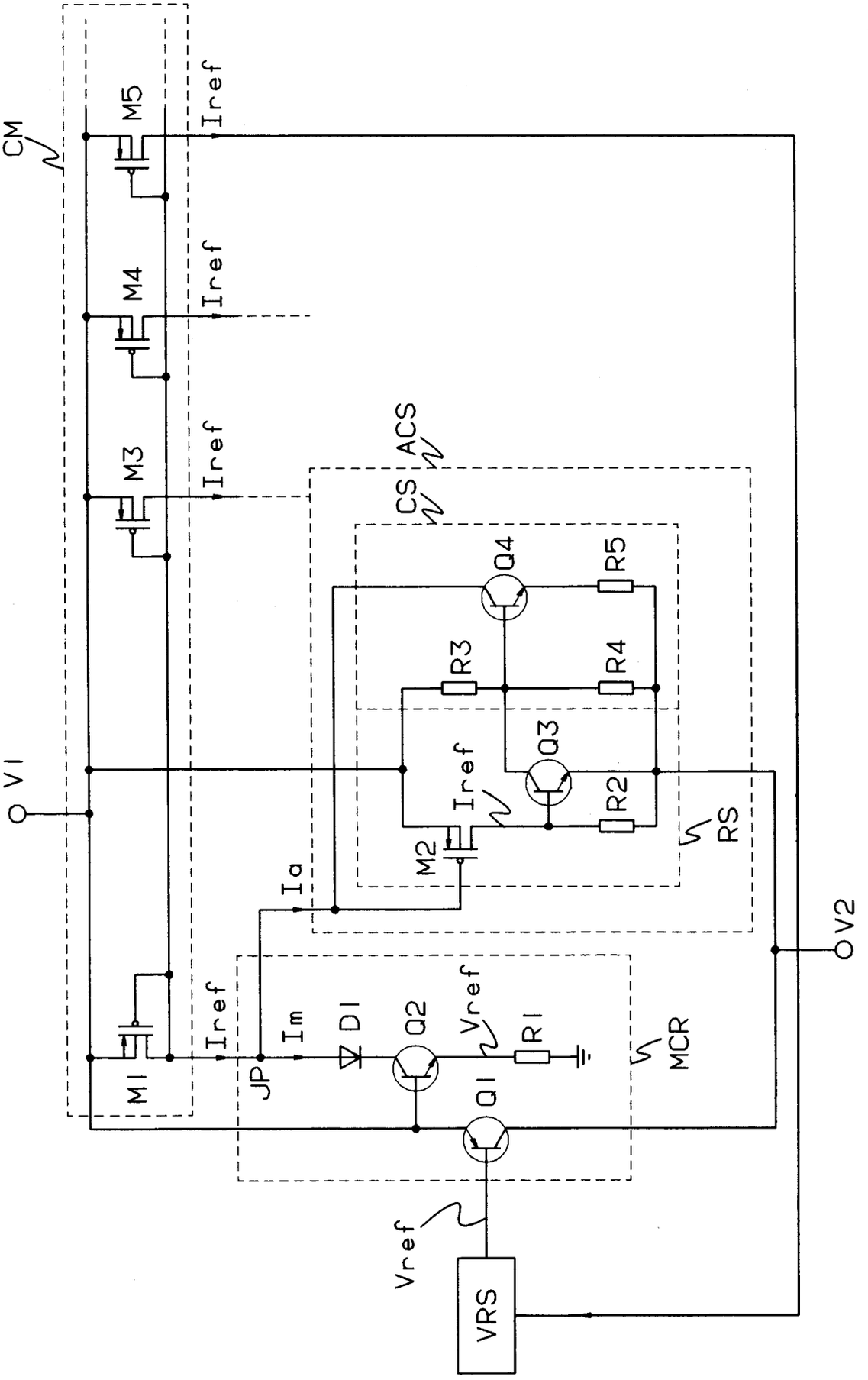
6. Current generating circuit according to claim 5, characterized in that said current source (CS) includes a second npn transistor (Q4) the collector of which is connected to said output of said auxiliary current (ACS) source and the emitter of which is coupled to said second power terminal (V2) via a second resistor (R5), and a cascade connection between said first (V1) and said second (V2) power terminal of a third (R3) and a fourth (R4) resistor, the junction point of which is connected to the base of said second npn transistor (Q4) and the collector of said first npn transistor.

7. Current generating circuit according to claim 1, characterized in that said output circuit (CM) is a current mirror and that said steady-state reference current (Iref) is distributed over an integrated circuit and provided to said voltage source (VRS) by means of said current mirror circuit (CM).

8. Current generating circuit according to claim 1, characterized in that said main current source (MCS) includes the cascade connection of a grounded resistor (R1) and an npn transistor (Q2) at the base of which a base voltage derived from said increasing and said steady-state reference voltage (Vref) is applied at start-up and nominal working respectively.

9. Current generating circuit according to claim 8, characterized in that said output circuit is a current mirror and that the collector of said npn transistor (Q2) is coupled to the drain and to the gate of a PMOS transistor (M1) which is part of said current mirror circuit (CM).

10. Current generating circuit according to claim 8, characterized in that said base voltage is applied to the base of said npn transistor (Q2) via a pnp transistor (Q1) the emitter of which is connected to the base of said npn transistor (Q2), said increasing and steady-state reference voltage being applied to the base of said pnp transistor (Q1) at start-up and nominal working respectively, thereby making the current generating circuit temperature independent.


CM
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EUROPEAN SEARCH REPORT

Application Number

EP 92 20 3508

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	US-A-4 839 535 (MILLER) * column 3, line 59 - column 4, line 22; figure *	1-3,7	G05F3/28 G05F3/26
A	US-A-4 857 823 (BITTING) * column 3, line 34 - column 4, line 66; figures 1,3 *	1,2	
A	PATENT ABSTRACTS OF JAPAN vol. 10, no. 177 (P-470)(2233) 21 June 1986 & JP-A-61 026 117 (ROHM CO LTD) 5 February 1986 * the whole document *	1,2,7	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

G05F

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	13 JULY 1993	SAAW L.J.

CATEGORY OF CITED DOCUMENTS

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