



Europäisches Patentamt
European Patent Office
Office européen des brevets



Publication number: **0 598 471 A1**

EUROPEAN PATENT APPLICATION

Application number: **93306610.2**

Int. Cl.⁵: **G06F 9/38, G06F 11/08**

Date of filing: **20.08.93**

Priority: **18.11.92 JP 307461/92**

Date of publication of application:
25.05.94 Bulletin 94/21

Designated Contracting States:
DE FR GB

Applicant: **FUJITSU LIMITED**
1015, Kamikodanaka
Nakahara-ku
Kawasaki-shi Kanagawa 211(JP)

Inventor: **Nabekura, Hideaki, c/o Fujitsu Limited**
1015, Kami-Kodanaka,

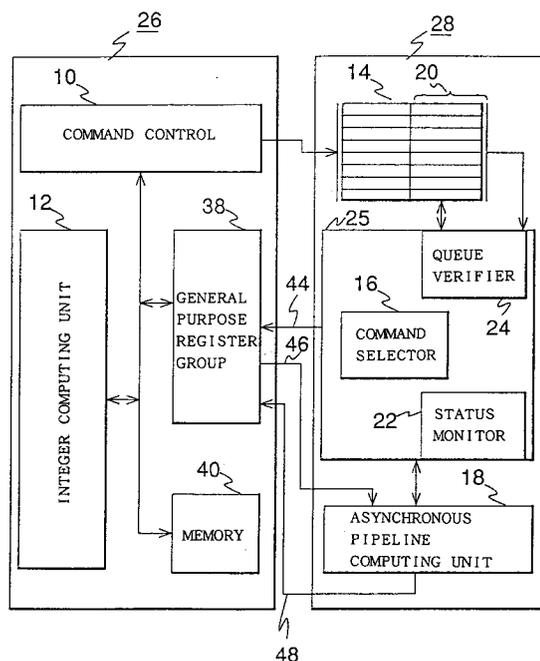
Nakahara-ku
Kawasaki-shi, Kanagawa 211(JP)
Inventor: **Fujioka, Shuntaro, c/o Fujitsu Limited**
1015, Kami-Kodanaka,
Nakahara-ku
Kawasaki-shi, Kanagawa 211(JP)

Representative: **Billington, Lawrence Emlyn et al**
HASELTINE LAKE & CO
Hazlitt House
28 Southampton Buildings
Chancery Lane
London WC2A 1AT (GB)

Method and apparatus for verifying the orderly processing of data.

Asynchronous computation commands sent from a command control are held in a command queue. The executable command is selected and supplied to a pipelined asynchronous computing unit. A status area is ensured for every command held in the command queue and pipeline bits indicative of the state of progress of the execution of the command in the unit are stored. A queue verifier discriminates the pipeline bits and verifies that a plurality of pipeline stages do not exist in an entry of any single command and that a plurality of pipeline stages do not exist among the commands, thereby guaranteeing the correct and orderly execution of the commands.

FIG. 4



EP 0 598 471 A1

The present invention relates to a method and apparatus for verifying data processing involving fetching a command held in a command queue and executing and, more particularly, to a method and apparatus for verifying data processing involving holding a command in a command queue until the execution of the command is normally finished.

In recent years, in association with the realization of a high command executing speed by a CPU, not only a command (synchronous command) is sequentially executed in every machine cycle by a synchronous computing unit but also a long command (asynchronous command) existing over a plurality of cycles is executed in parallel with the operation of the CPU by providing an asynchronous computation control unit as another computing unit. A circuit scale of the data processing apparatus, therefore, increases by a size corresponding to only the asynchronous computation control unit. Problems such as failure of an LSI and defective logic operations occur. A necessity to improve reliability is more and more increasing.

Fig. 1 shows a conventional data processing apparatus. An asynchronous computation control unit 28 to execute a long asynchronous command in parallel is provided for a central processing unit (CPU) 26 having an integer computing unit 12 to sequentially execute commands. The command is decoded by a command control 10 provided in the CPU 26. In case of a synchronous command, it is sent to the synchronous, computing unit 12 and is executed. In case of an asynchronous command, it is sent to the asynchronous computation control unit 28 and is executed. The asynchronous computation control unit 28 comprises: a command queue 14 to hold commands as a queue; a controller 25 to select the command which can be executed from the command queue 14; and an asynchronous pipeline computing unit 18 which functions as an asynchronous computing unit which receives the command selected and supplied from the command queue 14 by the controller 25 and executes the command in a plurality of cycles. As shown in Fig. 2, the command queue 14 is constructed by a command code 30, a first source register number 32, a second source register number 34, and a result register number (destination register number) 36.

When commands are generated from the command control 10 in the CPU 26, queueing to temporarily hold the commands in the command queue 14 is executed. After completion of the queueing, the command which can be executed is selected by the controller 25 and is fetched from the command queue 14 and is supplied to the asynchronous pipeline computing unit 18. When there is a command preserving request in this instance, the command is held in the command

queue 14 until the asynchronous pipeline computing unit 18 correctly finishes the execution of the command. When there is no command preserving request, the command is deleted from the command queue 14.

In the case of providing an asynchronous computation control unit in order to realize a high computation processing speed, however, the circuit scale of the data processing apparatus increases by an amount corresponding to such an asynchronous computation control unit, so that a possibility of the occurrence of an LSI failure or defective logic operation is high. That is, when the pipeline control of the asynchronous calculations based on the command queue 14 provided in the asynchronous computation control unit 28 is disturbed by the occurrence of a defective LSI, failure, disconnection of wire, defective logic operation, or the like, the contents of the command queue 14 which holds the commands as a queue cannot be guaranteed. There is consequently a problem such that the data processing apparatus does not operate in accordance with the order of the command queue and a contradiction occurs in the execution of the commands and the execution of the commands is abnormally finished.

According to the invention, there are provided a verifying method and apparatus of a data processing apparatus, in which the order and operation when asynchronous commands held in a command queue are executed are guaranteed.

According to a first aspect of the invention there is provided a method of verifying a data processing apparatus comprising:

a command transfer step of sequentially decoding commands and a distinguishing into synchronous computation commands and asynchronous computation commands and separately transferring those commands to different execution destinations;

a synchronous computing step of executing the synchronous computation commands sent by said command transfer step;

a command execution waiting step of holding the asynchronous computation commands sent by said command transfer step and waiting for the execution of said commands;

a command selecting step of selecting the executable commands from the commands held in said command execution waiting step and holding the selected command until the end of execution of the command;

a pipelined asynchronous computing step of dividing the asynchronous commands selected by said command selecting step into a plurality of stages and separately executing them;

a status monitoring step of ensuring a status area for every command held in said command

execution waiting step and storing information, indicative of the state of progress of execution of the command in said asynchronous computing step, in said status area; and

a verifying step of verifying contents of said status area.

According to a second aspect of the invention there is provided an apparatus for verifying a data processing apparatus, comprising:

command execution waiting means for holding commands and waiting for the execution of the command;

command selecting means for selecting an executable command from said command execution waiting means and for allowing said selected command to be held in said command execution waiting means until the end of the execution of the command;

pipelined asynchronous computing means for dividing the commands selected by said selecting means into a plurality of stages and executing said commands in parallel;

status monitoring means for ensuring a status area for every command held in said command execution waiting means and storing information, indicative of the state of progress of the execution of the command in said asynchronous computing means, in said status area; and

verifying means for verifying said status area.

In this specification, except where the context does not so permit, reference to pipeline stages and the like existing in the status area shall be construed to mean that status bits are set in the status area for the relevant command to indicate its being processed by the relevant pipeline stage. The terms "status bit" and pipeline bit" are used synonymously to mean data bits assigned to the various commands and set as flags to indicate the status of the command with respect to any one of the pipeline stages.

First, the invention is constructed by a central processing unit (CPU) and an asynchronous computation control unit. The CPU comprises: a command control for sequentially decoding commands in accordance with the order and distinguishing into a synchronous computation command and an asynchronous computation command and sending those commands to different destinations; and an integer computing unit (synchronous computing means) for executing the synchronous computing command sent from the command control. The asynchronous computation control unit comprises: a command queue for holding the asynchronous computing commands sent from the command control and waiting for the execution of the command; a command selector for selecting the command which can be executed from the command queue and for allowing the selected command to

be held in the command queue until the completion of the execution of the command; and an asynchronous pipeline computing unit which has been pipelined and executes the asynchronous command selected by the command selector in parallel at a plurality of stages.

According to the invention, further, there are provided: a status monitor for ensuring a status area for every command stored in the command queue and storing information (pipeline bits), indicative of the progress status of the execution of the command in the asynchronous pipeline computing unit, in the status area; and a queue verifier for verifying the status area. The queue verifier checks status bits (pipeline bits) of the status area for every command held in the command queue and verifies that a plurality of pipeline stages don't exist in an entry of the same command, thereby guaranteeing the order and operation when the command is executed. At the same time, the queue verifier checks status bits (pipeline bits) of the status area in portions among a plurality of commands held in the command queue and verifies that a plurality of the same pipeline stages don't exist among the commands, thereby guaranteeing the order and operation of the commands.

According to the verifying method and apparatus of the data processing apparatus of the invention as mentioned above, a status area 20 to store the pipeline bits is inventively provided for the command queue 14 of the asynchronous computation control unit, thereby enabling the following conditions to be verified and guaranteeing the order and operation upon execution of commands.

Condition 1:

More than one pipeline stage must not exist in the entry of any single command in the command queue.

Condition 2:

The same pipeline stage must not exist more than once among the commands in the command queue.

Therefore, in the case where a pipeline control of the asynchronous calculations based on the command queue provided in the asynchronous computation control unit is disturbed due to the occurrence of a defective LSI, failure, disconnection of wire, defective logic operation, or the like, two or more pipeline bits are set into the entry of one command or two or more pipeline bits are set into the same stage among a plurality of commands. Therefore, abnormalities of the order and operation in the execution of the commands are immediately recognized and a proper error re-

covering process is started. By adding command queue pipeline bits and by checking the order and operation in the execution of the commands based on the command queue, accordingly, the contents in the command queue can be guaranteed.

For a better understanding of the invention, and to show how the same may be carried into effect, reference will now be made, purely by way of example, to the accompanying drawings in which

Fig. 1 is an explanatory diagram of a conventional data processing apparatus;

Fig. 2 is an explanatory diagram of a conventional command queue;

Fig. 3 is a block diagram showing a whole construction of the invention;

Fig. 4 is a block diagram showing an embodiment of the invention;

Fig. 5 is an explanatory diagram of a command queue which is used in the invention;

Fig. 6 is a time chart showing a state of the parallel execution of commands in an asynchronous pipeline computing unit;

Fig. 7 is an explanatory diagram showing a checking state of pipeline bits in the case where the commands were correctly executed;

Fig. 8 is an explanatory diagram showing a checking state of pipeline bits in the case where an abnormality occurred during the execution of commands;

Fig. 9 is an explanatory diagram showing a checking state of pipeline bits among commands in the normal operation;

Fig. 10 is an explanatory diagram showing a checking state of the pipeline bits among the commands when an abnormal operation has occurred;

Fig. 11 is an explanatory diagram showing a command control of a central processing unit in Fig. 4; and

Fig. 12 is a flowchart showing an asynchronous control of an asynchronous computation control unit in Fig. 4.

Fig. 3 shows the complete construction of a data processing apparatus according to the invention. The data processing apparatus is constructed by a main storage unit (MSU) 100, a main storage control unit (MCU) 200, and the processor unit 300. The processor unit 300 includes the CPU 26 having a function serving as a synchronous computing unit to sequentially execute commands and the asynchronous computation control unit 28 having a pipeline computing unit for asynchronously executing a long command. An information processing apparatus for executing commands in parallel at a high processing speed by the CPU 26 and asynchronous computation control unit 28 as mentioned above is used as a scalar unit of each processor element which is used in a super computer with a

parallel machine structure.

Fig. 4 shows the details of the CPU 26 and asynchronous computation control unit 28 provided in the processor unit 300 in Fig. 3. The CPU 26 comprises: the command control 10; the integer computing unit 12 which functions as a synchronous computing unit; a general purpose register group 38 having various general registers which are used to execute commands; and a memory 40 which is used as a local memory such as a cache memory or the like. The command control 10 sequentially decodes commands and sends the command to the integer computing unit 12 after a synchronous computing command is decoded, thereby allowing an integer calculation which is finished in one cycle to be executed. When the command control 10 decodes an asynchronous computing command, for example, a floating point computing command, since such a command is a long command which is executed in a plurality of cycles, it is sent to the asynchronous computation control unit 28 and is executed in parallel.

The control unit 28 comprises: the command queue 14 as command queueing means; the controller 25; and the asynchronous pipeline computing unit 18 as a pipelined asynchronous computing unit. The command queue 14 is constructed by the command code 30, the first source register number 32, the second source register number 34, and the result register number (destination register number) 36 every commands 1 to n shown as indices in Fig. 5. Further, pipeline bits are provided as a status area 20. In the asynchronous pipeline computing unit 18 in Fig. 4, since the pipeline is constructed by four stages of a fetching stage F, a first executing stage E₁, a second executing stage E₂, and a writing stage W, storage areas of four pipeline bits corresponding to the stages F, E₁, E₂, and W are provided as pipeline bits of each command held in the command queue 14.

Referring again to Fig. 4, the controller 25 is provided in the asynchronous computation control unit 28. Various functions as command selector 16, status monitor 22, and queue verifier 24 are provided for the controller 25. The command selector 16 fetches the command which can be executed from the commands held as a queue in the command queue 14 and supplies to the asynchronous pipeline computing unit 18. In this instance, the command selector 16 notifies the first source register number 32, second source register number 34, and result register number 36 of the command fetched from the command queue 14 to the general purpose register group 38 of the CPU 26 through a register address bus 44 and supplies the source data stored in the corresponding source register to the asynchronous pipeline computing unit 18 through a source data bus 46. The result of

the execution by the computing unit 18 is written through a write data bus 48 into a destination register that is designated by the result register number designated via the register address bus 44. Further, the status monitor 22 and the queue verifier 24 are provided for the controller 25 in correspondence to the pipeline bits (F, E₁, E₂, W) provided in the status area 20 of the command queue 14. The status monitor 22 monitors a progressing situation of the command supplied to the asynchronous pipeline computing unit 18 and rewrites the pipeline bits provided in the status area 20 of the command queue 14 each time the command advances to the fetching stage, first executing stage, second executing stage, and writing stage.

Fig. 6 is a time chart showing an executing state of the commands in the asynchronous pipeline computing unit 18. First, a command 1 is supplied to the first fetching stage in a T₁ cycle. A process based on the source data in the first source register is executed at the first executing stage E₁ in the next T₂ cycle. In the T₂ cycle, the next command 2 is supplied to the fetching stage F. In the next T₃ cycle, the command 1 advances to the second executing stage E₂ and a process based on the source data from the second source register is executed. At the same time, the command 2 progresses to the first executing stage E₁ and a process based on the source data in the first source register is executed and a command 3 is further newly supplied to the fetching stage F. In the T₄ cycle, the command 1 progresses to the writing stage W and the result of the execution is written into the destination register. The command 2 advances to the second executing stage E₂ and the command 3 further progresses to the first executing stage E₁. In the T₅ cycle, the command 2 progresses to the writing stage W and the command 3 advances to the second executing stage E₂. In the T₆ cycle, the command 3 progresses to the writing stage W.

The parallel executing stages of a plurality of commands in the asynchronous pipeline computing unit 18 as shown in Fig. 6 are monitored by the status monitor 22. As for the pipeline bits (F, E₁, E₂, W) of each command in the status area 20 of the command queue 14, the pipeline bit indicative of the stage at which the corresponding command exists is set into bit 1 and the other pipeline bits are reset to 0. The queue verifier 24 provided in the controller 25 checks the contents in the status area 20 of a plurality of commands held in the command queue 14 for every cycle of the asynchronous pipeline computing unit 18, thereby verifying whether the order and operation of the asynchronous pipeline computing unit 18 according to the commands held in the command queue 14 are

correct or not.

Fig. 7 shows cycle changes in pipeline bits in the status area 20 of the command queue 14 in the case where a certain command had been supplied to the computing unit 18 and was correctly executed. Such cycle changes correspond to, for example, the command execution for an interval from T₀ cycle to the T₄ cycle of the command 1 shown in Fig. 6. The first T₀ cycle indicates the pipeline bits before the command is supplied. When the commands are correctly executed as mentioned above, only a single one of the pipeline bits (F, E₁, E₂, W) in all of the T₁ to T₄ cycles is equal to 1 for any single command. That is, more than one pipeline stage is not permitted in the entry of the single command. Before the command is supplied, all of the pipeline bits are set to 0.

The queue verifier 24 of the invention executes an NC1 check every command with regard to the pipeline bits of the command queue 14. The NC1 check denotes that in the case where all of the four pipeline bits are equal to 0 or any single one of them is set to 1, a check output signal of 1 is generated, thereby indicating that the operation is correctly being executed by the check output 1. On the other hand, when two or more bits among the four pipeline bits are equal to 1, a check output signal of 0 is generated, thereby indicating that the operation is abnormally executed.

Fig. 8 shows an abnormality of the operation such that the pipeline bits F and E₁ are equal to 1 and two commands exist in the same entry in the T₁ cycle in Fig. 7. In this case, the result of the NC1 check in the T₁ cycle is equal to 0 and the occurrence of an abnormality can be detected. Fig. 9 shows a verification of the pipeline bits among a plurality of commands in the queue verifier 24 and shows the case where all of the commands are correctly being executed. In such a case, for example, five commands of the command Nos. 1 to 5 are held in the command queue 14 and have the bit contents shown in the pipeline bits (F, E₁, E₂, W) and the normal operations are being executed. Therefore, only one bit exists in the same stage among the commands, namely, in the bit train when it is seen in the vertical direction. Since a plurality of commands cannot exist in the same stage of the pipeline the queue verifier 24 guarantees the correct order and operation. In this case as well, the NC1 check is executed over the same pipeline bit among a plurality of commands and the operation is correctly executed, so that all of the results of the verification among the commands are set to 1.

Fig. 10 shows the case where an abnormality occurred in the NC check among the commands in Fig. 9. The bit 1 is set in the command Nos. 2 and 3 with respect to the pipeline bit E₁ and the result

of the verification is set to 0, so that the occurrence of an abnormality of the operation can be recognized. In the queue verifier 24 in the invention, either one of NC1 check of every command shown in Figs. 7 and 8 and the NC1 check among the commands shown in Figs. 9 and 10 can be executed. In order to discriminate that the abnormality has occurred with respect to the execution of any command, it is desirable to simultaneously execute the NC1 check of every command and the NC1 check among the commands. For example, when an abnormality as shown in Fig. 10 occurs, it is possible to recognize that although the order and operation in the execution of the commands of the command No. 3 are correct, it is possible to recognize that the operation and order of the next command number 4 are wrong. Such an abnormality can be recovered by the retry of the command 4.

Fig. 11 is a flowchart showing control processes by the command control 10 of the CPU 26 shown in Fig. 4. First, in step S1, the command control 10 fetches commands in accordance with a predetermined order. In step S2, the command control decodes the command. In step S3, a check is made to see if the command is a floating point computation command or not from the result of the decoding of the command. When the command is an integer computation command, it is sent to the integer computing unit 12, by which the integer computation command is executed in one cycle in step S4. When the command is the floating point computation command, step S8 follows and the floating point computation command is sent to the command queue 14 in the asynchronous computation control unit 28. When the integer computation command is executed in step S4, a check is made in step S5 to see if the apparatus waits for the end of the queueing preceding command sent to the asynchronous computation control unit 28 or not. If YES, step S6 follows and the apparatus waits for a notification indicative of the end of the execution of the preceding command sent to the control unit 28. If NO in step S5 or when the notification of the end of the execution of the preceding command is received in step S6, the processing routine advances to step S7 and the command number is increased by +1. The processing routine is again returned to step S1 and the next command is fetched and processes similar to those mentioned above are also executed hereinafter.

Fig. 12 is a flowchart showing asynchronous controls by the controller 25 provided in the asynchronous computation control unit 28 shown in Fig. 4. First, in step S1, the command which can be executed by the command selector 16 provided in the controller 25 is selected from the commands in the command queue 14 and supplied to the asynchronous pipeline computing unit 18. In step S2, a

check is made to see if there is a preserving request or not with respect to the supplied command. If there is not preserving request, the command which has already been supplied to the computing unit 18 is deleted from the command queue 14 in step S8. Since the floating point computation command as a target of the verification in the invention has the preserving request, it is not deleted from the command queue 14 and the processing routine advances to step S3. A bit updating process to set the pipeline bit corresponding to the pipeline stage in which the command exists into 1 each time the command cycle is executed by the asynchronous pipeline computing unit 18 is executed for the status area 20 of the command queue 14. In step S4, each time the bit updating process is finished, the pipeline bit stored in the status area 20 of the command queue 14 is discriminated. In this discrimination, both of the NC1 check in the entry of every command and the NC1 check between commands are performed. In step S5, the presence or absence of an abnormality is judged from the result of the NC1 checks. When all of the results of the NC1 checks are equal to 1, it is determined that the operation was correctly executed, so that step S6 follows. In step S6, a check is made to see if the command which has finished the final stage exists or not. If YES, step S7 follows and an execution end command is deleted from the command queue.

When bit 0 is obtained from the result of the NC1 checks about the pipeline bits in step S5, it is determined that there is an abnormality, so that step S9 follows an error process is executed. For example, a retry process for again fetching the command in which an abnormality has occurred from the command queue 14 and for supplying to the asynchronous pipeline computing unit 18 is executed. By executing such a retry process, when the normal operation is judged from the NC1 checks about the pipeline bits in step S9, it is decided that the operation has been recovered. The processing routine is again returned to the process in step S1. On the other hand, when the occurrence of the abnormality is based on a cause of the hardware such as disconnection of wire, failure, or the like, the abnormality will not be recovered even by executing the retry process. Therefore, the processing routine advances to step S11 and a termination is made as an abnormality. In such an abnormality termination, for instance, in the case where the data processing apparatus of the invention is used in the scalar units of processor elements of a super computer with a parallel machine structure or the like, a process such as to disconnect the processor element having the scalar unit which has caused an abnormality from target for the parallel processes or the like is executed.

According to the invention as mentioned above, in the case where an abnormality occurred due to the occurrence of a disturbance of the control in the execution of the commands based on the command queue because of a defective LSI, failure, disconnection of wire, defective logic operation, or the like, since the pipeline bits provided for the command queue are always discriminated, the operation abnormality can be recognized on the basis of the result of the discrimination. A countermeasure such as abnormality termination or the like, accordingly, can be made. The correct order and operation of the execution of the commands using the command queue can be always guaranteed. The reliability of the asynchronous computation control unit can be remarkably improved.

Although the above embodiment has been described with respect to the data processing apparatus which is used as a scalar unit in the processor element of a super computer as an example, the invention is not limited to such an example but can be also directly used as a central processing unit of a conventional computer.

Further, the present invention is not limited to the above embodiment but many modifications and variations are possible without departing from the spirit and scope of the claims of the invention. The invention is also not limited by the numerical values shown in the embodiment.

Claims

1. A method of verifying a data processing apparatus comprising:
 - a command transfer step of sequentially decoding commands and distinguishing into synchronous computation commands and asynchronous computation commands and separately transferring those commands to different execution destinations;
 - a synchronous computing step of executing the synchronous computation commands sent by said command transfer step;
 - a command execution waiting step of holding the asynchronous computation commands sent by said command transfer step and waiting for the execution of said commands;
 - a command selecting step of selecting the executable commands from the commands held in said command execution waiting step and holding the selected command until the end of execution of the command;
 - a pipelined asynchronous computing step of dividing the asynchronous commands selected by said command selecting step into a plurality of stages and separately executing them;
 - a status monitoring step of ensuring a sta-

tus area for every command held in said command execution waiting step and storing information, indicative of the state of progress of execution of the command in said asynchronous computing step, in said status area; and
a verifying step of verifying contents of said status area.

2. A method according to claim 1, wherein in said status monitoring step, each storage area is provided with a status bit for each pipeline stage in said asynchronous computing step and the status bit is set as a bit flag indicative of the execution of the command.
3. A method according to claim 2, wherein in said verifying step, the status bits of each status area are discriminated for each command held in said command execution waiting step, thereby verifying that a plurality of pipeline stages do not exist for any single command entry.
4. A method according to claim 1, 2 or 3, wherein in said verifying step, in the case where a plurality of pipeline bits exist in the status area of any single command, it is determined that an abnormality in the computation control has occurred.
5. A method according to claim 3 or 4, wherein in said verifying step, status bits of the status area are discriminated among said plurality of commands held in said command execution waiting step, thereby verifying that more than one of the same pipeline stage does not exist among the said plurality of commands.
6. A method according to any one of claims 2 to 5 wherein in said verifying step, in the case where a plurality of status bits exist for the same pipeline stage in a plurality of commands, it is determined that an abnormality in the computation control has occurred.
7. A method according to any one of the preceding claims, wherein in the said command control step, in the case where a floating point command is decoded, said floating point command is sent to said command execution waiting step.
8. A method according to any one of the preceding claims wherein in said command selecting step, in the case where a floating point command is selected, said floating point command is held in said command execution waiting step until the end of the execution of the command by said asynchronous computing

step.

9. An apparatus for verifying a data processing apparatus, comprising:
- command execution waiting means for holding commands and waiting for the execution of the command; 5
 - command selecting means for selecting an executable command from said command execution waiting means and for allowing said selected command to be held in said command execution waiting means until the end of the execution of the command; 10
 - pipelined asynchronous computing means for dividing the commands selected by said selecting means into a plurality of stages and executing said commands in parallel; 15
 - status monitoring means for ensuring a status area for every command held in said command execution waiting means and storing information, indicative of the state of progress of the execution of the command in said asynchronous computing means, in said status area; and 20
 - verifying means for verifying said status area. 25
10. An apparatus according to claim 9, further comprising:
- command control means for sequentially decoding commands and distinguishing said commands into synchronous computation commands and asynchronous computation commands and separately transferring said commands to different execution destinations; 30
 - synchronous computing means for executing the synchronous computation commands sent from said command control means; 35
 - and wherein the commands sent to the command execution waiting means are asynchronous commands. 40
11. An apparatus according to claim 9 or claim 10, wherein said status monitoring means provides each storage area with a status bit for every pipeline stage of said asynchronous computing means and sets the status bit as a bit flag indicative of the state of execution of the command. 45
12. An apparatus according to claim 9, 10 or 11, wherein the said verifying means discriminates each status bit of the status area for every command held in the command execution waiting means, thereby verifying that a plurality of pipeline stages do not exist for any single command entry. 50
13. An apparatus according to claim 9, 10, 11 or 12, wherein in the case where a plurality of pipeline bits exist in the status area of any single command, said verifying means verifies that an abnormality in the computation control has occurred.
14. An apparatus according to any one of claims 9 to 13, wherein said verifying means discriminates status bits in the status areas among said plurality of commands held in the command execution waiting means, thereby verifying that more than of the same pipeline stage does not exist for the said plurality of commands.
15. An apparatus according to any of claims 10 to 14, wherein in the case where a plurality of status bits exist indicating the same pipeline stage for the plurality of commands, said verifying means determines that an abnormality of the computer has occurred.
16. An apparatus according to any one of claims 9 to 15, wherein in the case where a floating point command is decoded, said command control means transfers said floating point command to said command execution waiting means.
17. An apparatus according to any one of claims 9 to 16, wherein in the case where said command selecting means selects a floating point command, said floating point command is held in said command execution waiting means until the end of the execution of the command by said asynchronous computing means.
18. An apparatus according to any one of claims 9 to 17, wherein said command control means and said synchronous computing means together form a central processing unit.
19. An apparatus according to any one of claims 9 to 19, wherein said command execution waiting means, said command selecting means, said asynchronous computing means, said status monitoring means, and said verifying means together form an asynchronous computation control unit. 55

FIG. 1
PRIOR ART

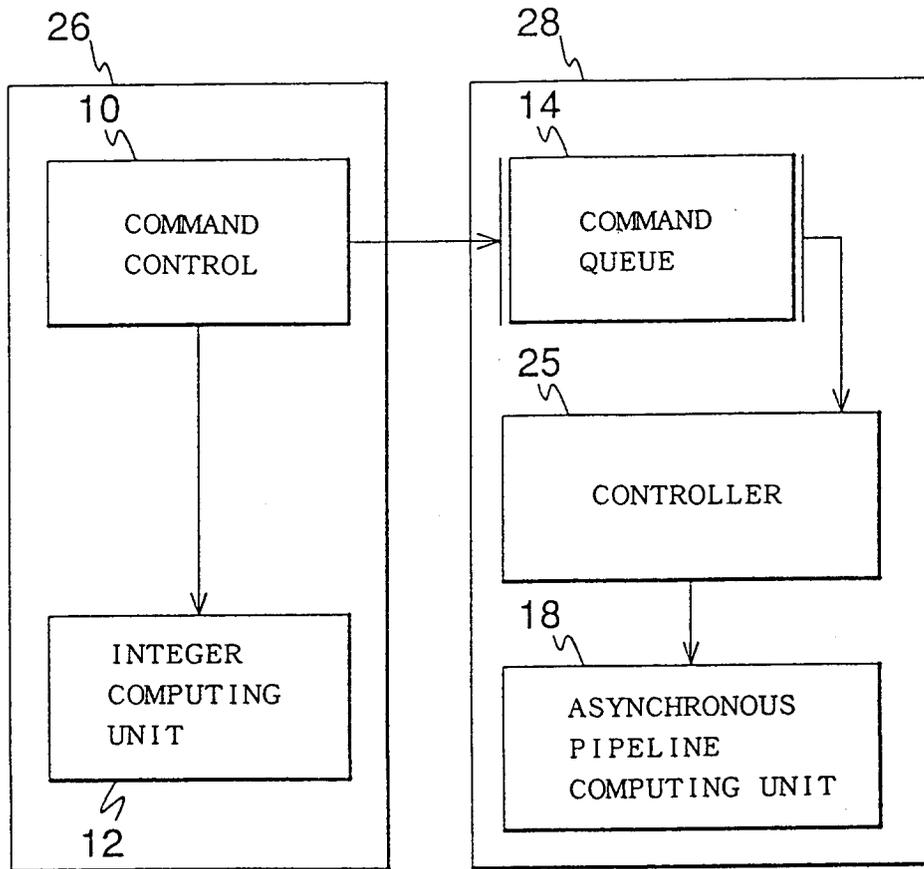


FIG. 2
PRIOR ART

	COMMAND CODE	FIRST SOURCE REGISTER NUMBER	SECOND SOURCE REGISTER NUMBER	RESULT REGISTER NUMBER
COMMAND n	<u>30</u>	<u>32</u>	<u>34</u>	<u>36</u>
⋮	⋮	⋮	⋮	⋮
COMMAND 2				
COMMAND 1				

FIG. 3

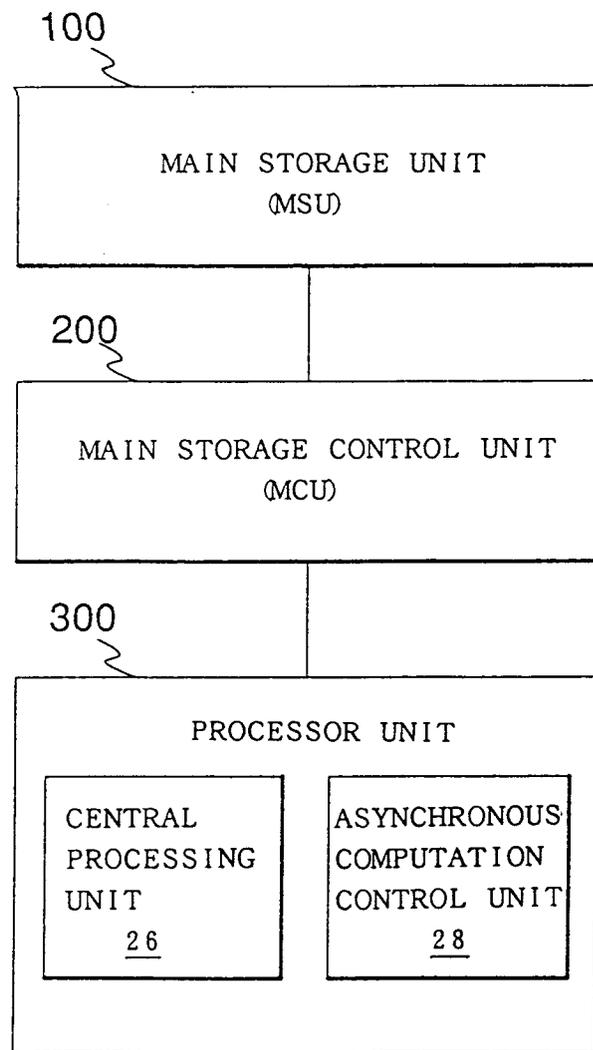


FIG. 4

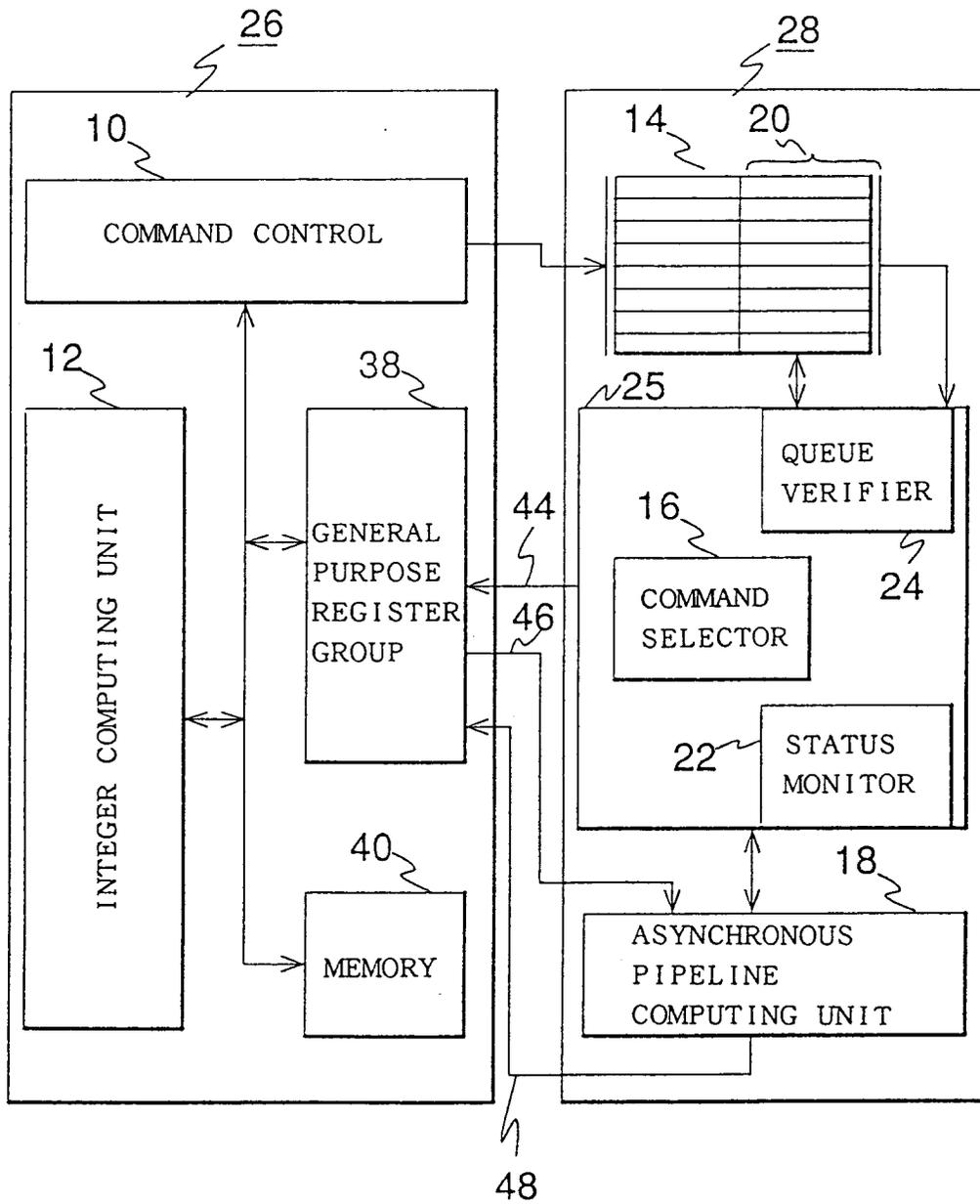


FIG. 5

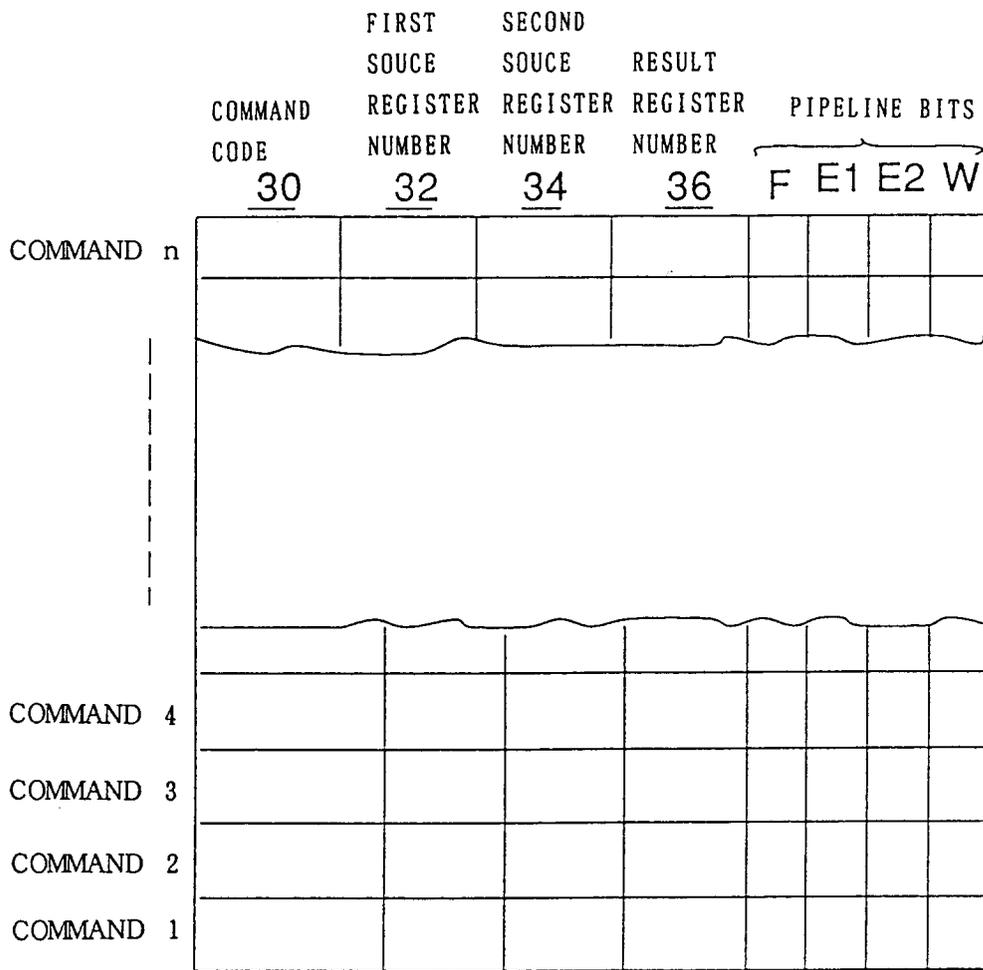


FIG. 6

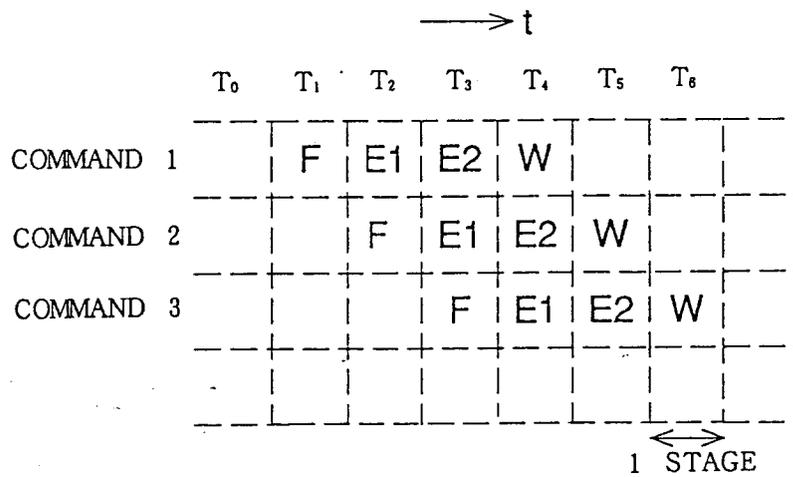


FIG. 7

TIME	PIPELINE BIT				RESULT OF CHECK-IN ENTRY
	F	E1	E2	W	
T ₀	0	0	0	0	1
T ₁	1	0	0	0	1
T ₂	0	1	0	0	1
T ₃	0	0	1	0	1
T ₄	0	0	0	1	1

FIG. 8

TIME	PIPELINE BIT				RESULT OF CHECK-IN ENTRY
	F	E1	E2	W	
T ₀	0	0	0	0	1
T ₁	1	1	0	0	0 ← ERROR
T ₂	0	1	0	0	1
T ₃	0	0	1	0	1
T ₄	0	0	0	1	1

FIG. 9

COMMAND NUMBER	PIPELINE BIT			
	F	E1	E2	W
5	0	0	0	0
4	1	0	0	0
3	0	1	0	0
2	0	0	1	0
1	0	0	0	1
	1	1	1	1

FIG. 10

COMMAND NUMBER	PIPELINE BIT			
	F	E1	E2	W
5	0	0	0	0
4	1	1	0	0
3	0	1	0	0
2	0	0	1	0
1	0	0	0	1
	1	0	1	1

↑
ERROR

FIG. 11

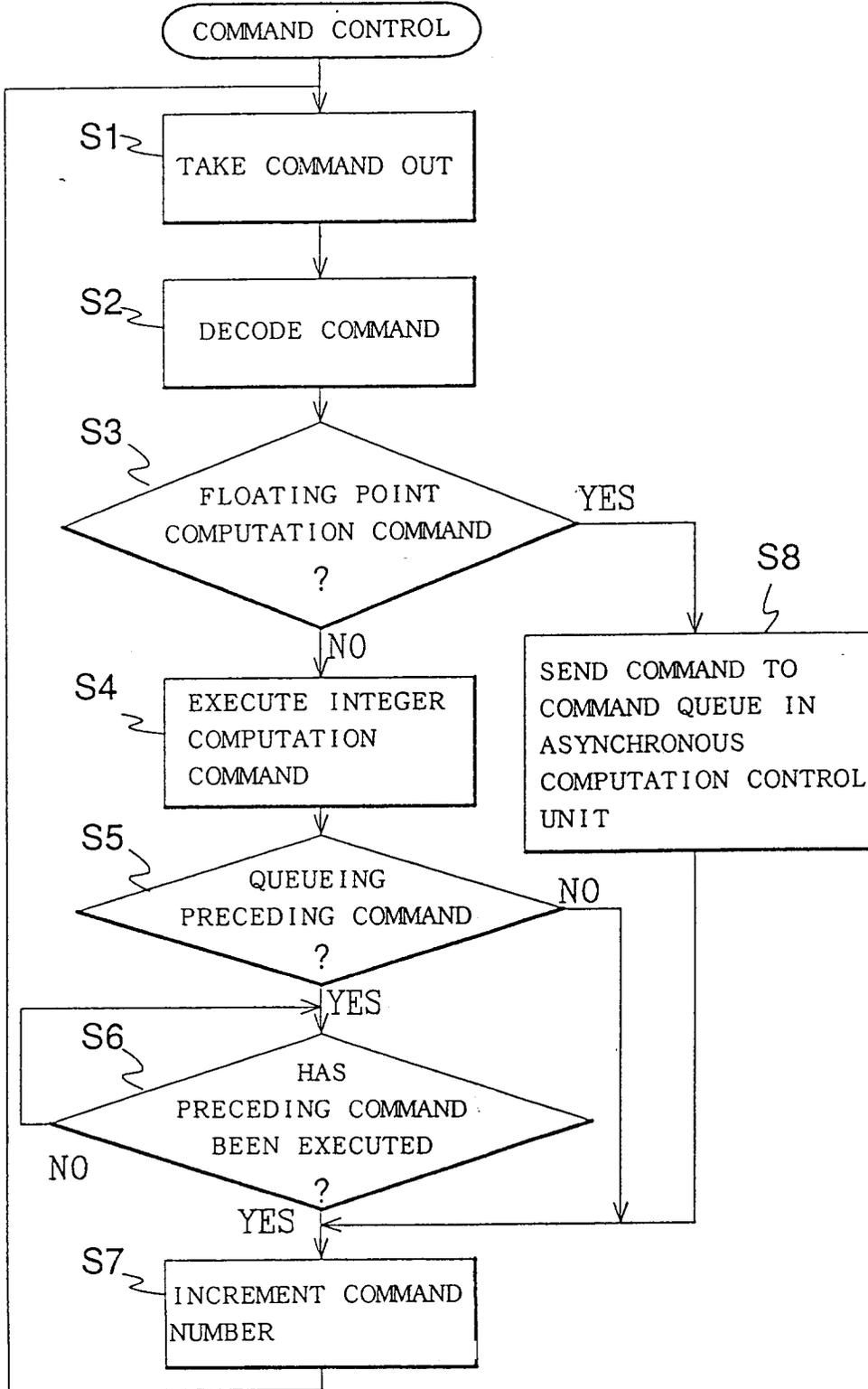
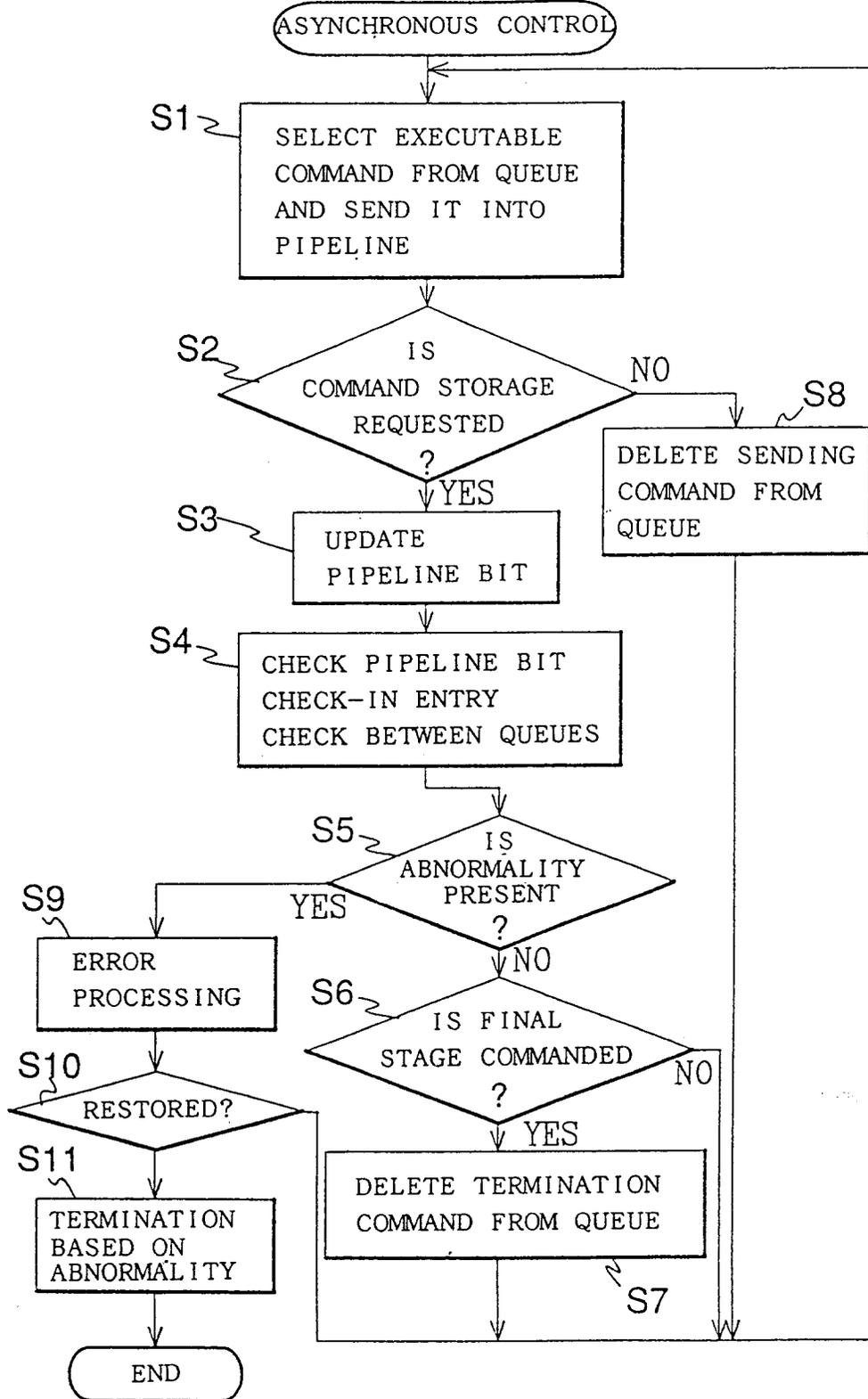


FIG. 12





DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
Y	US-A-5 109 514 (GARNER ET AL.) * summary; column 5, line 55 - column 7, line 35 * ---	1,2, 7-11, 16-19	G06F9/38 G06F11/08
P,Y	WO-A-93 01544 (THE VICTORIA UNIVERSITY OF MANCHESTER) * the whole document * ---	1,2, 7-11, 16-19	
A	INTERNATIONAL CONFERENCE ON COMPUTER DESIGN, ICCD '90, 17 September 1990 , CAMBRIDGE, US pages 14 - 19 YOSHIDA ET AL. 'A strategy for avoiding pipeline interlock delays in a microprocessor' * figure 4; section 3.1 : 'Scoreboard register' * ---	1,2,9,11	
A	EP-A-0 405 489 (BULL HN INFORMATION SERVICES LTD.) * the whole document * -----	1,2,9,11	TECHNICAL FIELDS SEARCHED (Int.Cl.5) G06F
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 2 February 1994	Examiner Weinberg, L
CATEGORY OF CITED DOCUMENTS		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document	
X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document			

EPO FORM 1503 03.82 (P04C01)