



⑪ Publication number: **0 600 499 A1**

⑫ **EUROPEAN PATENT APPLICATION**

⑳ Application number: **93119471.6**

⑤① Int. Cl.⁵: **G09G 3/36**

㉔ Date of filing: **02.12.93**

③① Priority: **02.12.92 JP 349887/92**

④③ Date of publication of application:
08.06.94 Bulletin 94/23

⑧④ Designated Contracting States:
DE FR GB IT NL

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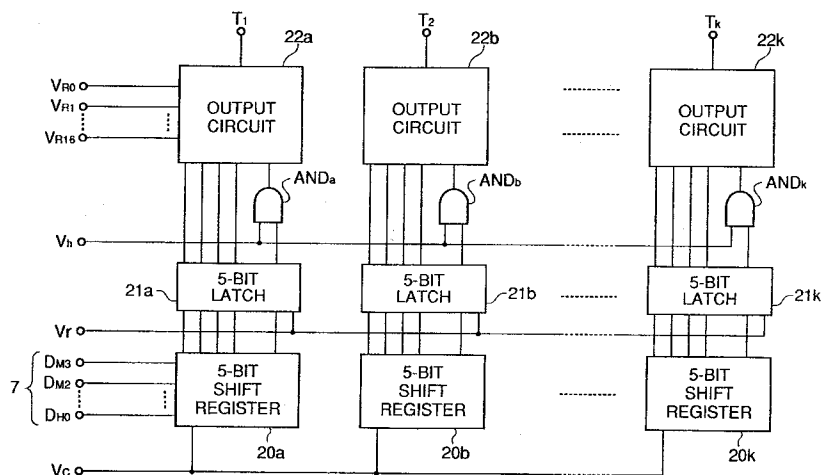
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⑤④ **Circuit for driving liquid crystal device.**

⑤⑦ A liquid crystal display driving circuit comprises a plurality of transfer gates having their one end connected in common to a source line of a liquid crystal display panel and their other end connected to a plurality of driving voltages, respectively, for supplying a different voltage to the source line. A control circuit receives an image input data for selectively turning on the transfer gates, for the purpose of realizing a multiple gray scale display. The control circuit is configured to turn on one transfer

gate selected from the plurality of transfer gates during a first period of one display period, and then, to maintain the turned-on condition of the selected transfer gate during the remaining period of one display period, or to simultaneously turn on two transfer gates which are selected from the plurality of transfer gates and which include the selected transfer gate during the remaining period of one display period.

FIGURE 5



Background of the Invention

Field of the invention

The present invention relates to a liquid crystal device driving circuit, and more specifically, to a circuit for driving a liquid crystal display panel capable of displaying an image with a multiple tone level.

Description of related art

As a liquid crystal device driving circuit for generating a source voltage driving a liquid crystal display panel typified by an active matrix type, a circuit for enabling a multiple tone or gray scale image on the order of eight gray scale levels has been implemented in the form of a LSI (large scale integrated circuit) and is now put under a mass production and widely actually used.

Figure 1 is a block diagram showing one example of a conventional liquid crystal device driving circuit. In order to display a multiple gray scale image in a liquid crystal display panel, it is required to supply a drive voltage corresponding to a required luminance, from drive voltage output terminals T1 to Tk of a transistor switch circuit 3 to corresponding source lines of the liquid crystal display panel.

For this purpose, the drive circuit includes "k" stages of "n"-bit shift registers 15a to 15k receiving an image input data Vi from an image data input terminal, a corresponding number of "n"-bit latches 16a to 16k each for latching the "n"-bit data of a corresponding one of the "n"-bit shift registers 15a to 15k, and a corresponding number of selector circuits 14a to 14k for selectively turning on output transistors Q11 to Qmk included in the transistor switch circuit 3 on the basis of an output of the latches 16a to 16k.

Namely, an "n"-bit digital image input data Vi indicative of "m" gray scale levels is supplied from the image data input terminal 7, and shifted and stored in the "n"-bit shift registers 15a to 15k in response to a clock pulse Vc applied to a clock input terminal 1. In response to a latch pulse Vr applied to a latch pulse input terminal 2, the data stored in each of the registers is transferred to a corresponding one of the "n"-bit latches 16a to 16k.

The "n"-bit data latched in each latch is decoded by a corresponding one of the selector circuits 14a to 14k to the effect that one transistor of the first "m" output stage transistors Q11 to Qm1 connected to the drive output terminal T1 of the transistor switch circuit 3 is turned on, and one transistor of the "k"th "m" output stage transistors Q1k to Qmk connected to the drive output terminal

Tk is turned on. With this arrangement, voltages V1, V2, . . . , Vm corresponding to drain voltage terminals 8a to 8m of "m" gray scale levels are supplied, so that voltages of "m" gray scale levels are supplied to an external liquid crystal display.

For example, assuming that the image input data Vi is composed of digital signals D0, D1, . . . , Dn-1, the voltage Vo appearing on the drive output terminal T1 is as shown in Figure 2.

In this conventional liquid crystal device driving circuit, if the number of gray scale levels is increased, it is required to connect low-impedance large-current-capacity, external voltage supplies, and therefore, when the driving circuit is assembled in the liquid crystal display panel, wiring conductors must be thickened and the overall assembly of the liquid crystal display panel correspondingly becomes large. In addition, with increase in the number of pixels in the liquid crystal display panel, the driving circuit is required to have a low impedance.

Furthermore, if the number of gray scale levels is increased, when a buffer circuit having a low impedance and a large output capacity is implemented on the same semiconductor substrate, the chip size becomes extremely large, and therefore, the driving circuit becomes a high cost. Because of this reason, most of this type of liquid crystal display driver is on the order of 8 gray scale levels to 16 gray scale levels. For a full-color display, however, the liquid crystal display panel required to have a gray scale of 64 levels or more is going to be put on market.

Under this circumstance, in order to increase the number of gray scale levels, the present applicant has proposed one approach, which is disclosed in the specification of Japanese Patent Application No. Hei 4-80176. This approach is featured, not only by turning on only one of the transistors Q11 to Qm1 of the transistor switch circuit as in the circuit shown in Figure 1, but also by simultaneously turning on a plurality of transistors of the transistors Q11 to Qm1, so that the voltage outputted from the drive voltage output terminal T1 has a multiple voltage level.

Figure 3 is a block diagram of this liquid crystal display driving circuit, and in Figure 3, the elements similar to those shown in Figure 1 are given the same Reference Numerals. This liquid crystal display driving circuit includes

For this purpose, the drive circuit includes "k" stages of "(n+1)"-bit shift registers 5a to 5k receiving an image input data from an image data input terminal 7, a corresponding number of "(n+1)"-bit latches 6a to 6k each for latching the "(n+1)"-bit data of a corresponding one of the "(n+1)"-bit shift registers 5a to 5k, and a corresponding number of selector circuits 4a to 4k for

selectively turning on output transistors Q11 to Qmk included in the transistor switch circuit 3 by decoding the data outputted from the latches 6a to 6k. With a selective turning-on control of the transistors Q11 to Qmk in the transistor switch circuit 3, a drive output voltage Vo is generated on each of the drive voltage output terminals T1 to Tk.

Namely, a digital image input data Vi formed of "(n+1)" bits (D0, D1, . . . , Dn) is supplied from the input terminal 7, and sequentially shifted and stored in the "(n+1)"-bit shift registers 5a to 5k in response to a clock pulse Vc. In response to a latch pulse Vr, the data stored in each of the registers is transferred to a corresponding one of the "(n+1)"-bit latches 6a to 6k. The "(n+1)"-bit data latched in each latch is decoded by a corresponding one of the selector circuits 4a to 4k to the effect that either one transistor or two transistors of the first "m" output stage transistors Q11 to Qm1 connected to the drive output terminal T1 of the transistor switch circuit 3 is simultaneously turned on, and either one transistor or two transistors of the "k"th "m" output stage transistors Q1k to Qmk connected to the drive output terminal Tk is simultaneously turned on. With this arrangement, voltages V1, V2, . . . , Vm corresponding to drain voltage terminals 8a to 8m of "m" gray scale levels or their combined voltages are generated.

For example, assuming that the "(n+1)"-bit image input data Vi is composed of digital signals D0, D1, . . . , Dn, the voltage Vo appearing on the drive output terminal T1 is as shown in Figure 4.

Here, when the digital signals (D0, D1, . . . , Dn) = (0, 0, . . . , 0), only the output transistor Q11 is turned on by the associated selector circuit 4a, so that the output voltage V1 is outputted. When the digital signals (D0, D1, . . . , Dn) = (0, 0, . . . , 1), the output transistors Q11 and Q21 are simultaneously turned on by the associated selector circuit 4a. At this time, assuming that all the output transistors Q11 to Qmk have the same current driving capacity, the output voltage Vo becomes $V_o = (V_1 + V_2)/2$.

Namely, the output transistors are equally formed on the same silicon substrate, the characteristics of the output transistors Q11 to Qmk have only a little variation in a relative small zone within the same chip, even if it greatly varies from one manufacturing lot to another and from one wafer to another. Namely, the variation of the transistors is on the order of 10% at maximum. Therefore, it becomes $V_o \approx (V_1 + V_2)/2$, dependently upon a ratio in on-resistance ratio of the output transistors Q11 and Q21. Furthermore, in order to realize a multiple gray scale level in the liquid crystal display panel, the intervals of voltage steps is obtained by dividing the voltage of about 3 V to 4 V applied to the liquid crystal display, by the number

of required gray scale levels.

For example, if 16 gray scale levels are required, the voltage steps having the voltage intervals on the order of 0.25 V (= 4 V/16) are applied to the liquid crystal display panel. Accordingly, assuming that when the output transistors Q11 and Q21 are simultaneously turned on, a relative variation between the output transistors Q11 and Q21 is 10%, if $(V_1 - V_2) = 0.25$ V, the variation of the output voltage Vo is on the order of 25 mV. This is not so significant in an image displayed on the liquid crystal display panel.

Similarly, either one or two of each "m" transistors of the output transistors Q1k to Qmk are simultaneously turned on by the associated selector circuit 4k. Thus, (2m - 1) different output drive voltages can be obtained from the "m" different voltages Vm supplied from the voltage supply terminals 8a to 8m.

Incidentally, for convenience, the switching elements of the transistor switch circuit 3 have been composed of the transistors Q11 to Qmk. However, even if the transistors are replaced with transfer gates, the same effect can be obtained.

In the above mentioned liquid crystal device driving circuit, when the output transistors Q11 and Q21 are simultaneously turned on, since the output impedance of the output transistors Q11 and Qmk is on the order of about 10 K Ω to about 5 K Ω , the current flowing through each output becomes on the order of about 50 μ A to about 25 μ A (= 0.25 V/10K Ω to 0.25 V/5 K Ω). In an LCD driver LSI in which a driving circuit for the liquid crystal display panel is formed on a silicon substrate, in the case of the output number "k" = 192, the current becomes 4.8 mA to 9.6 mA, and therefore, the consumed electric power correspondingly becomes 1.2 mW to 2.4mW (= (4.8 mA to 9.6 mA) $\times$ 0.25 V). This value is almost no problem as the LCD driver LSI.

However, the liquid crystal panel uses at least 10 LCD driver LSIs each having the 192 outputs, and therefore, a voltage supply for the liquid crystal device driving circuit requires at least a current corresponding to the 10 LCD driver LSIs, namely, a current supplying capacity of 48mA to 96 mA. If the voltage supply is 20 V, there is required a large consumed electric power of 0.96 W to 1.92 W (= (48 mA to 96 mA) $\times$ 20 V).

Furthermore, the conventional liquid crystal device driving circuit can realize the (2m - 1) gray scale levels, by simultaneously turning on any two transistors of each "m" transistors of the output transistors Q1k to Qmk by action of the selector circuit 4k. However, if the potential difference between the simultaneously turned-on transistors is large, a very large current is required for the conventional liquid crystal device driving circuit, and

therefore, the consumed electric power correspondingly becomes large. This is not practical.

Summary of the Invention

Accordingly, it is an object of the present invention to provide a liquid crystal device driving circuit which has overcome the above mentioned defect of the conventional ones.

Another object of the present invention is to provide a driving circuit for a multiple gray scale liquid crystal device, with a reduced number of external voltage supplies and with a reduced consumed electric power.

The above and other objects of the present invention are achieved in accordance with the present invention by a liquid crystal display driving circuit comprising a plurality of switching means having their one end connected in common to a source line of a liquid crystal display panel and their other end connected to a plurality of driving voltages, respectively, for supplying a different voltage to the source line, and a control means receiving an image input data for selectively turning on the switching means, for the purpose of realizing a multiple gray scale display, the control means including means for turning on one switching means selected from the plurality of switching means during a first period of one display period, and for simultaneously turning on the one switching means or a plurality of switching means selected from the plurality of switching means during a second period of one display period.

The above and other objects, features and advantages of the present invention will be apparent from the following description of preferred embodiments of the invention with reference to the accompanying drawings.

Brief Description of the Drawings

Figure 1 is a block diagram showing one example of a conventional liquid crystal device driving circuit;

Figure 2 is a table showing the relation between the image input data, the driving output voltage and the switching transistors in the circuit shown in Figure 1;

Figure 3 is a block diagram of another liquid crystal display driving circuit,

Figure 4 is a table showing the relation between the image input data, the driving output voltage and the switching transistors in the circuit shown in Figure 3;

Figure 5 is a block diagram of one embodiment of the liquid crystal device driving circuit in accordance with the present invention;

Figure 6 is a detailed circuit diagram of the output circuit shown in the liquid crystal device driving circuit shown in Figure 5;

Figure 7 is a table showing the relation between the input image data and the output voltage in the liquid crystal device driving circuit shown in Figure 5;

Figure 8 is a timing chart illustrating an operation of the liquid crystal device driving circuit shown in Figure 5;

Figure 9 is a block diagram of a second embodiment of the liquid crystal device driving circuit in accordance with the present invention;

Figure 10 is a detailed circuit diagram of the output circuit included in the liquid crystal device driving circuit shown in Figure 9;

Figure 11 is a circuit diagram illustrating one example of a transfer gate;

Figure 12 is a detailed block diagram showing the selector circuit in the liquid crystal device driving circuit shown in Figure 9;

Figure 13 is a logic diagram showing a specific circuit of the control circuit included in the selector circuit shown in Figure 12;

Figure 14 is a truth table showing the relation between the inputs and the outputs of the control circuit shown in Figure 13;

Figures 15, 16, 17 and 18 are equivalent circuits showing various conditions of the output circuit included in the liquid crystal device driving circuit shown in Figure 9; and

Figures 19 and 20 are tables for illustrating operation of the liquid crystal device driving circuit shown in Figure 9.

Description of the Preferred embodiments

Now, embodiments of the present invention will be described with reference to the drawings.

Referring to Figure 5, there is shown a block diagram of one embodiment of the liquid crystal device driving circuit in accordance with the present invention. As one example, the shown embodiment is configured to receive image data of 5 bits (D_{M3} , D_{M2} , D_{M1} , D_{M0} , D_{H0}) and to generate driving voltages of $2^5 = 32$ gray scale levels. In addition, the most significant bit of the 5-bit image data is labelled " D_{M3} ", and the least significant bit of the 8-bit image data is labelled " D_{H0} ". For convenience of description, the bits " D_{M3} " to " D_{M0} " of the 5-bit image data are called "main bits", and the bit " D_{H0} " of the 5-bit image data is called a "sub (interpolating) bit".

The shown drive circuit includes "k" stages of 5-bit shift registers 20a to 20k receiving an image input data from an image data input terminal 7, a corresponding number of 5-bit latches 21a to 21k each for latching the 5-bit data of a corresponding

one of the 5-bit shift registers 20a to 20k, external gray scale level voltages V_{R0} , V_{R1} , $\dots$, V_{R16} corresponding to 16 gray scale levels, a corresponding number of output circuits 22a to 22k each generating an intermediate voltage between each pair of adjacent voltages of the gray scale level voltages V_{R0} , V_{R1} , $\dots$, V_{R16} on the basis of the interpolating bit "D_{H0}", and a corresponding number of AND gates ANDa to ANDk for controlling the output of the interpolating bit "D_{H0}" from the 5-bit latches 21a to 21k to the output circuits 22a to 22k on the basis of an output voltage interpolating input Vh.

Figure 6 shows a circuit diagram of the output circuits 22a to 22k. Each of the output circuits 22a to 22k includes a decoder 24 receiving the main bits "D_{M3}" to "D_{M0}" of 4 bits for activating one selection signal, transfer gates TG₀ to TG₁₆ connected to the external gray scale level voltages V_{R0} , V_{R1} , $\dots$, V_{R16} , respectively, and control circuits SE₀ to SE₁₆ each receiving the interpolating bit "D_{H0}" and a corresponding one of outputs O_{M0} to O_{M16} of the decoder 24 for controlling a corresponding one of the transfer gates. Each of the control circuits SE₀ to SE₁₆ is formed of one AND gate and one OR gate connected as shown.

The 5-bit image input data D_{M3} to D_{M0} and D_{H0} is supplied through the image input terminal 7, and transferred through the 5-bit shift registers 20a to 20k in response to the clock pulse Vc. In response to the latch pulse Vr, the image input data in the 5-bit shift registers 20a to 20k is transferred and latched in the 5-bit latches 21a to 21k. The main bits D_{M3} to D_{M0} of the data latched in each latch is supplied to the decoder 24 of a corresponding output circuit 22a to 22k, so that an active selection pulse is outputted from one of the outputs O_{M0} to O_{M16} of the decoder in accordance with the content of the main bits D_{M3} to D_{M0}, as shown in Figure 7. In Figure 7, the label "ON" shows an active condition, and the label "OFF" indicates an inactive condition.

Namely, if (D_{M3}, $\dots$, D_{M0}) = (0, 0, 0, 0), the output O_{M0} is "ON" (active), and if (D_{M3}, $\dots$, D_{M0}) = (0, 0, 0, 1), the output O_{M1} is "ON" (active). If (D_{M3}, $\dots$, D_{M0}) = (1, 1, 1, 1), the output O_{M15} is "ON" (active).

In addition, the sub bit D_{H0} of the data latched in each latch is supplied through the AND gates ANDa to ANDk to the control circuits SE₀ to SE₁₆ of each output circuit 22a to 22k when the output voltage interpolating input Vh is "1" (high level). When the sub bit D_{H0} is "0", the control circuits SE₀ to SE₁₆ output the signals received from the outputs O_{M0} to O_{M16} of the decoder, without modification. Namely, only any one of the transfer gates TG₀ to TG₁₆ is turned on in accordance with the content of the main bits D_{M3} to D_{M0}, so that one of

the gray scale level voltages V_{R0} to V_{R16} connected to the transfer gates TG₀ to TG₁₆, respectively, is selected and outputted to an output terminals OUT (T₁ to T_k).

On the other hand, when the sub bit D_{H0} is "1", the control circuits SE_n and SE_(n+1) are selected by an active output signal OM_n of the decoder 24, so that the transfer gates TG_n and TG_(n+1) are simultaneously selected. As a result, an intermediate voltage between the gray scale level voltage V_{Rn} connected to the transfer gates TG_n and the gray scale level voltages $V_{R(n+1)}$ connected to the transfer gate TG_(n+1) is generated at the output terminal T₁ to T_k of the output circuits 22a to 22k.

Here, assuming that the all the transfer gates TG₀ to TG₁₆ are constructed to have the same structure and the same on-resistance, the output voltage becomes $\{V_{Rn} + V_{R(n+1)}\}/2$. The function explained until here is completely the same as that of the conventional liquid crystal device driving circuit. Here, the relation between the input image data and the output voltage is as shown in Figure 7.

Here, when the output voltage interpolating input Vh is "0", the output of the AND gates ANDa to ANDk becomes "0", and therefore, only one transfer gate is selected in accordance with the content of the main bits D_{M3} to D_{M0}. On the other hand, when the output voltage interpolating input Vh is "1", if the sub bit D_{H0} is "0", one transfer gate is selected in accordance with the content of the main bits D_{M3} to D_{M0}, similarly to the case of Vh = "0". However, if the sub bit D_{H0} is "1", a gray scale voltage near to an intermediate voltage between a pair of adjacent gray scale voltage supply voltages is selected as mentioned above.

Furthermore, an operation of the embodiment of the liquid crystal device driving circuit will be described with reference to the timing chart of Figure 8. In an active matrix type liquid crystal display panel, a voltage supplied from a source side liquid crystal device driving circuit is charged through a wiring conductor on the liquid crystal display panel, to a thin film transistor associated to a corresponding pixel on the liquid crystal display panel, during one horizontal scan period T₀.

For example, if the data latched in the 5-bit latches 21a to 21k in response to the latch pulse Vr is (D_{M3}, D_{M2}, D_{M1}, D_{M0}, D_{H0}) = (0, 0, 0, 0, 1), when the output voltage interpolating input Vh is "0", the transfer gate TG₀ is selected in accordance with Figure 7, so that V₀ is outputted, and the display panel is charged V₀ during a first partial period T₁ of the horizontal scan period T₀.

Next, when the output voltage interpolating input Vh becomes "1", the transfer gates TG₀ and TG₁ are selected in accordance with Figure 7, so that the voltage of $(V_0 + V_1)/2$ is outputted, and

the display panel is charged from V_0 to $(V_0 + V_1)/2$ during a second and final partial period T_2 of the horizontal scan period T_0 . In this case, assuming that the voltage before the charging is V_{16} , the voltage is required to change over a full swing range between V_0 and V_{16} , and therefore, a sufficient time period T_1 is required to change over the full swing range. During the time period T_2 , it is sufficient if the voltage changes only from V_0 to $(V_0 + V_1)/2$, namely, over $1/32$ of the full swing range. Accordingly, the time period T_2 can be sufficiently shortened in comparison with the times T_0 and T_1 .

For example, it is assumed that the time constant for charging the liquid crystal display panel is $T_0/6$. Also assuming that the full swing range is 5 V, an error rate of the charged voltage in the charging over the period T_0 is about 0.3%, namely 15mV. Here, if the voltage interval of one gray scale level, namely $5 V/32 (=0.15 V)$ is charged during a period $T_0/3$ under the same charging time constant, the error rate of the charged voltage is about 13%, namely, about 20 mV. Accordingly, the time period T_1 and T_2 can be made to $2T_0/3$ and $T_0/3$, respectively.

In the above mentioned operation, the period in which two transfer gates of the transfer gates TG_0 to TG_{16} are simultaneously in the on condition, is the period T_2 . Accordingly, the time period in which the two transfer gates are simultaneously turned on so that the current flows through the gray scale level voltage supplies and therefore the electric power is consumed, is shortened to $1/3$. If the time constant for charging the liquid crystal display panel is extremely smaller than the time period T_0 , or if the number of gray scale levels is increased so as to make the voltage interval of each one gray scale level further small, the period of T_2 can be further made small, and therefore, the averaged current of the gray scale level voltage supplies can correspondingly further be reduced.

Incidentally, it is a matter of course that when the sub bit D_{H0} is "0", no current flows through the gray scale level voltage supplies. It is sufficient if the output voltage interpolating input V_h is optimized in match with the characteristics of the liquid crystal display panel.

Now, referring to Figure 9, explanation will be made on a second embodiment of the liquid crystal device driving circuit in accordance with the present invention, which is configured to reduce the current of the gray scale level voltage supplies in accordance with the principle of the first embodiment, and which can obtain a multiple gray scale increased by one bit, with the same number of external gray scale level voltage supplies. Namely, the image input data is increased from 5 bits to 6 bits, and the gray scale levels of $2^6 = 64$ are gen-

erated with the same number (17) of external gray scale level voltage supplies.

Similarly to the first embodiment, the four most significant bits D_{M3} to D_{M0} of the 6-bit image input data are called the "main bits", and the two least significant bits D_{H1} to D_{H0} of the 6-bit image input data are called the "sub bits".

The shown drive circuit includes "k" stages of 6-bit shift registers 28a to 28k receiving an image input data from an image data input terminal 7, a corresponding number of 6-bit latches 29a to 29k each for latching the 6-bit data of a corresponding one of the 6-bit shift registers 28a to 28k, and a number of AND gates AND1a to AND1k and AND0a to AND0k for controlling the output of the interpolating bits on the basis of an output voltage interpolating input V_h , and a number of output circuits 26a to 26k each receiving external gray scale level voltages V_{R0} , V_{R1} , ..., V_{R16} for generating voltages of 64 gray scale levels.

Each of the output circuits 26a to 26k has a construction as shown in Figure 10. Each gray scale level voltages V_{Rn} is connected to one end of a main transfer gate TGMn and one end of a sub transfer gate TGHn in parallel, and the other end of all the transfer gates are connected in common to an output terminal OUT (T_1 to T_k). Figure 11 shows an detailed logic circuit of the transfer gate used as the main transfer gate TGMn and the sub transfer gate TGHn. One N-channel transistor NMOS and a P-channel transistor PMOS are connected in parallel to each other between an input "I" and an output "O", and a gate signal G is supplied to a gate of the N-channel transistor NMOS and through an inverter INV to a gate of the P-channel transistor PMOS. Thus, when the gate signal G is at a high level, both of the N-channel transistor NMOS and the P-channel transistor PMOS are turned on, namely, the transfer gate is turned on. When the gate signal G is at a low level, both of the N-channel transistor NMOS and the P-channel transistor PMOS are turned off, namely, the transfer gate is turned off.

The main transfer gates TGM_0 to TGM_{16} and the sub transfer gates TGH_0 to TGH_{16} are on-off controlled by a selector circuit 25. Figure 12 shows a detailed block diagram of the selector circuit 25. The selector circuit 25 includes a decoder 24 receiving the main bits D_{M3} to D_{M0} for generating 16 selection signals OM_{15} to OM_0 , similarly to the first embodiment, and control circuits SEL_0 to SEL_{16} which correspond to the control circuits SE_0 to SE_{16} of the first embodiment, but which receive the sub bits D_{H1} and D_{H0} . A specific circuit of each of the control circuits SEL_0 to SEL_{16} which is shown in Figure 13, and its truth table is shown in Figure 14. Each of the control circuits SEL_0 to SEL_{16} includes three OR gates OR_1 , OR_2 and OR_3 , three

AND gates AND_1 , AND_2 and AND_3 and one NAND gate $NAND_1$, connected as shown in Figure 13.

First, operation of the output circuits 26a to 26k will be described. All the main transfer gates TGM_0 to TGM_{16} and all the sub transfer gates TGH_0 to TGH_{16} have the same on-resistance, respectively. For example, this can be realized if all the transfer gates has the same construction and the same size when the liquid crystal device driving circuit is implemented on a silicon substrate.

A ratio between the on-resistance of the main transfer gates TGM_0 to TGM_{16} and the on-resistance of the sub transfer gates TGH_0 to TGH_{16} is set to be 1 : 2. At this time, if the sub bits $(D_{H1}, D_{H0}) = (0, 0)$, the output TGH_n of the control circuits SEL_0 to SEL_{16} are "0", and the output TGM_n is M_n , as will be understood from the truth table of Figure 14. Therefore, only one transfer gate TGM_n selected in accordance with the content of the main bits D_{M3} to D_{M0} is selected, so that V_n is outputted from the output OUT. An equivalent circuit of the output circuit in this condition is shown in Figure 15. In Figure 15 and in succeeding Figures 16 to 18, the resistance value "R" shows the on-resistance of the main transfer gates TGM_0 to TGM_{16} and the resistance value "2R" shows the on-resistance of the sub transfer gates TGH_0 to TGH_{16} .

Next, function of the sub bits D_{H1} and D_{H0} will be described. Firstly, assume that the output OM_n of the decoder 24 is selected or activated in accordance with the content of the main bits D_{M3} to D_{M0} . At this time, if the sub bits $(D_{H1}, D_{H0}) = (0, 1)$, the outputs TGM_n and TGH_n of the control circuit SEL_n are selected, and also, the output $TGH_{(n+1)}$ of the control circuit $SEL_{(n+1)}$ is selected, as will be understood from the truth table of Figure 14. At this time, an equivalent circuit of the output circuit becomes as shown in Figure 16. Namely, the output voltage of $\{3V_n + V_{(n+1)}\} / 4$ is outputted.

If the sub bits $(D_{H1}, D_{H0}) = (1, 0)$, the outputs TGM_n and TGH_n of the control circuit SEL_n are selected, and also, the outputs $TGM_{(n+1)}$ and $TGH_{(n+1)}$ of the control circuit $SEL_{(n+1)}$ are selected, as will be understood from the truth table of Figure 14. In this condition, an equivalent circuit of the output circuit becomes as shown in Figure 17. Namely, the output voltage of $\{V_n + V_{(n+1)}\} / 2$ is outputted.

If the sub bits $(D_{H1}, D_{H0}) = (1, 1)$, the output TGH_n of the control circuit SEL_n is selected, and also, the outputs $TGM_{(n+1)}$ and $TGH_{(n+1)}$ of the control circuit $SEL_{(n+1)}$ are selected, as will be understood from the truth table of Figure 14. At this time, an equivalent circuit of the output circuit becomes as shown in Figure 18. Namely, the output voltage of $\{V_n + 3V_{(n+1)}\} / 4$ is outputted.

As mentioned above, a multiple of different voltages can be generated by connecting the main

transfer gates TGM_0 to TGM_{16} and the sub transfer gates TGH_0 to TGH_{16} in parallel to the gray scale level voltage supplies, and by turning on these transfer gates in various different combinations.

Now, the overall operation of the second embodiment of the liquid crystal device driving circuit will be described. Similarly to the first embodiment, the image input data D_{M3} to D_{M0} and D_{H1} and D_{H0} are transferred through the 6-bit shift registers 28a to 28k, and then latched into the 6-bit latches 29a to 29k in response to the latch pulse V_r . In addition, the AND gates AND_{0a} to AND_{0k} and AND_{1a} to AND_{1k} are controlled by the output voltage interpolating input V_h , so as to control application of the sub bits D_{H1} and D_{H0} to the output circuit. Thus, the relation between the image data and the output voltage as shown in the tables of Figures 19 and 20 can be obtained. Accordingly, operation similarly to the first embodiment can be preformed, and the averaged current flowing through the gray scale level voltage supplied can be effectively reduced. On the other hand, if the number of the transfer gates is increased, it is possible to increase the number of gray scale level voltages.

The invention has thus been shown and described with reference to the specific embodiments. However, it should be noted that the present invention is in no way limited to the details of the illustrated structures but changes and modifications may be made.

Claims

1. A liquid crystal display driving circuit comprising a plurality of switching means having their one end connected in common to a source line of a liquid crystal display panel and their other end connected to a plurality of driving voltages, respectively, for supplying a different voltage to said source line, and a control means receiving an image input data for selectively turning on said switching means, for the purpose of realizing a multiple gray scale display, the control means including means for turning on one switching means selected from said plurality of switching means during a first period of one display period, and for simultaneously turning on said one switching means or a plurality of switching means selected from said plurality of switching means during a second period of one display period.
2. A liquid crystal display driving circuit comprising a plurality of switching means having their one end connected in common to a source line of a liquid crystal display panel and their other end connected to a plurality of driving voltages, respectively, for supplying a different

voltage to said source line, and a control means receiving an image input data for selectively turning on said switching means, for the purpose of realizing a multiple gray scale display, the control means including selection means for selecting one or a plurality of switching means to be simultaneously turned on from said plurality of switching means, and timing control means for maintaining said one switching means in an on condition during one display period when said one switching means is selected by said selection means, said timing control means operating, when said plurality of switching means are selected by said selection means, to turn on one of said plurality of selected switching means during a first period of one display period, and then to simultaneously turn on said plurality of switching means during a second period of one display period.

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3. A liquid crystal display driving circuit claimed in Claim 2 wherein each of said switching means includes a plurality of switching elements, and wherein when said plurality of switching means are selected by said selection means, said control means controls on the basis of the image input data, a combination of switching elements to be turned on included in said plurality of selected switching means.

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4. A liquid crystal display driving circuit comprising a plurality of transfer gates having their one end connected in common to a source line of a liquid crystal display panel and their other end connected to a plurality of driving voltages, respectively, for supplying a different voltage to the source line, and A control circuit receiving an image input data for selectively turning on the transfer gates, for the purpose of realizing a multiple gray scale display, said control circuit being configured to turn on one transfer gate selected from the plurality of transfer gates during a first period of one display period, and then, to maintain the turned-on condition of the selected transfer gate during the remaining period of one display period, or to simultaneously turn on at least two transfer gates which are selected from the plurality of transfer gates and which include the selected transfer gate during the remaining period of one display period.

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FIGURE 1
PRIOR ART

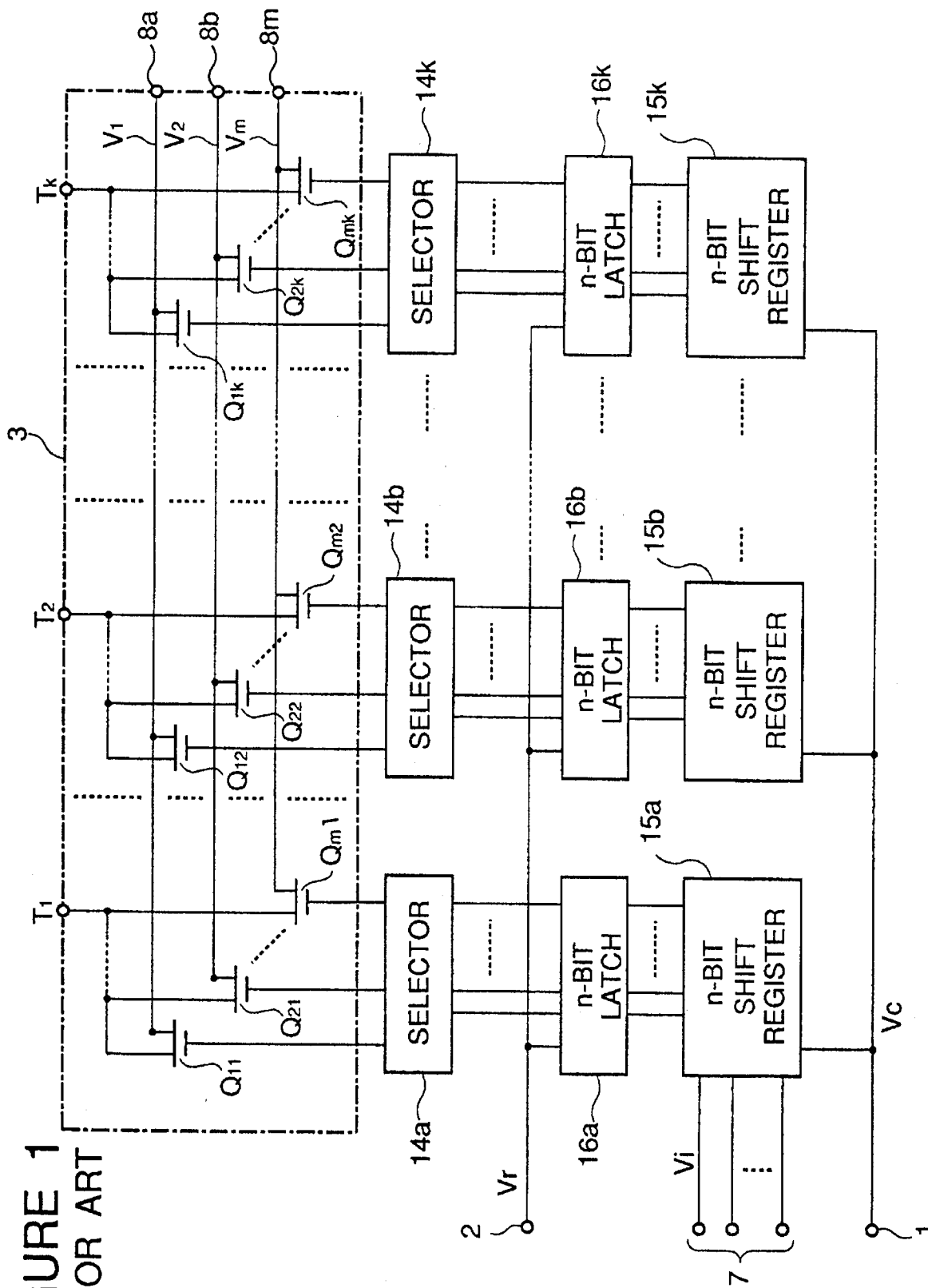


FIGURE 2 PRIOR ART

IMAGE INPUT DATA V_i				DRIVE OUTPUT VOLTAGE V_0	TURNED-ON OUTPUT TRANSISTOR
D_{n-1}		D_1	D_0		
0		0	0	V_1	Q_{11}
0		0	1	V_2	Q_{21}
0		1	0	V_3	Q_{31}
0		1	1	V_4	Q_{41}
⋮		⋮	⋮	⋮	⋮
1		1	1	V_m	Q_{m1}

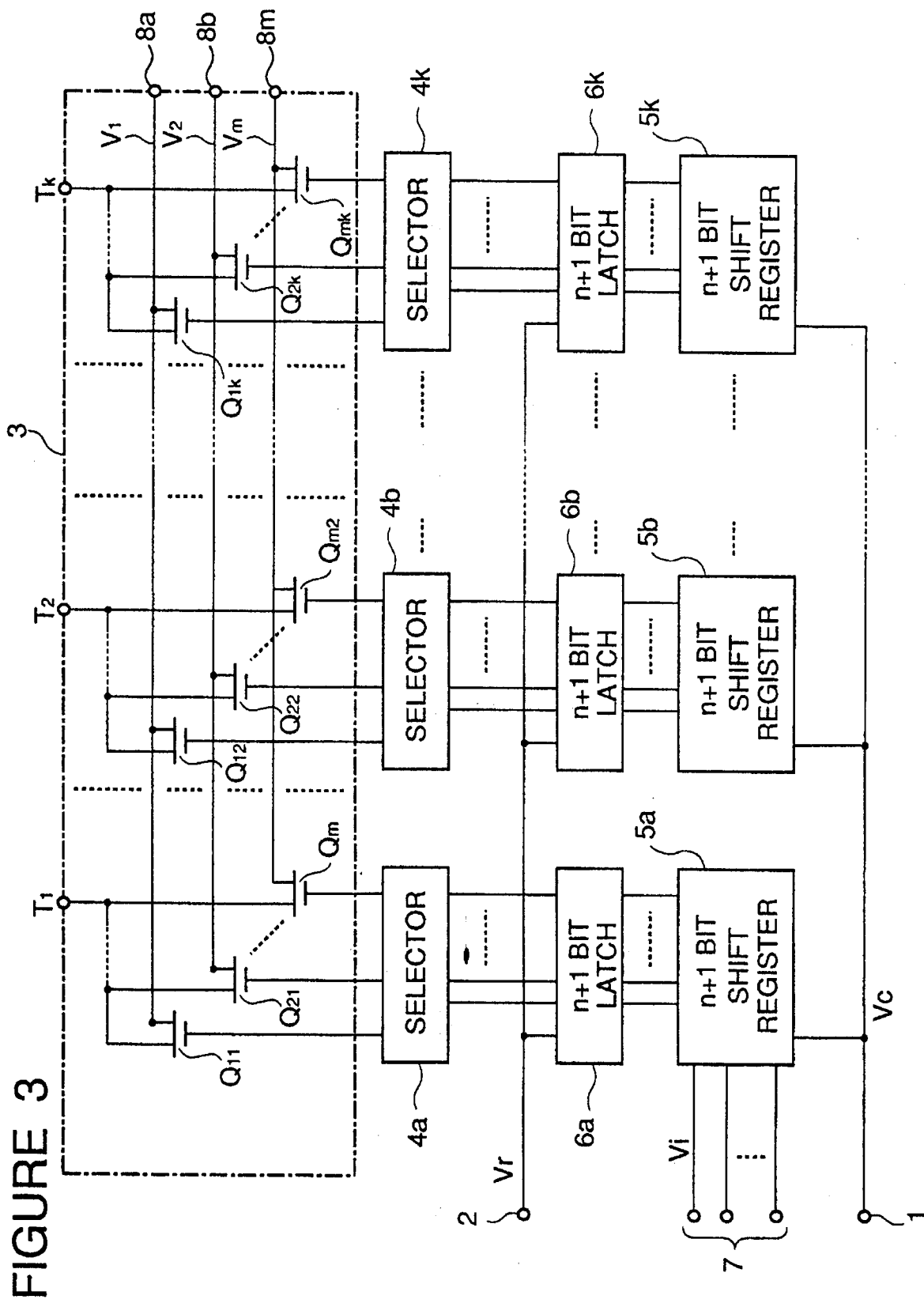


FIGURE 4

IMAGE INPUT DATA V_i				DRIVE OUTPUT VOLTAGE V_0	TURNED-ON OUTPUT TRANSISTOR
D_{n-1}		D_1	D_0		
0		0	0	V_1	Q_{11}
0		0	1	$\approx \frac{V_1+V_2}{2}$	Q_{11} AND Q_{21}
0		1	0	V_2	Q_{21}
0		1	1	$\approx \frac{V_2+V_3}{2}$	Q_{21} AND Q_{31}
				V_3	Q_{31}
⋮		⋮	⋮	⋮	⋮
1		0	1	$\approx \frac{V_{m+1}+V_m}{2}$	Q_{m-1} AND Q_m
1		1	0	V_m	Q_m

FIGURE 5

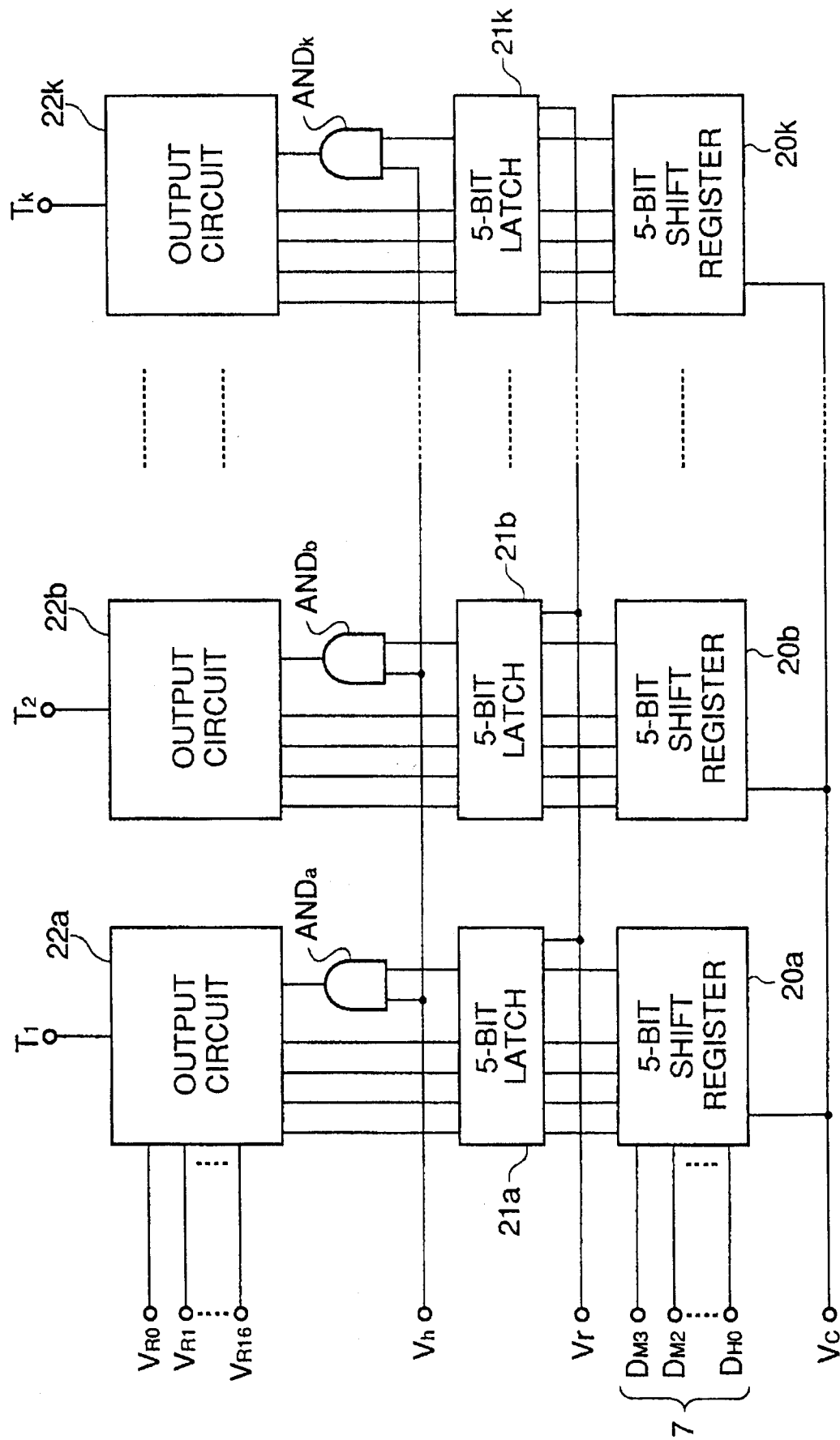


FIGURE 6

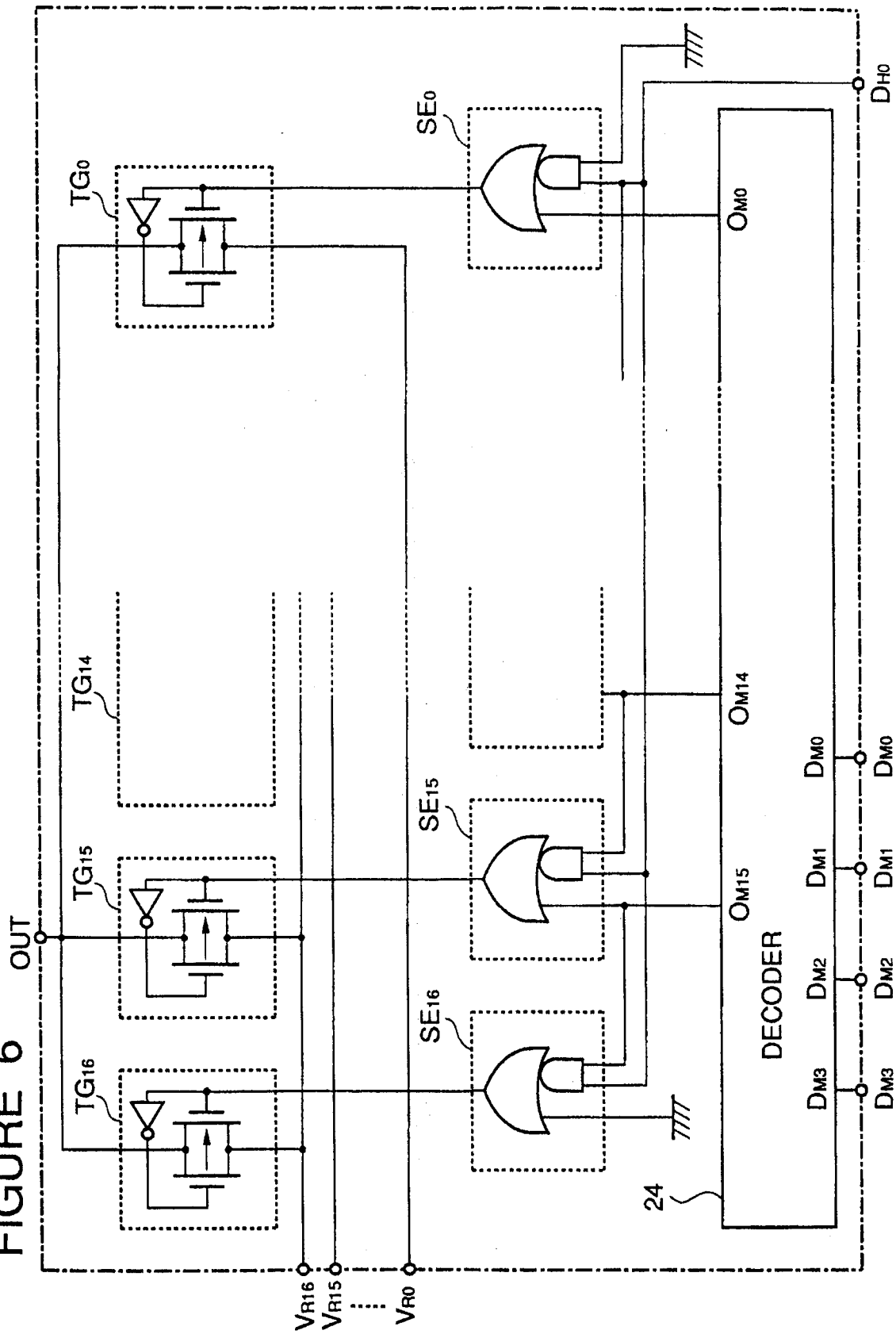


FIGURE 7

OUTPUT VOLTAGE	IMAGE INPUT DATA					STATUS OF TRANSFER GATE								OUTPUT OF DECODER			
	MAIN BIT				SUB BIT												
	D _{M3}	D _{M2}	D _{M1}	D _{M0}		D _{H0}	TGM ₁₆	TGM ₁₅	TGM ₁₄	TGM ₂	TGM ₁	TGM ₀	OM ₁₅	OM ₁₄	OM ₁	OM ₀	
V ₀	0	0	0	0	0	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON		
$\frac{V_0+V_1}{2}$	0	0	0	0	1					ON	↓			↓	↓		
V ₁	0	0	0	1	0				↓		OFF			OFF	OFF		
$\frac{V_1+V_2}{2}$	0	0	0	1	1				ON	↓				↓	↓		
V ₂	0	0	1	0	0				↓	OFF	↓			OFF	↓		
V ₁₄	1	1	1	0	1	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF		
$\frac{V_{14}+V_{15}}{2}$	1	1	1	0	0		ON	↓				↓	↓		↓		
V ₁₅	1	1	1	1	0			OFF				ON	OFF		↓		
$\frac{V_{15}+V_{16}}{2}$	1	1	1	1	1	ON		↓				↓	↓	↓	↓		

FIGURE 8

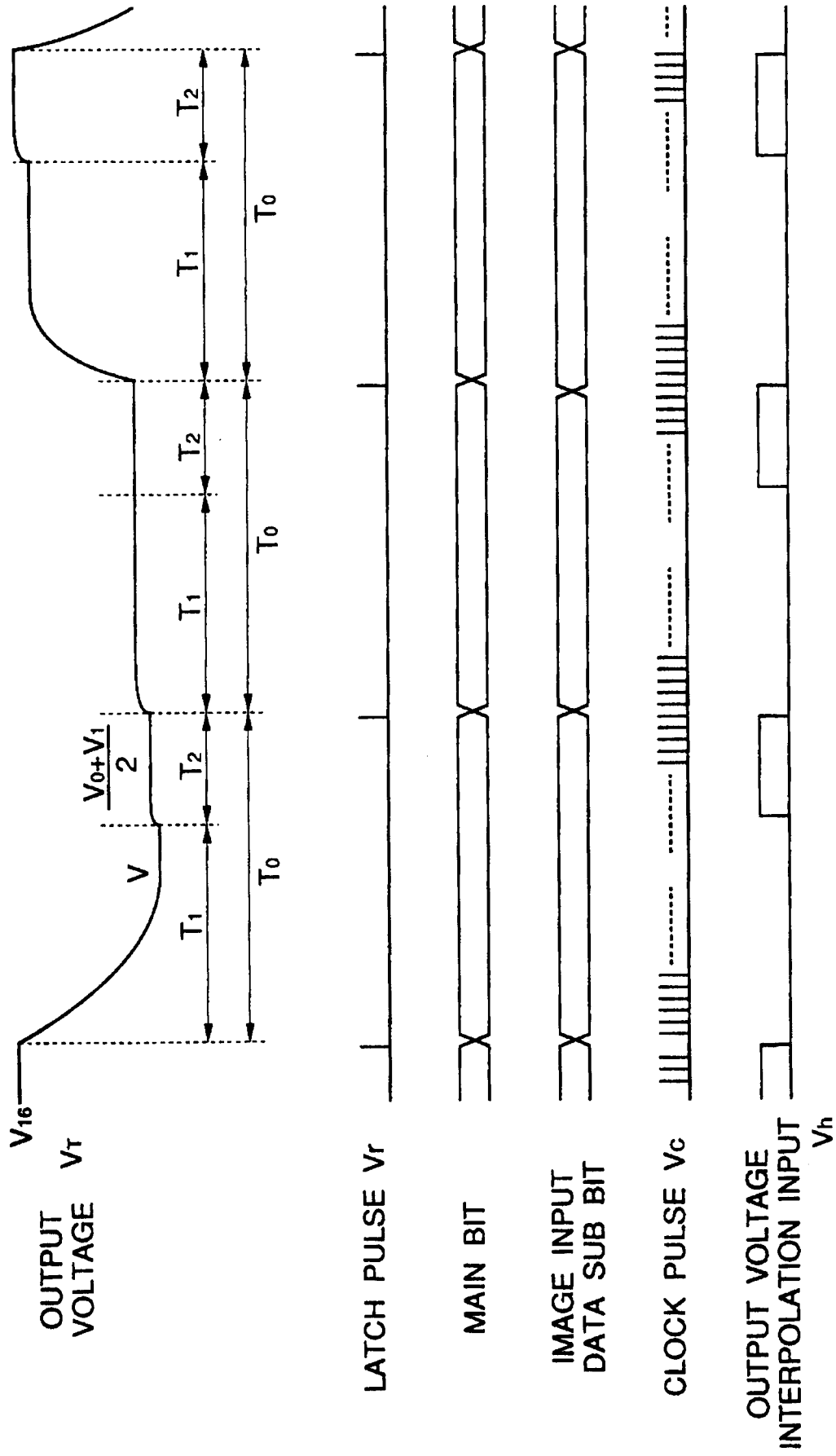


FIGURE 9

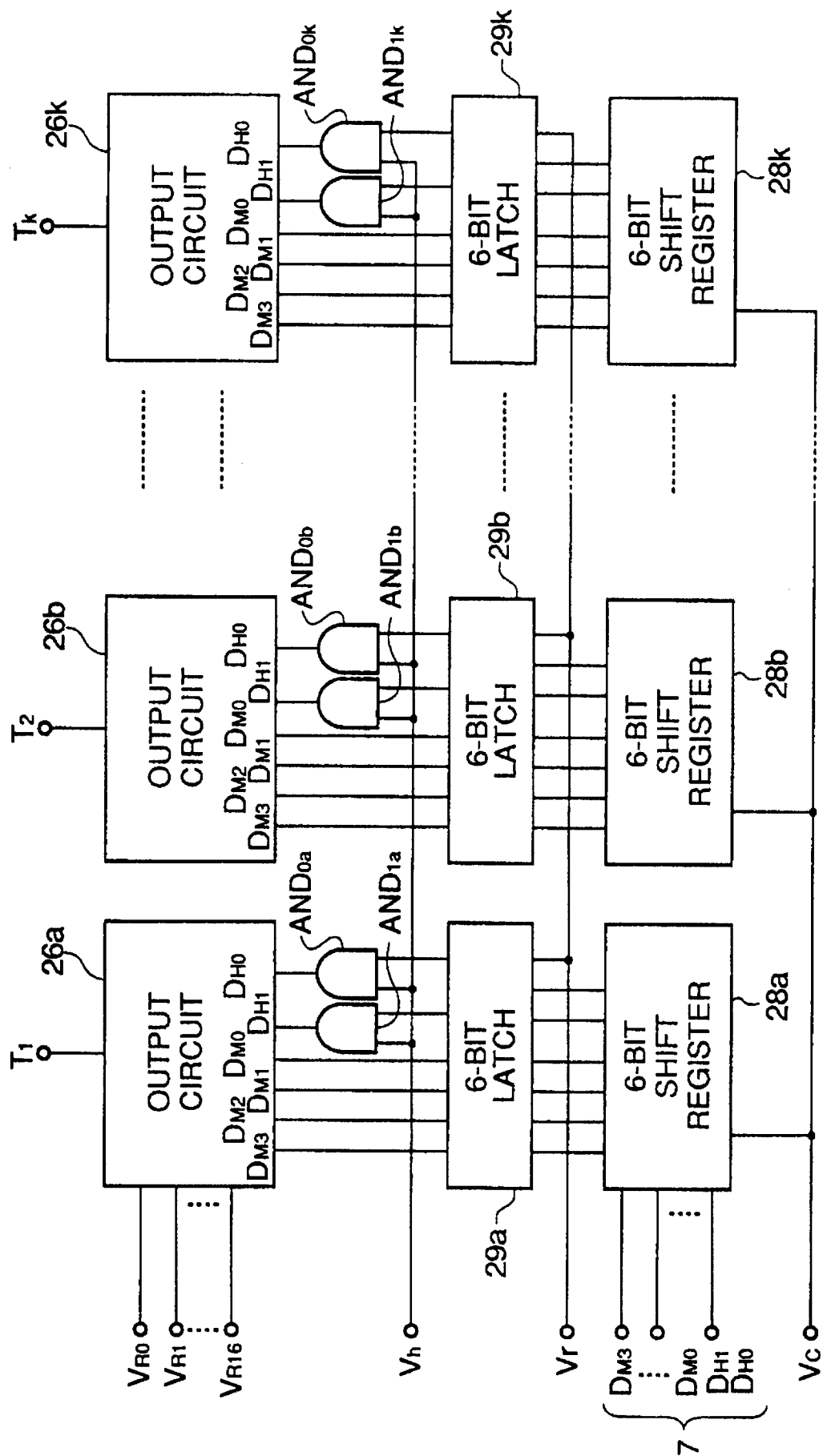


FIGURE 10

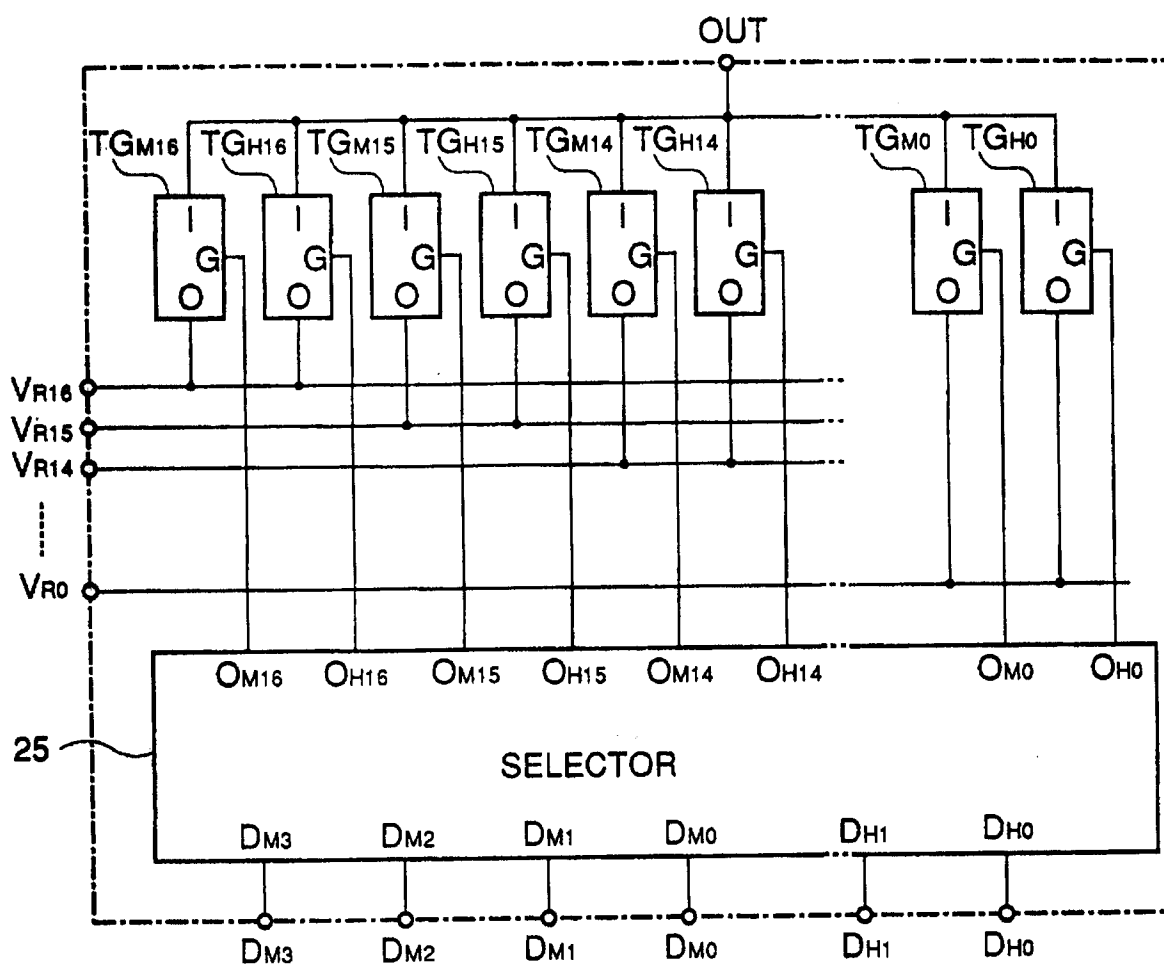


FIGURE 11

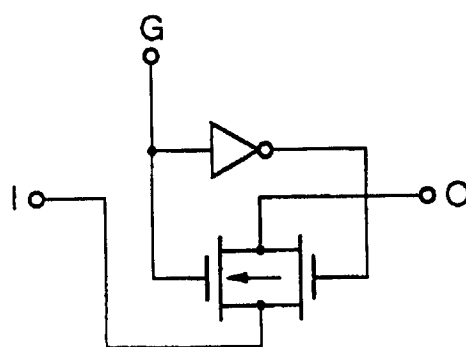


FIGURE 12

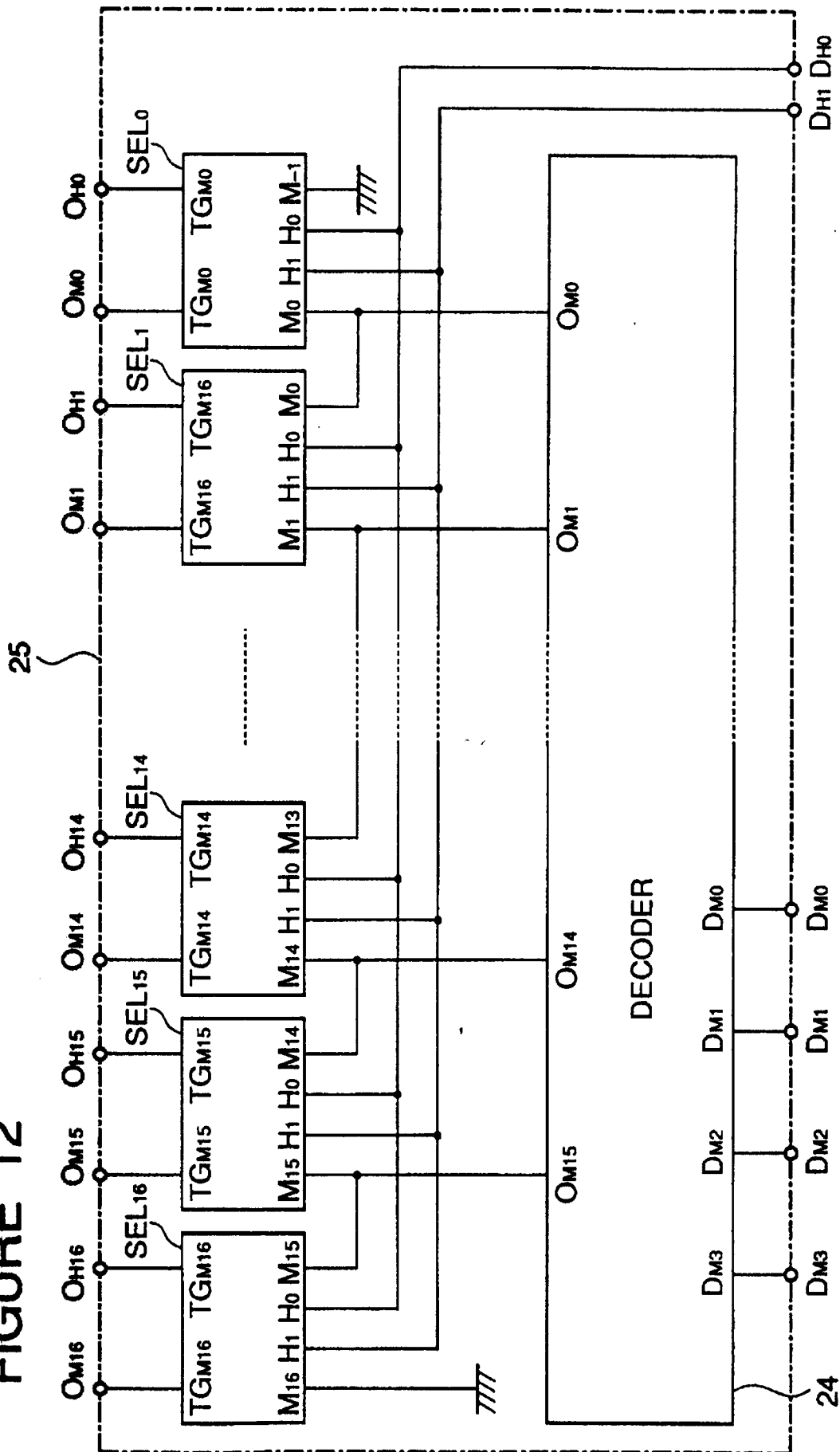


FIGURE 13

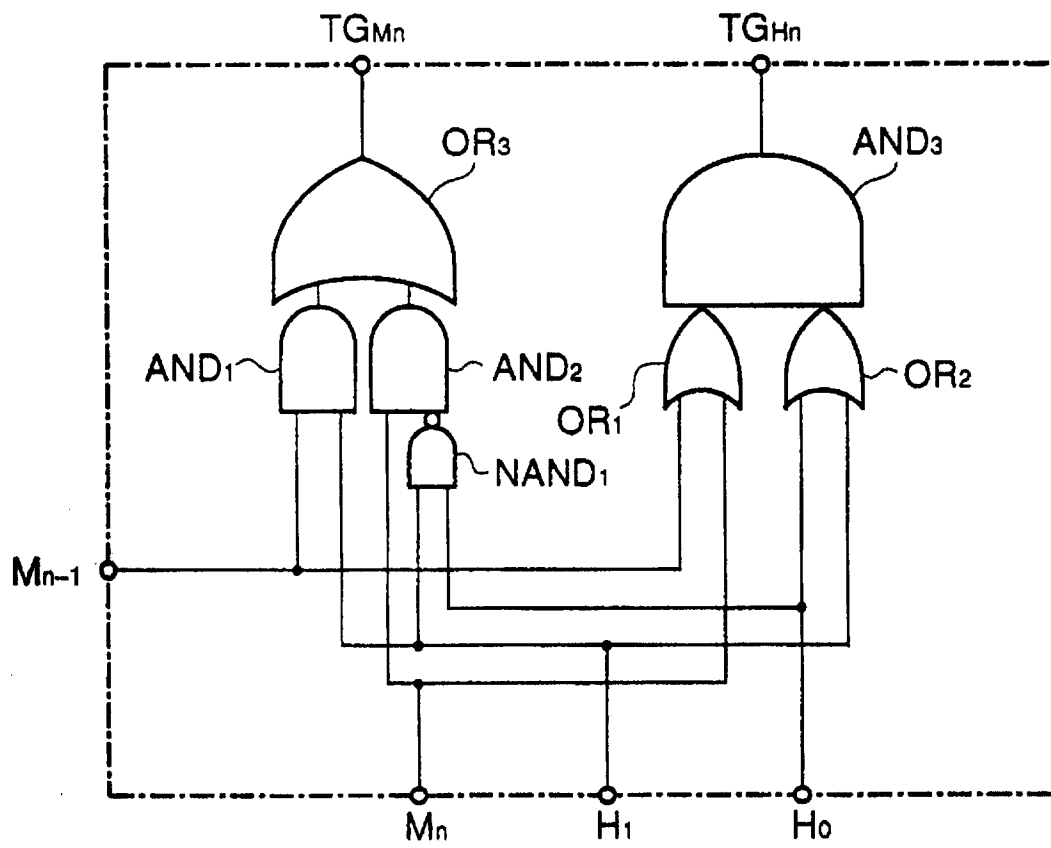


FIGURE 14

INPUT				OUTPUT	
H_1	H_0	M_n	M_{n-1}	TG_{Mn}	TG_{Hn}
0 ↓	0 ↓	0	0	0	0
		0	1	0	0
		1	0	1	0
		1	1	1	0
0 ↓	1 ↓	0	0	0	0
		0	1	0	1
		1	0	1	1
		1	1	1	1
1 ↓	0 ↓	0	0	0	0
		0	1	1	1
		1	0	1	1
		1	1	1	1
1 ↓	1 ↓	0	0	0	0
		0	1	1	1
		1	0	0	1
		1	1	1	1

FIGURE 15

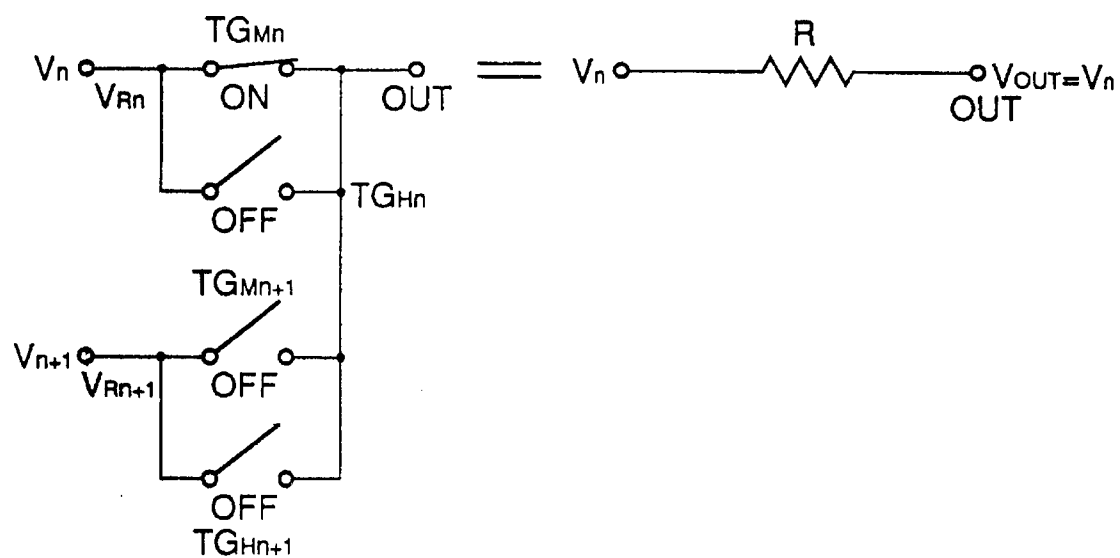


FIGURE 16

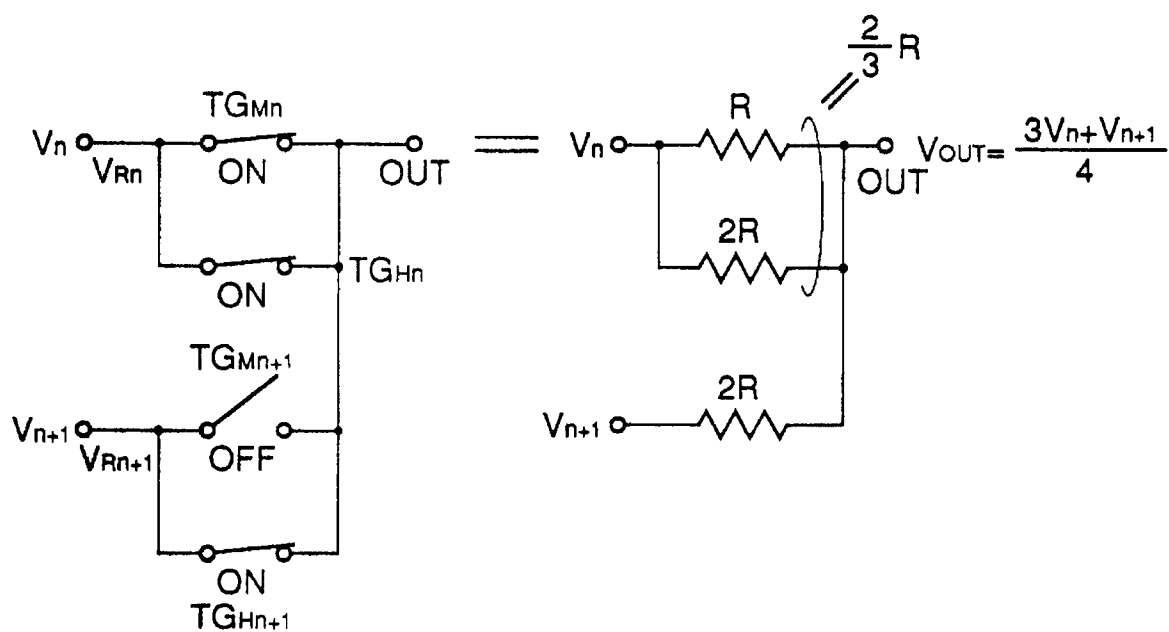


FIGURE 17

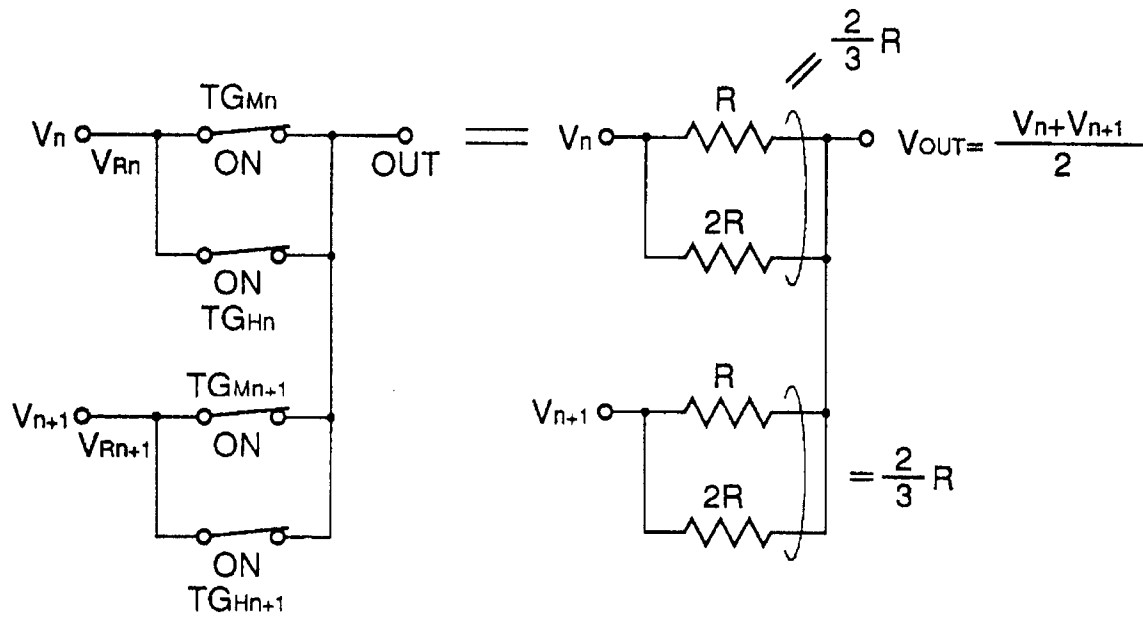


FIGURE 18

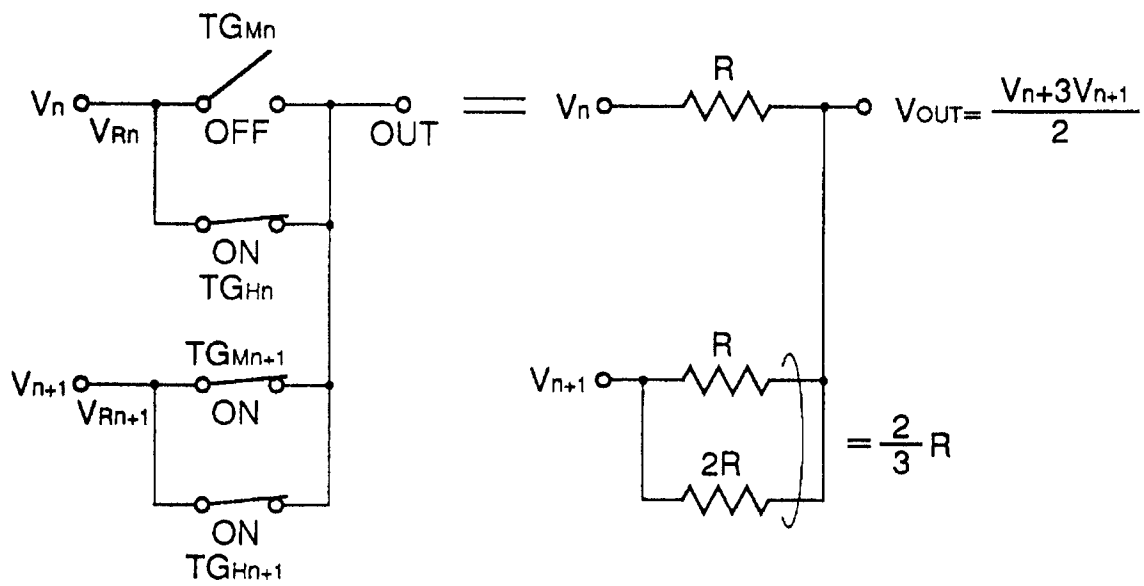


FIGURE 19

OUTPUT VOLTAGE	IMAGE INPUT DATA							STATUS OF TRANSFER GATE									
	MAIN BIT				SUB BIT			MAIN TRANSFER GATE					SUB TRANSFER GATE				
	D _{M3}	D _{M2}	D _{M1}	D _{M0}	D _{H1}	D _{H0}		TG _{M16}	TG _{M15}	TG _{M2}	TG _{M1}	TG _{M0}	TG _{H16}	TG _{H15}	TG _{H2}	TG _{H1}	TG _{H0}
V_0	0	0	0	0	0	0		OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF
$\frac{3V_0+V_1}{4}$	0	0	0	0	0	1					↓					ON	ON
$\frac{V_0+V_1}{2}$	0	0	0	0	1	0					ON	↓					
$\frac{V_0+3V_1}{4}$	0	0	0	0	1	1			↓	↓	↓	OFF		↓	↓	↓	↓
V_1	0	0	0	1	0	0		OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF
$\frac{3V_1+V_2}{4}$	0	0	0	1	0	1				↓					ON	ON	
$\frac{V_1+V_2}{2}$	0	0	0	1	1	0				ON	↓						
$\frac{V_1+3V_2}{4}$	0	0	0	1	1	1			↓	↓	OFF	↓		↓	↓	↓	↓

FIGURE 20

OUTPUT VOLTAGE	IMAGE INPUT DATA						STATUS OF TRANSFER GATE											
	MAIN BIT				SUB BIT		MAIN TRANSFER GATE				SUB TRANSFER GATE							
	D _{M3}	D _{M2}	D _{M1}	D _{M0}	D _{H1}	D _{H0}	T _{GM16}	T _{GM15}	T _{GM2}	T _{GM1}	T _{GM0}	T _{GH16}	T _{GH15}	T _{GH2}	T _{GH1}	T _{GH0}		
V ₂	0	0	1	0	0	0	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF		
$\frac{3V_2+V_3}{4}$	0	0	1	0	0	1								ON				
$\frac{V_2+V_3}{2}$	0	0	1	0	1	0			↓									
$\frac{V_2+3V_3}{4}$	0	0	1	0	1	1		↓	OFF	↓	↓	↓	↓	↓	↓	↓		
V ₃	0	0	1	1	0	0	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF		
V ₁₅	1	0	0	0	0	0	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF		
$\frac{3V_{15}+V_{16}}{4}$	1	0	0	0	0	1	↓					ON	ON					
$\frac{V_{15}+V_{16}}{2}$	1	0	0	0	1	0	ON	↓										
$\frac{V_{15}+3V_{16}}{4}$	1	0	0	0	1	1	↓	OFF	↓	↓	↓	↓	↓	↓	↓	↓		



European Patent
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EUROPEAN SEARCH REPORT

Application Number
EP 93 11 9471

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
X	EP-A-0 478 386 (SHARP) * abstract; claims 1,4; figures 1,2,4-7 * * page 4, line 13 - line 51 * * page 6, line 36 - line 47 * ---	1-4	G09G3/36
Y	EP-A-0 488 516 (IBM) * the whole document * ---	1-4	
Y	EP-A-0 458 169 (TOSHIBA) * abstract; claim 1; figures 4-6 * * column 3, line 17 - column 4, line 19 * * column 6, line 18 - column 7, line 41 * ---	1-4	
A	IBM TECHNICAL DISCLOSURE BULLETIN., vol.33, no.6B, November 1990, NEW YORK US pages 384 - 385 'Driving method for TFT/LCD grayscale' * the whole document * -----	1-4	
			TECHNICAL FIELDS SEARCHED (Int.Cl.5)
			G09G H04N
The present search report has been drawn up for all claims			
Place of search BERLIN		Date of completion of the search 22 February 1994	Examiner Saam, C
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document	