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The diagram shows a four-terminal network. The input terminals are labeled 1 and 2, and the output terminals are labeled 3 and 4. The circuit includes five transistors: T1, T2, T3, T4, and T5 (labeled C5). There are also four capacitors: C1, C2, C3, and C4. The circuit is configured as follows:

- Terminal 1 is connected to the base of T1 and the collector of T5.
- Terminal 2 is connected to the emitter of T1, the emitter of T2, and the emitter of T4.
- The collector of T1 is connected to the base of T2 and the collector of T3.
- The collector of T2 is connected to the base of T4 and the collector of T5.
- The collector of T3 is connected to terminal 3.
- The collector of T4 is connected to terminal 4.
- Capacitor C1 is connected between the collector of T1 and the emitter of T2.
- Capacitor C2 is connected between the collector of T2 and the emitter of T2.
- Capacitor C3 is connected between the collector of T3 and the emitter of T3.
- Capacitor C4 is connected between the collector of T4 and the emitter of T4.
- Capacitor C5 (labeled T5) is connected between the collector of T5 and the emitter of T5, which is also connected to terminal 2.

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The invention relates to electrical circuit arrangements. The invention is particularly applicable to electrical circuit arrangements having an input branch for receiving an input current and an output branch for producing an output current related to the input current. Examples of such circuit arrangements are current mirror circuits and in particular current mirror circuits employing MOS transistors.

MOS current mirror circuits add harmonic distortion components to signals passing through them which increases as the signal frequency and signal amplitude increase. This distortion in MOS current mirror circuits is due to the charging and discharging of various capacitances present at the nodes of the circuit.

It is an object of the invention to enable the reduction of harmonic distortion in circuits where capacitances associated with non linear devices cause the generation of harmonic distortion.

The invention provides an electrical circuit arrangement including a plurality of circuit nodes and a plurality of circuit devices having a non-linear voltage/current characteristic together with an associated capacitance; wherein a further capacitance is connected to a selected node, said further capacitance being arranged and having a value so as to compensate currents drawn by said associated capacitances.

The circuit arrangement may have an input branch for receiving an input current, the input branch comprising a first device having a non-linear voltage/current characteristic and having an associated capacitance; and an output branch for producing an output current related to the input current, the output branch comprising a second device having the same non-linear voltage/current characteristic as the first device and having an associated capacitance: wherein a further capacitance is connected at a selected node to compensate currents drawn by said associated capacitances.

In a MOS current mirror having an input branch comprising a diode connected MOS transistor and an output branch comprising an MOS transistor having its gate electrode connected to the gate electrode of the diode connected transistor an input current must flow into the capacitances associated with the transistors, normally parasitic device capacitances, which current subtracts from the drain current of the input transistor. Thus the drain current of the output transistor which is a replica of the drain current of the input transistor is not equal to the input current. Since the gate voltage of the input transistor would vary in a non-linear fashion (approximately a square law relationship for an MOS transistor) in the absence of any associated capacitance, the current which flows into the capacitance at this node is similarly non-linear. As a result harmonic distortion components are added to the output current. While this effect will also occur in bipolar circuitry the result is less serious be-

cause of the high device transconductance for a given parasitic capacitance. Thus the invention is particularly useful when applied to circuit arrangements including MOS transistors but may be used with any other active devices with varying degrees of usefulness.

Thus in an electrical circuit arrangement according to the invention said input branch may comprise first and second MOS transistors having their source-drain paths arranged in series and wherein the drain electrode of the first transistor is connected to the gate electrode of the second transistor and to the input of the circuit arrangement; said output branch may comprise third and fourth transistors having their source-drain paths arranged in series, the drain electrode of the third transistor being connected to the output of the circuit arrangement; the gate electrode of the second transistor may be connected to the gate electrode of the fourth transistor; the gate electrodes of the first and third transistors may be connected to a source of bias potential; and a compensation capacitor may be formed between the gate and source electrodes of the first transistor, the compensation capacitor having such a value as to cause substantial compensation of currents drawn by the parasitic capacitances associated with the transistors.

The compensation capacitor may comprise a fifth MOS transistor having its drain and source electrodes connected together. By forming the compensation capacitor within an MOS transistor it will have the same characteristics as the parasitic capacitances of the other four transistors and thus will maintain a fixed relationship with them. In addition when fabricated as part of an integrated circuit it can be formed in the same processing steps as the other transistors and no special steps are needed to form the compensation capacitance.

The above and other features and advantages of the invention will become apparent from the following description, by way of example, of an embodiment of the invention with reference to the accompanying drawings, in which:-

Figure 1 is a circuit diagram of a known MOS current mirror circuit showing the parasitic capacitances associated with the transistors, and

Figure 2 is a circuit diagram of an MOS current mirror circuit incorporating the invention.

As shown in Figure 1, the current mirror circuit comprises an input branch comprising first and second MOS transistors T1 and T2 connected in series between an input 1 and a common line 2. The drain electrode of transistor T1 is connected to the input 1 and to the gate electrode of transistor T2. The current mirror circuit further comprises an output branch comprising third and fourth MOS transistors T3 and T4 connected in series between an output 3 and the common line 2, the drain electrode of transistor T3

being connected to the output 3. The gate electrode of transistor T2 is connected to the gate electrode of transistor T4 while the gate electrodes of transistors T1 and T3 are connected to a point 4 to which, in operation, a bias voltage is applied. Capacitors C1 to C4 are shown connected between the gate and source electrodes of transistors T1 to T4 respectively. These capacitors are representative of the parasitic capacitances associated with each of the transistors.

In terms of signal currents if an input current I_{in} is applied to input 1 then a current $I_{C2}+I_{C4}$ is present in the common gate connection of transistors T2 and T4 while a current of $I_{in}-I_{C2}-I_{C4}+I_{C1}$ is present at the drain of transistor T2. This current is mirrored to the drain of transistor T4 but at the output 2 the current I_{out} becomes

$$I_{in} - I_{C2} - I_{C4} + I_{C1} - I_{C3}.$$

Thus the current mirror circuit shown in Figure 1 produces an error current dependent upon the parasitic capacitances of the transistors.

The current mirror circuit shown in Figure 2 is modified from that shown in Figure 1 by the provision of a further MOS transistor T5 which has its gate electrode connected to the gate electrodes of transistors T1 and T3 and its drain and source electrodes connected together and to the drain electrode of transistor T2.

The effect of transistor T5 is to add a capacitance C5 which will cause a further current to be produced which, if the value of the capacitance C5 is appropriately chosen, will substantially cancel the error current caused by capacitances C4 and C2. If it is assumed that transistors T1 to T4 all have the same dimensions then the output current $I_{out} = I_{in} - I_{C2} - I_{C4}$ since the contributions due to C1 and C3 cancel out. Thus by adding a capacitance equal to $C2 + C4$ at the drain electrode of transistor T2 a further current of $I_{C2} + I_{C4}$ will be added to the current at the drain electrode of transistor T2 thus cancelling the error current due to capacitances C2 and C4 associated with transistors T2 and T4.

By making the capacitance C5 equal to $C2 + C4$ the error currents are cancelled, at least as regards first order effects. In order to cause the additional fabricated capacitance C5 to maintain a fixed relationship with C2 and C4 it is made as an MOS transistor using the same processes as are used to produce transistors T1 to T4. Current mirrors of this type are of course commonly fabricated as part of an integrated circuit.

Satisfactory dimensions for transistor T5 can be derived from first order theory. It is assumed that transistors T1 to T4 are operated in their saturated region whereas T5 will be in the triode region. Thus the gate-source capacitances of transistor T2 and T4 will be $2WLCox/3$. Hence by making W.L of T5 equal to $4/3 (W.L)T2$ the capacitance C5 will cause the error currents caused by capacitances C2 and C4 to be

substantially cancelled. This is normally achieved using equal values of L for all the transistors to maintain best matching, in which case $W(T5)$ is made equal to $4W/3 (T2)$.

The above analysis assumes identical devices for transistors T1 to T4 but it can be shown that if the ratio W/L of transistor T4 is n times that of transistor T2, i.e. to provide an output current n times the input current, then the dimensions of transistor T5 should be $\frac{2}{3} (1+n) W.L$.

While the invention has been described with reference to a "high-compliance" or cascode connected current mirror circuit using MOS transistors it is not restricted to such an application. The invention may be applied to other circuits where a linear component shares a current with a non-linear one and where an output current is dependent on a voltage generated across the non-linear component due to a current applied thereto. Other non-linear devices could be used, for example bi-polar transistors, although the utility of the invention will depend on the particular non-linear characteristic of the devices employed and the value of the associated capacitances.

Claims

1. An electrical circuit arrangement including a plurality of circuit nodes and a plurality of circuit devices having a non-linear voltage/current characteristic together with an associated capacitance; wherein a further capacitance is connected to a selected node, said further capacitance being arranged and having a value so as to compensate currents drawn by said associated capacitances.
2. An electrical circuit arrangement as claimed in Claim 1, having an input branch for receiving an input current, the input branch comprising a first device having a non-linear voltage/current characteristic and having an associated capacitance; and an output branch for producing an output current related to the input current, the output branch comprising a second device having the same non-linear voltage/current characteristic as the first device and having an associated capacitance; wherein a further capacitance is connected at a selected node to compensate currents drawn by said associated capacitances.
3. An electrical circuit arrangement as claimed in Claim 1 or Claim 2 in which said non-linear devices are MOS transistors.
4. An electrical circuit arrangement as claimed in Claim 3 in which said input branch comprises first and second MOS transistors having their source-

drain paths arranged in series and wherein the drain electrode of the first transistor is connected to the gate electrode of the second transistor and to the input of the circuit arrangement; said output branch comprises third and fourth MOS transistors having their source-drain paths arranged in series, the drain electrode of the third transistor being connected to the output of the circuit arrangement; the gate electrode of the second transistor is connected to the gate electrode of the fourth transistor; the gate electrodes of the first and third transistors are connected to a source of bias potential; and a compensation capacitor is formed between the gate and source electrodes of the first transistor, the compensation capacitor having such a value as to cause substantial compensation of currents drawn by the parasitic capacitances associated with the transistors.

5. An electrical circuit arrangement as claimed in Claim 4 in which said compensation capacitor comprise a fifth MOS transistor having its drain and source electrodes connected together.
6. A electrical circuit arrangement as claimed in Claim 4 in which the first to fourth transistors are identical and have a channel width to length ratio of W/L and the fifth transistor has a width to length ratio of $4W/3L$.
7. An electrical circuit arrangement as claimed in Claim 5 in which the first and second transistors have a width to length ratio of W/L , the third and fourth transistors have a width to length ratio of nW/L , and the fifth transistor has a width to length ratio of $2(1+n)W/3L$.
8. An electrical circuit arrangement as claimed in any preceding claim fabricated as part of an integrated circuit wherein the associated capacitances are the parasitic capacitances of the non-linear devices.

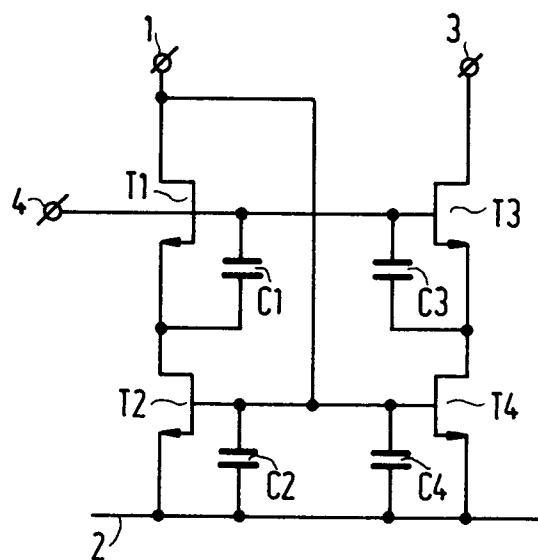


FIG. 1

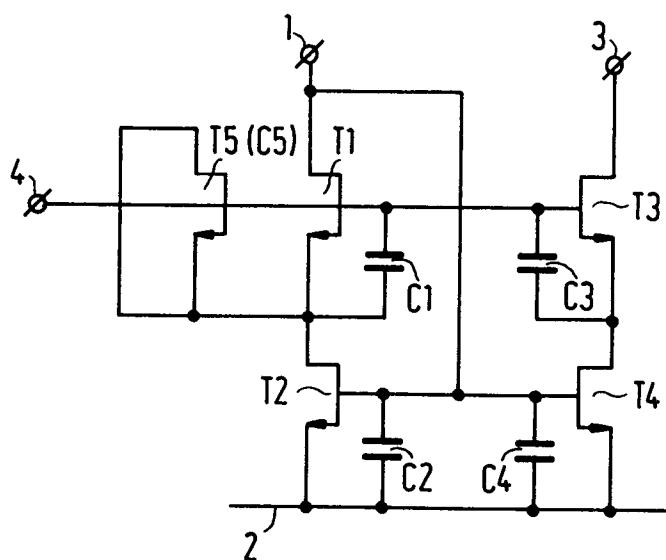


FIG. 2



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EUROPEAN SEARCH REPORT

Application Number
EP 94 20 0014

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
P,X	DE-A-42 01 155 (TEXAS INSTRUMENTS DEUTSCHLAND GMBH) * column 3, line 29 - column 4, line 32; figures 3-5 *	1-4,8	G05F3/26
X	EP-A-0 488 315 (BROOKTREE CORPORATION) * column 3, line 37 - column 5, line 37; figures 2,3 *	1-5,8	
A	EP-A-0 496 424 (NEC CORPORATION) * column 3, line 28 - line 49 * * column 5, line 22 - line 50; figures 1,4 *	1,3,5,8	
			TECHNICAL FIELDS SEARCHED (Int.Cl.5)
			G05F
The present search report has been drawn up for all claims			
Place of search		Date of completion of the search	Examiner
THE HAGUE		18 March 1994	Cleary, F
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document			