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(54) System for prevention of erroneous detection of synchronization in a data transmission system with forward error correction.

(57) The present invention provides, in a system in which synchronization of an interleaver circuit and a deinterleaver circuit, to be inserted between a convolutional encoder and a Viterbi decoder, is obtained from a synchronization detecting circuit of the Viterbi decoder, forward error correcting transmitter and receiver permitting prevention of erroneous detection of synchronization. For this, an LFSR is used as a row-direction address counter in writing and an up/down counter is used as a column-direction address counter in reading, in the interleaver circuit. In the deinterleaver circuit, an up/down counter is used as the column-direction address counter in writing, and an LFSR is used as the row-direction address counter in reading.

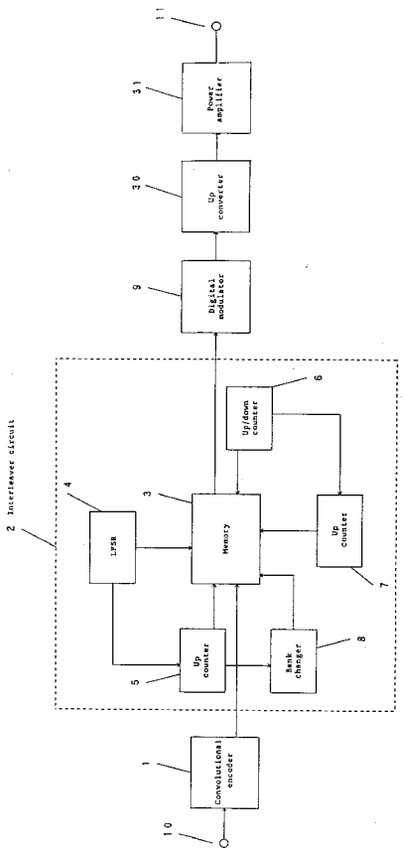

Fig. 1

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BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION

The present invention relates to forward error correcting transmitter and receiver used for digital transmission such as multiphase PSK (Phase Shift Keying) and multi-value QAM (Quadrature Amplitude Modulation).

2. DESCRIPTION OF PRIOR ART

Along with the recent progress of band compression technology of image signals through digital signal processing, transmission of digital data has now potentiality of being diffused not only in the communications area but also widely in the broadcasting area, and a forward error correcting apparatus for digital transmission such as QPSK (Quadrature Phase Shift Keying) and 16QAM has become essential technology.

The conventional forward error corrector is composed of a transmitter for transmitting digital signals and a receiver receiving thus transmitted digital signals.

The transmitter comprises a convolution encoder which converts an input digital signal to be transmitted into a forward error corrected code, an interleaver circuit which changes a sequence of output data within each of predetermined block lengths, and a digital modulator which modulates an output of the interleaver circuit.

The receiver comprises a digital demodulator which demodulates an entered digital wave, a block phase control circuit which controls a block partition of demodulated digital signal, a deinterleaver circuit which releases interleaving made on a transmitting side, and a Viterbi decoder which conducts forward error correcting decoding. A synchronization detecting circuit which detects synchronization of codes is connected to the Viterbi decoder; the block phase control circuit is controlled on the basis of results of detection thereof.

In the transmitter, the interleaver circuit sequentially writes digital signals converted into forward error correction codes by the convolution encoder in the row direction into memories arranged, for example seven in the row direction and four in the column direction, and then,sequentially reads out data written into the memories in the column direction (see Fig. 8). The read-out data are modulated by the digital modulator, and transmitted to the transmission line.

Then, in the receiver, the transmitted digital modulated wave is demodulated by the digital demodulator and enter the block phase control circuit. When a code is determined not to be in synchronization with a certain integral period in the synchronization detecting circuit, the block phase control circuit causes a shift for one symbol of the partition of deinterleaved block. This shift is continued until code synchronization is confirmed, and upon determination of synchronization, then block partition is kept. This utilizes the fact that disagreement between the block partition interleaved on the transmission side and the block partition to be deinterleaved on the receiving side makes it impossible to achieve synchronization of the Viterbi decoder.

Thus, an interleaved block partition is found on the receiving side with the use of the synchronization detecting circuit of code, to cause deinterleaving for each block partition, and forward error correcting decoding is accomplished by the Veterbi decoder (for example, see Japanese Laid-Open Patent Publication No. 3-32, 131; for code synchronization, see, for example: Yasuda et al. "Code Synchronizing Method in Viterbi Decoding," The Transaction of the Institute of the Electronics Information and Communication Engineers, (B), vol. J66-B, No. 5, pp. 623-630 (May 1983)).

In the configuration as described above, however, data columns before interleaving remain at many points even when interleaving has been accomplished at a wrong block partition as shown in Fig. 8, and another problem is possibility of erroneous synchronization detection in the synchronization detecting circuit.

SUMMARY OF THE INVENTION

An object of the present invention is therefore to provide forward error correcting transmitter and receiver which take account of the above-mentioned problems in the conventional forward error corrector and permit prevention of erroneous detection of synchronization.

To achieve the object, the forward error correcting transmitter of the present invention comprises: an error correcting encoding means which error-correcting-encodes a digital signal to obtain an error-correcting-encoded signal; an interleaving means comprising a memory being composed of rows and columns and permitting read and write of said error-correcting-encoded signal, and a memory control means which controls said memory, when writing in said memory, so as to write said error-correcting-encoded signal row by row in a prescribed fixed sequence in each row, and controls said memory, when reading out from said memory, so as to read out said error-correcting-encoded signal written in said memory sequentially in one direction in each column alternately reversing the direction column by column; a modulating means which modulates said error-correcting-encoded signal read out from said memory to obtain a modulated signal; and a transmitting means providing a transmitting signal from said modulated signal.

The forward error correcting receiver of the present invention comprises: a receiving means which receives a transmitting signal; a demodulating means which demodulates said transmitting signal to obtain an input signal; an deinterleaving means comprising a memory being composed of rows and columns and permitting read and write of said input signal, and a memory control means which controls said memory, when writing in said memory, so as to write said input signal sequentially in one direction in each column alternately reversing the direction column by column, and controls said memory, when reading out from said memory, so as to read out said input signal row by row in a prescribed fixed sequence in each row; an error correcting decoding means which error-correcting-decodes said input signal read out from said memory; and a synchronization detecting means which detects synchronization of said input signal to be error-correcting-decoded.

In the forward error correcting transmitter of the present invention, by the configuration as described above, the error correcting encoding means converts a digital signal into an error-correcting-encoded signal, the interleaving means writes in, when writing in the memory, the error-correcting-encoded signal into the memory in accordance with a row-direction address based on a previously determined random number, reads out, when reading out from the memory, the error-correcting-encoded signal written in the memory in the column direction, and reads out, when switching over to the next column, in the reverse direction, and the modulating means provides a signal read out from the memory as an output.

In the forward error correcting receiver of the present invention, the demodulating means demodulates the transmitted signal, the deinterleaving mean writes in, when writing in the memory, the input signal in the column direction, write in, when switching over to the next column, the input signal in the reverse direction, and reads out, when reading out from the memory, the input signal written in the memory in accordance with a row-direction address based on the predetermined random numbers; the error correcting decoding means error-correcting-decodes the input signal read out from the memory; and the synchronization detecting means detects synchronization of the input signal to be error-correcting-decoded.

According to the present invention, deinterleaving at a wrong block partition causes breakage and diffusion of the original data array, thus permitting prevention of erroneous detection of synchronization upon decoding the error-correcting-encoded signal.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram of a forward error correcting transmitter of an embodiment of the present invention;

Fig. 2 is a block diagram of a forward error correcting receiver of the embodiment of the present invention;

Fig. 3 is a block diagram of the forward error correcting transmitter of another embodiment of the present invention;

Fig. 4 is a block diagram of the forward error correcting receiver of the another embodiment of the present invention;

Fig. 5 is a descriptive view of functions of a interleaver circuit and a deinterleaver circuit of the embodiment;

Fig. 6 is a descriptive view of functions of the interleaver circuit and the deinterleaver circuit of the another embodiment;

Fig. 7 is a descriptive view of functions of the interleaver circuit and the deinterleaver circuit of a further another embodiment; and

Fig. 8 is a descriptive view of functions of the interleaver circuit and the deinterleaver circuit of the conventional apparatus.

DESCRIPTION OF PREFERRED EMBODIMENTS

Now, the present invention will be described with reference to drawings showing embodiments thereof.

Fig. 1 is a block diagram of a forward error correcting transmitter of an embodiment of the present invention, and Fig. 2 is a block diagram of a forward error correcting receiver of an embodiment of the present invention. A forward error corrector is composed of the forward error correcting transmitter and the forward error correcting receiver.

The forward error correcting transmitter shown in Fig. 1 is provided with an input terminal 10 for entering a digital signal to be transmitted, and a convolutional encoder 1 for converting the digital signal into an error-correcting-encoded signal is connected to the input terminal 10. An interleaver circuit 2 which changes a sequence of data within a block for each of predetermined block lengths is connected to this convolutional encoder 1. A digital modulator 9 for modulating a digital signal as an output means is connected to the interleaver circuit 2. An output of the digital modulator 9 is connected to an output terminal 11.

The interleaver circuit 2 is provided with a 2-port type memory 3, permitting simultaneous read and write, composed of rows and columns. The memory 3 is composed of two banks of two-dimensional memories expressed by m x n, having in general a size of (m x n) x2. In other words, during writing in one bank, data of the immediately preceding block already written in are read out from the other bank, and at the point when processing has reached the full memory size, write and read are conducted in succession by switching over the bank. An LFSR (Linear Feedback Shift Register) 4 for providing a row-direction address when writing data from the convolutional encoder 1,

an up counter 5 for providing a column-direction address, and a bank changer 8 are connected to the memory 3. In addition, an up/down counter 6 for providing a row- direction address when reading out and an up counter 7 for providing row-direction address are connected to the memory 3.

The forward error correcting receiver shown in Fig. 2 is, on the other hand, provided with an input terminal 17 for entering a digital modulated wave, to which a digital demodulator 12 for demodulating the digital modulated wave is connected. A block phase control circuit 13 for changing the block partition of an input signal is connected to this digital demodulator 12. A deinterleaver circuit 14 for releasing interleaving of data is connected to this block phase control circuit 13, and a Viterbi decoder 15 for decoding the error-correcting-encoded signal is connected to this deinterleaver circuit 14. An output terminal 18 for providing a decoded signal as an output and a synchronization detecting circuit 16 for detecting code synchronization are connected to the Viterbi decoder 15, and this synchronization detecting circuit 16 is connected to the block phase control circuit 13.

A 2-port type memory 21 permitting simultaneous read and write composed of rows and columns is provided in the deinterleaver circuit 14, as in the interleaver circuit 2. The memory 21 has in general a size (m x n) x 2 and is composed of two banks of two-dimensional memory expressed by m x n. An up-/down counter 24 for providing column-direction address when writing in data from the block phase control circuit 13, and an up counter 25 for providing a row-direction address are connected to the memory 21. In addition, an LFSR 22 for providing a row-direction address when reading out data, an up counter 23 for providing a column-direction address, and a bank changer 26 are connected to the memory 21. For the LFSRs 4 and 22 used for the interleaver circuit 2 and the de-interleaver circuit 14, the same generator polynominal must be employed. Because the LFSR can give a native initial value by means of a reset signal, it is possible to perform the same operations on the interleaving and deinterleaving sides.

At this point, the convolutional encoder 1 conducts error correcting encoding, and the Viterbi decoder 15 conducts error correcting decoding.

Now, the operations of the forward error corrector configured as described above will be described. First, in the forward error correcting transmitter, the digital signal is encoded into an error-corrected code, and this signal is interleaved by the interleaver circuit 2. This interleaving writes data in the row direction through a first port set on the write port into the memory 3 composed of seven row-direction memories and four column-direction ones, as shown in Fig. 5, for example. This row-direction address during writing is provided by random numbers generated by the LFSR 4, and when a row is filled fully with data, the up counter 5 increases the column-direction addresses by one, which is given as the column-direction address.

Furthermore, the bank changer 8 detects completion of write into the m x n memory areas under the effect of a carry signal of the up counter 5, and performs bank switchover by reversing the MSB (Most Significant Bit) of the addresses in the memory 3.

Then, the thus written data are read out through a second port set on the read-out port of the memory 3. The column-direction address during this reading out operation is given by the up/down counter 6, and the row-direction address is provided by the up counter 7. The data are read out sequentially in the column-direction, and when switching over to the next column, in the reverse direction. The data outputted from the interleaver circuit 2 are digital-modulated (such as PSK, QAM, etc.) in a predetermined intermediate frequency band by the digital modulator 9. After the data outputted from the digital modulator 9 are up converted by an up converter 30, the data are amplified to a predetermined transmitting power by a power amplifier 31, and transmitted as transmitting signals to a transmission line from an output terminal 11.

In the forward error correcting receiver, the transmitting signals entered from an input terminal 17 are chosen in channel and down converted to the predetermined intermediate frequency band in a tuner 32. Signals outputted from the tuner are demodulated in the digital demodulator 12 and restored as digital data by being identified at a threshold level. The digital data is sent to the block phase control circuit 13. The synchronization detecting circuit 16 determines, for each block partition of the deinterleaver circuit 14, whether detection of synchronization at the Viterbi decoder 15 is successful or not, and in the case of an unsuccessful detection, the block partition of the block phase control circuit 13 is changed by one symbol (corresponding to one clock) to another direction. The block phase control circuit 13 can be achieved by using it continuously in circulation with the use of a memory capable of reading and writing. More specifically, write and read are performed in succession, and the block partition is shifted by changing the amount of delay by sequentially changing the difference between the write address and the read address.

Then, the output from the block phase control circuit 13 is entered into the deinterleaver circuit 14. The processing in the deinterleaver circuit 14 forms a pair with that in the interleaver circuit 2. The signal entered into the deinterleaver circuit 14 is written in through the first port of the memory 21 set on the write port. A column-direction address for this writing is given by the up/down counter 24, and a row-direction address, by the up counter 25. Signals are sequentially written in the column direction, and when switching over to the next column, are written in the reverse direction.

Then, data are read out in the row direction through the second port set on the readout port of the memory 21. The row- direction address in this reading is given by random numbers generated by the LFSR 22, and when an entire row is fully filled with data, the up counter 23 increases the column-direction address by one, and this one is provided as the column-direction address.

Furthermore, completion of readout of the m x n memory areas is detected by means of a carry signal of the up counter 23, and the bank changer 26 performs bank switchover by reversing MSB of the address of the memory 21.

Data of which the sequence has been altered by interleaving on the transmitting side, when being deinterleaved at a proper data partition by the deinterleaver circuit 14, return to the original data column before interleaving and enter the Viterbi decoder 15. The Viterbi decoder 15 conducts Viterbi decoding of an entered data column and sends the result as an output to the output terminal 18. To ensure detection and maintenance of synchronization even through a robust transmission line, the synchronization detecting circuit 16 determines whether detection of synchronization is successful or not by monitoring the data for a certain period of time, i.e., monitoring a certain number of the data. If the memory area is assumed to have a block size of m x n, it is necessary, in order for the synchronization detecting circuit 16 to make such a determination within a block, that a monitoring time of the Viterbi decoder 15 should be set so as to be smaller than m x n.

Now, the following paragraphs explain that, in the deinterleaver circuit 14 of the above-mentioned embodiment, deinterleaving at a position other than the proper data partition causes breakage and diffusion of the original data column, thus making detection of synchronization unsuccessful in the synchronization detecting circuit 16.

Figs. 5 and 8 illustrate the data column sequentially before interleaving, in the interleaver circuit, in the transmission line, in the deinterleaver circuit, and then after deinterleaving. For simplicity, the two-dimensional memories used in the interleaver circuit 2 and the deinterleaver circuit 14 comprise 7 x 4 memory spaces arranged seven in the row direction and four in the column direction. The addresses begin with 0 for both rows and columns, and the origin of address is located upper left of a memory space.

Fig. 8 illustrates a conventional case using ordinary up counters for both the row direction and the column direction, in which deinterleaving is conducted at a position off the proper data partition by one symbol. As it is clear from the result after deinterleaving, the data column before interleaving is maintained to some extent, so that erroneous detection of synchronization is highly probable in the synchronization detecting circuit 16.

Fig. 5 illustrates a case where an up/down counter 24 is used as the column-direction counter upon writing of the deinterleaver circuit 14, and an LFSR 22 is used as the row-direction counter upon reading. In this case, a generator polynominal $X^3 + X^2 + 1$ is assumed for the LFSR. The count value varies in period of seven from 0 to 4, 6, 3, 5, 2, 1, and then 0. In general, an LFSR 22 composed of a generator polynominal having a degree of n has a period of $2^n - 1$. Fig. 5 covers the case of deinterleaving at a position off the proper data partition by one column: since the original data column is broken and diffused as a result of deinterleaving, there is no possibility that erroneous detection of synchronization should be successful in the synchronization detecting circuit 16.

According to this embodiment, as described above, the original data column is not broken but returns to the original state only when conducting deinterleaving at the proper data partition, by using a configuration in which the up/down counter 24 is used as the column-direction address counter when writing in the memory for the deinterleaver circuit, and using the LFSR as the row-direction address counter when reading out, thus permitting avoidance of generation of erroneous detection of synchronization in the synchronization detecting circuit 16.

Then, in the forward error correcting transmitter of an another embodiment, the row-direction address in writing into the memory 3 of the interleaver circuit 2 is given in succession in a single direction, and the column-direction address in reading is given by the up/down counter as in the above-mentioned embodiment (see Fig. 3). In the forward error correcting receiver, so as to correspond to the above, the column-direction address when writing in the memory 21 of the deinterleaver circuit 14 is given, as in the above-mentioned embodiment, by the use of the up/down counter, and the row-direction address is given in succession in a single direction (see Fig. 4). According to the configuration as described above, as shown in Fig. 6, when using the up/down counter as the column-direction counter in writing of the deinterleaver circuit 14, and an ordinary up counter as the row-direction counter in reading out (the case of deinterleaving at a position off the proper data partition by one symbol, shown in Fig. 6 as in Fig. 8), the original data column is broken and diffused as a result of deinterleaving, thus eliminating the possibility of erroneous detection of synchronization in the synchronization detecting circuit 16.

When deinterleaving is conducted at a position off the proper data partition by one column as in Fig. 5, use of the up/down counter as the column-direction counter in writing exerts no effect, and the original data column before interleaving is maintained to some extent, thus resulting in a higher possibility of erroneous detection of synchronization in the synchronization detecting circuit.

Although the LFSR has been used for generating random numbers in the above-mentioned embodiments, this is not limitative, but any other random number generator may be employed with the condition that the sequence of addresses corresponds between the interleaving side and the deinterleaving side.

While the above embodiment has had a configuration using the up counters 5 and 7 and the up counters 23 and 25, a configuration using down counters may be used. The bank changer in the above-mentioned embodiments has used a configuration in which the carry signal of the up counter 5 or 23 is entered, whereas it is also possible to adopt a configuration in which the carry signal of the up counter 7 or 25 is entered.

While the 2-port memory permitting simultaneous read and write has been used in the above embodiments, read and write may be conducted by time-sharing processing with the use of a 1-port memory.

Although the two-dimensional memories have ad 7 x 4 memory spaces in the above-mentioned embodiments, the memory size is not limited to this.

The interleaver circuit 2 and the deinterleaver 14 have been configured with special hardware in the above embodiments. It is needless to mention, however, that the configuration is not limited to this, so the same function may be achieved in a form of computer software.

Claims

1. A forward error correcting transmitter which comprises:

   an error correcting encoding means which error-correcting-encodes a digital signal to obtain an error-correcting-encoded signal;

   an interleaving means comprising

   a memory being composed of rows and columns and permitting read and write of said error-correcting-encoded signal, and

   a memory control means which controls said memory,

   when writing in said memory, so as to write said error-correcting-encoded signal row by row in a prescribed fixed sequence in each row, and controls said memory, when reading out from said memory, so as to read out said error-correcting-encoded signal written in said memory sequentially in one direction in each column alternately reversing the direction column by column;

   a modulating means which modulates said error-correcting-encoded signal read out from said memory to obtain a modulated signal; and

   a transmitting means providing a transmitting signal from said modulated signal.

2. A forward error correcting transmitter as claimed in Claim 1, wherein said prescribed fixed sequence is a predetermined random sequence.

3. A forward error correcting transmitter as claimed in Claim 2, wherein said predetermined random sequence is an M-series sequence.

4. A forward error correcting transmitter as claimed in Claim 1, wherein said prescribed fixed sequence is continuous in one direction.

5. A forward error correcting receiver which comprises:

   a receiving means which receives a transmitting signal;

   a demodulating means which demodulates said transmitting signal to obtain an input signal;

   an deinterleaving means comprising:

   a memory being composed of rows and columns and permitting read and write of said input signal, and

   a memory control means which controls said memory, when writing in said memory, so as to write said input signal sequentially in one direction in each column alternately reversing the direction column by column, and controls said memory, when reading out from said memory, so as to read out said input signal row by row in a prescribed fixed sequence in each row;

   an error correcting decoding means which error-correcting-decodes said input signal read out from said memory; and

   a synchronization detecting means which detects synchronization of said input signal to be error-correcting-decoded.

6. A forward error correcting receiver as claimed in Claim 5, wherein said prescribed fixed sequence is a predetermined random sequence.

7. A forward error correcting receiver as claimed in Claim 6, wherein said predetermined random numbers represent a maximum length shift register sequence.

8. A forward error correcting receiver as claimed in Claim 5, wherein said prescribed fixed sequence is continuous in a single direction.

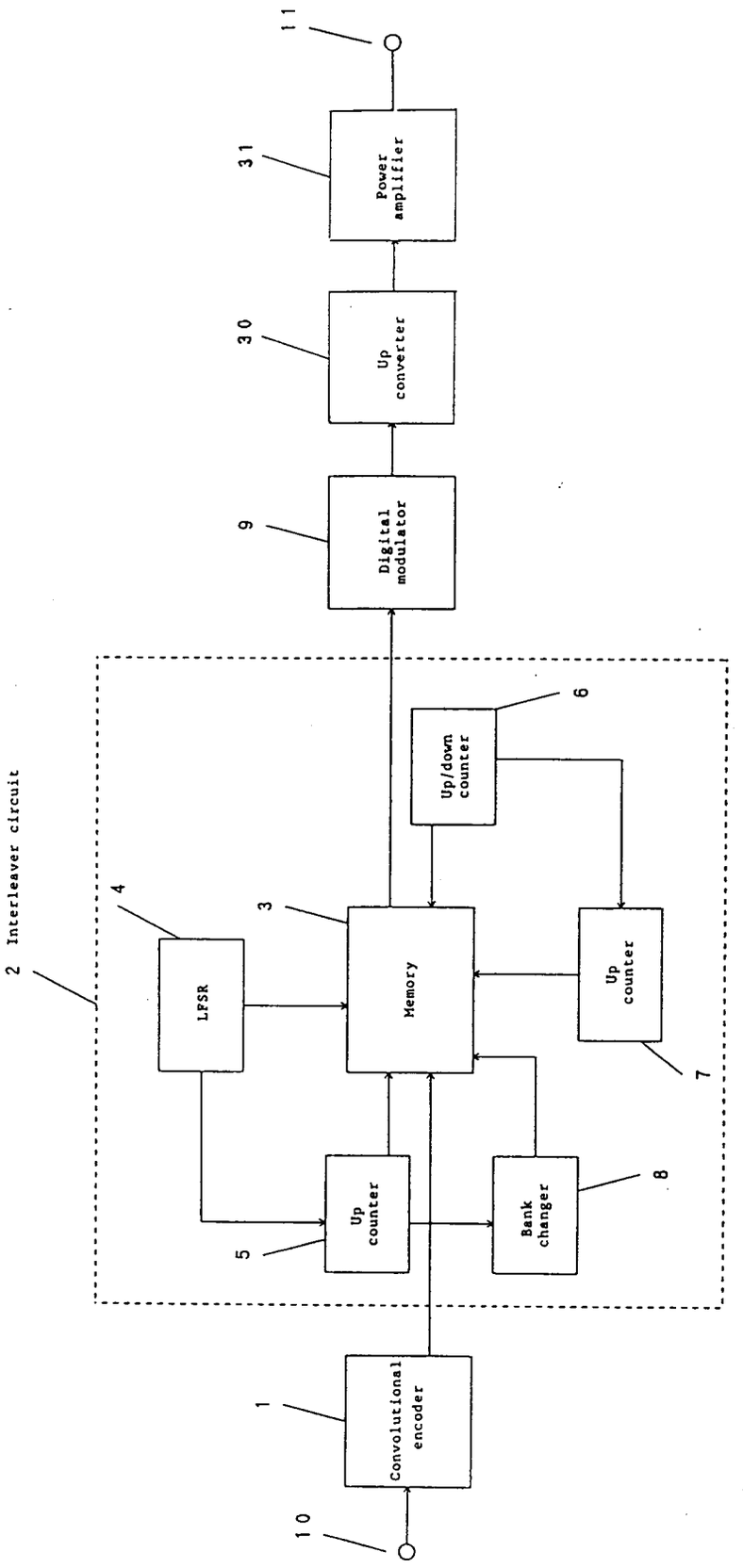

11
Power amplifier
31
Up converter
30
Digital modulator
9
2 Interleaver circuit
Up/down counter
6
4
3
LFSR
Memory
Up counter
7
5
Up counter
Bank changer
8
1
Convolutional encoder
10

Fig. 1

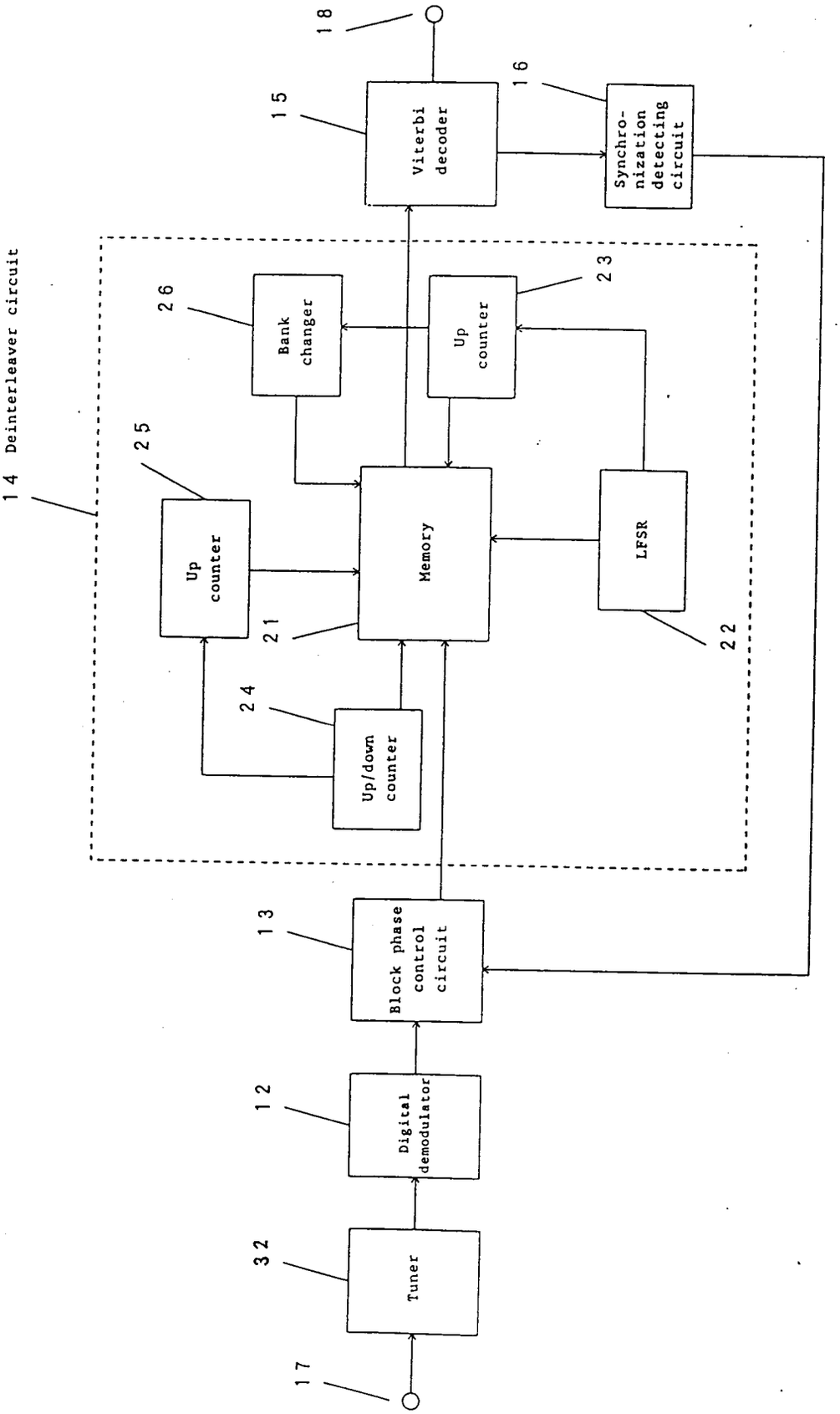
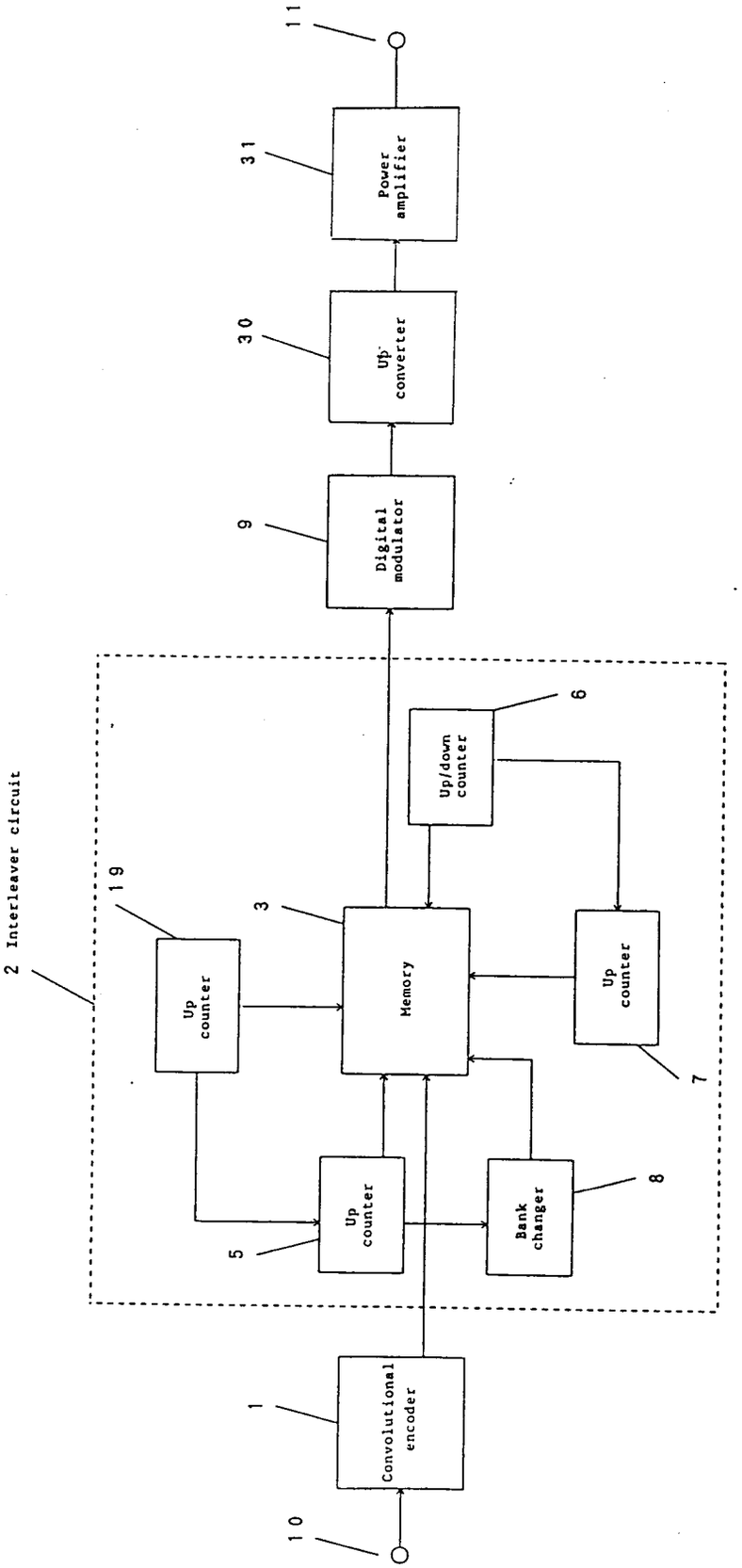

17
32
Tuner
12
Digital demodulator
13
Block phase control circuit
14 Deinterleaver circuit
15
Viterbi decoder
16
Synchro-nization detecting circuit
18
21
Memory
22
LFSR
23
Up counter
24
Up/down counter
25
Up counter
26
Bank changer

Fig. 2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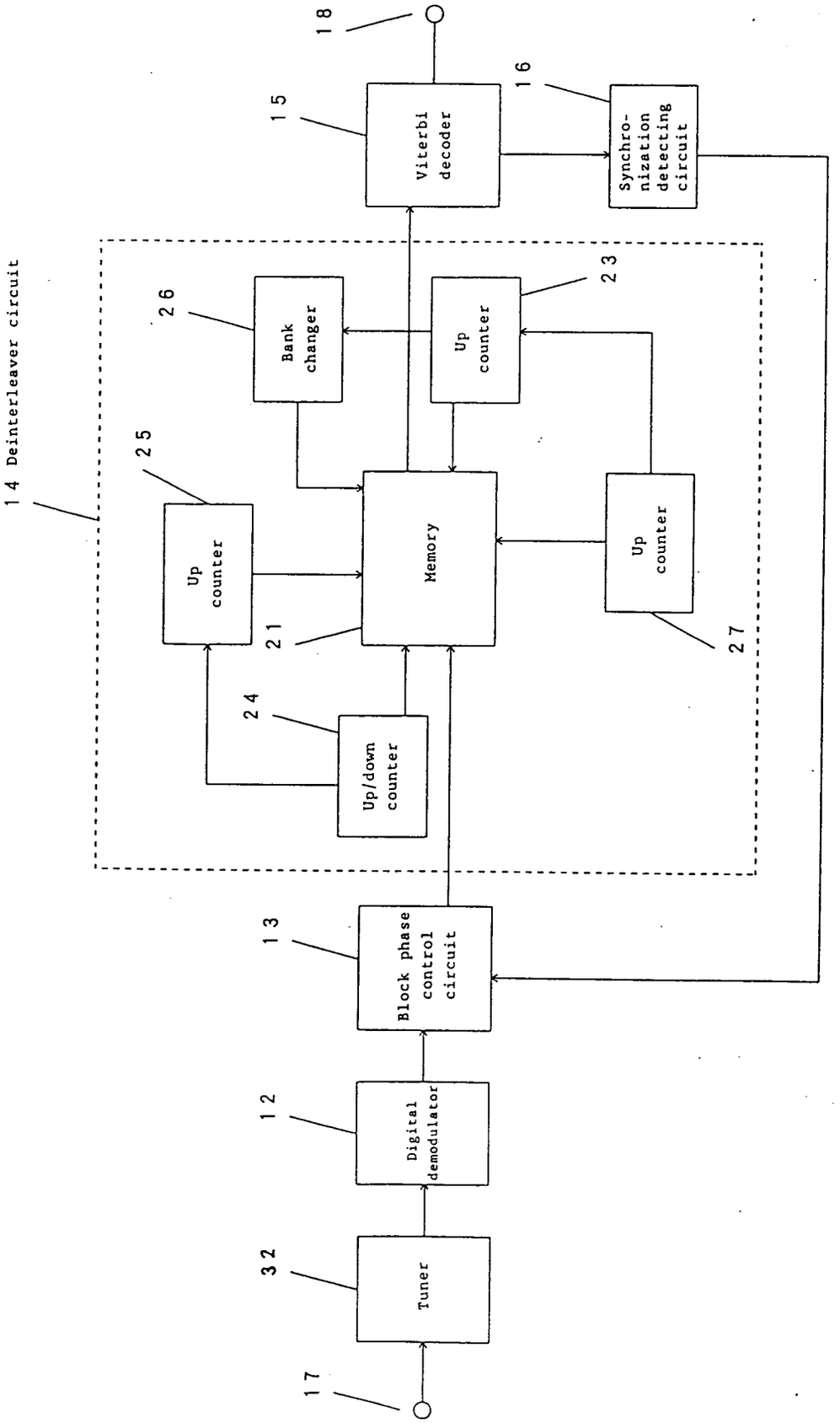
1
2 Interleaver circuit
19
Up counter
3
Memory
Up counter
7
Up counter
5
Bank changer
8
Up/down counter
6
Digital modulator
9
Up converter
30
Power amplifier
31
11

Fig. 3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32
Tuner
12
Digital demodulator
13
Block phase control circuit
14 Deinterleaver circuit
15
Viterbi decoder
16
Synchro-nization detecting circuit
18
21
Memory
23
Up counter
24
Up/down counter
25
Up counter
26
Bank changer
27
Up counter

Fig. 4

Fig. 5

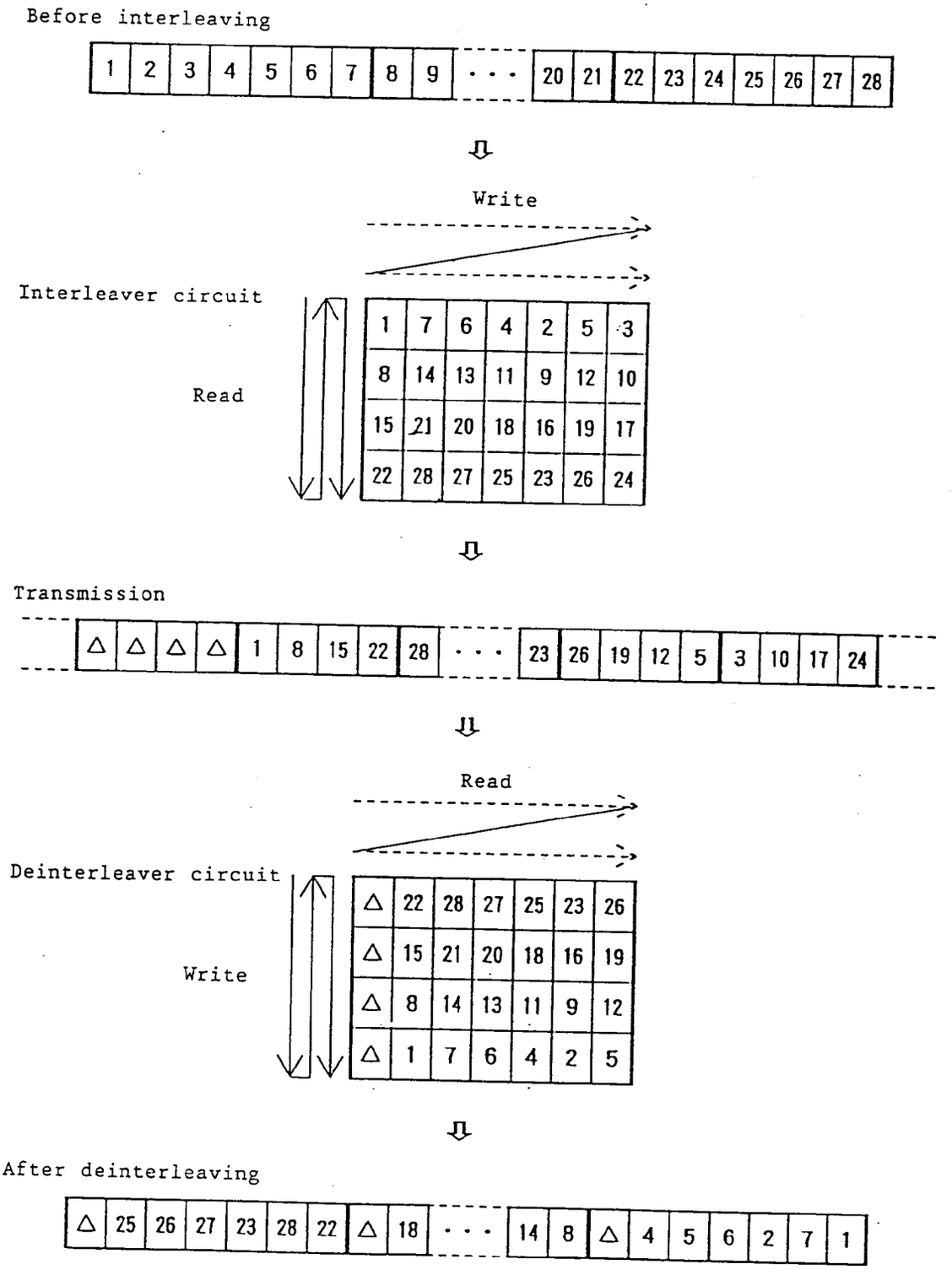
Before interleaving
1 2 3 4 5 6 7 8 9 · · · 20 21 22 23 24 25 26 27 28
Write
Interleaver circuit
Read
1 7 6 4 2 5 3
8 14 13 11 9 12 10
15 21 20 18 16 19 17
22 28 27 25 23 26 24
Transmission
Δ Δ Δ Δ 1 8 15 22 28 · · · 23 26 19 12 5 3 10 17 24
Read
Deinterleaver circuit
Write
Δ 22 28 27 25 23 26
Δ 15 21 20 18 16 19
Δ 8 14 13 11 9 12
Δ 1 7 6 4 2 5
After deinterleaving
Δ 25 26 27 23 28 22 Δ 18 · · · 14 8 Δ 4 5 6 2 7 1

Fig. 6

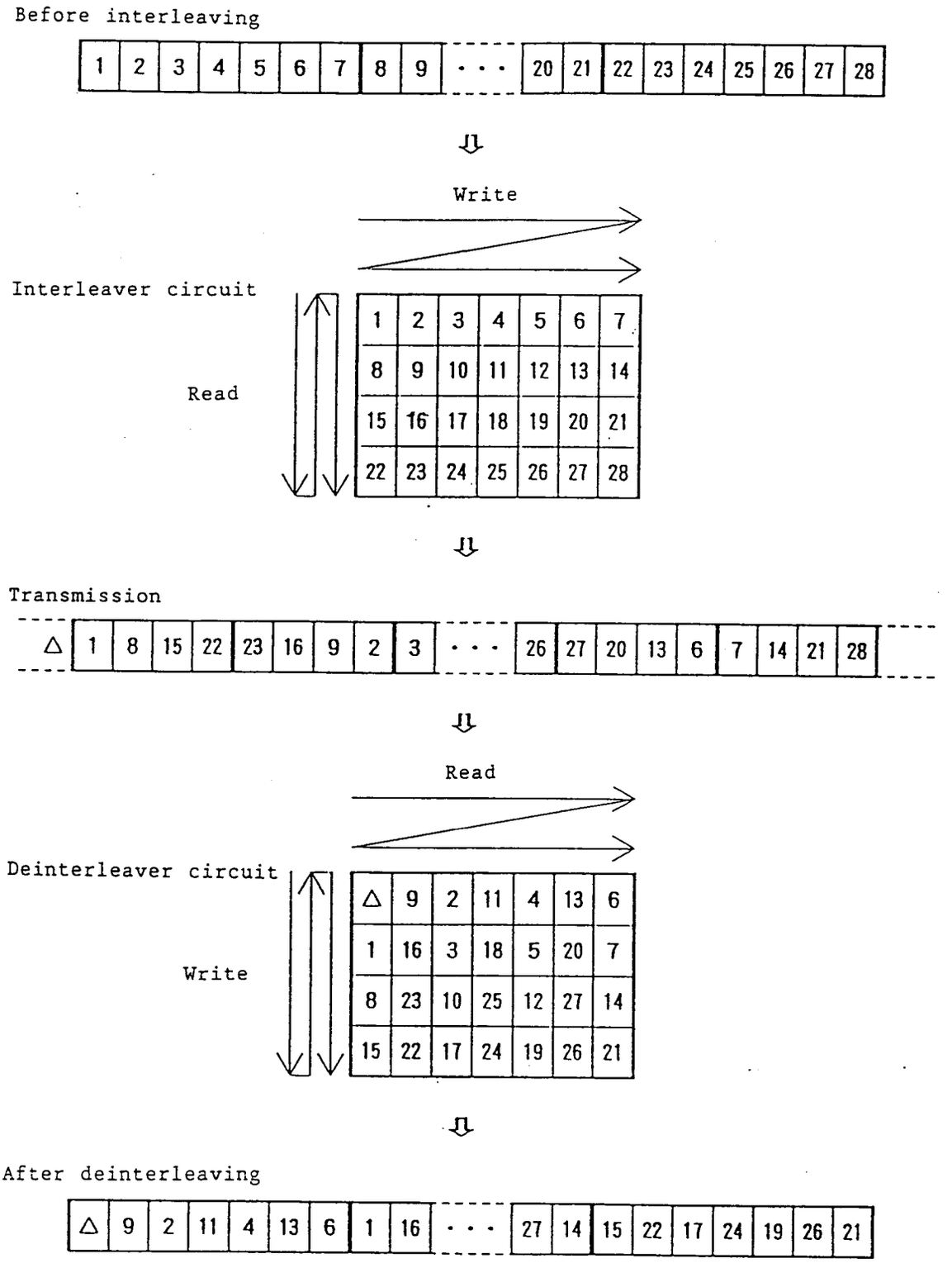
Before interleaving
1 2 3 4 5 6 7 8 9 · · · 20 21 22 23 24 25 26 27 28
Write
Interleaver circuit
Read
1 2 3 4 5 6 7
8 9 10 11 12 13 14
15 16 17 18 19 20 21
22 23 24 25 26 27 28
Transmission
Δ 1 8 15 22 23 16 9 2 3 · · · 26 27 20 13 6 7 14 21 28
Read
Deinterleaver circuit
Write
Δ 9 2 11 4 13 6
1 16 3 18 5 20 7
8 23 10 25 12 27 14
15 22 17 24 19 26 21
After deinterleaving
Δ 9 2 11 4 13 6 1 16 · · · 27 14 15 22 17 24 19 26 21

Fig. 7

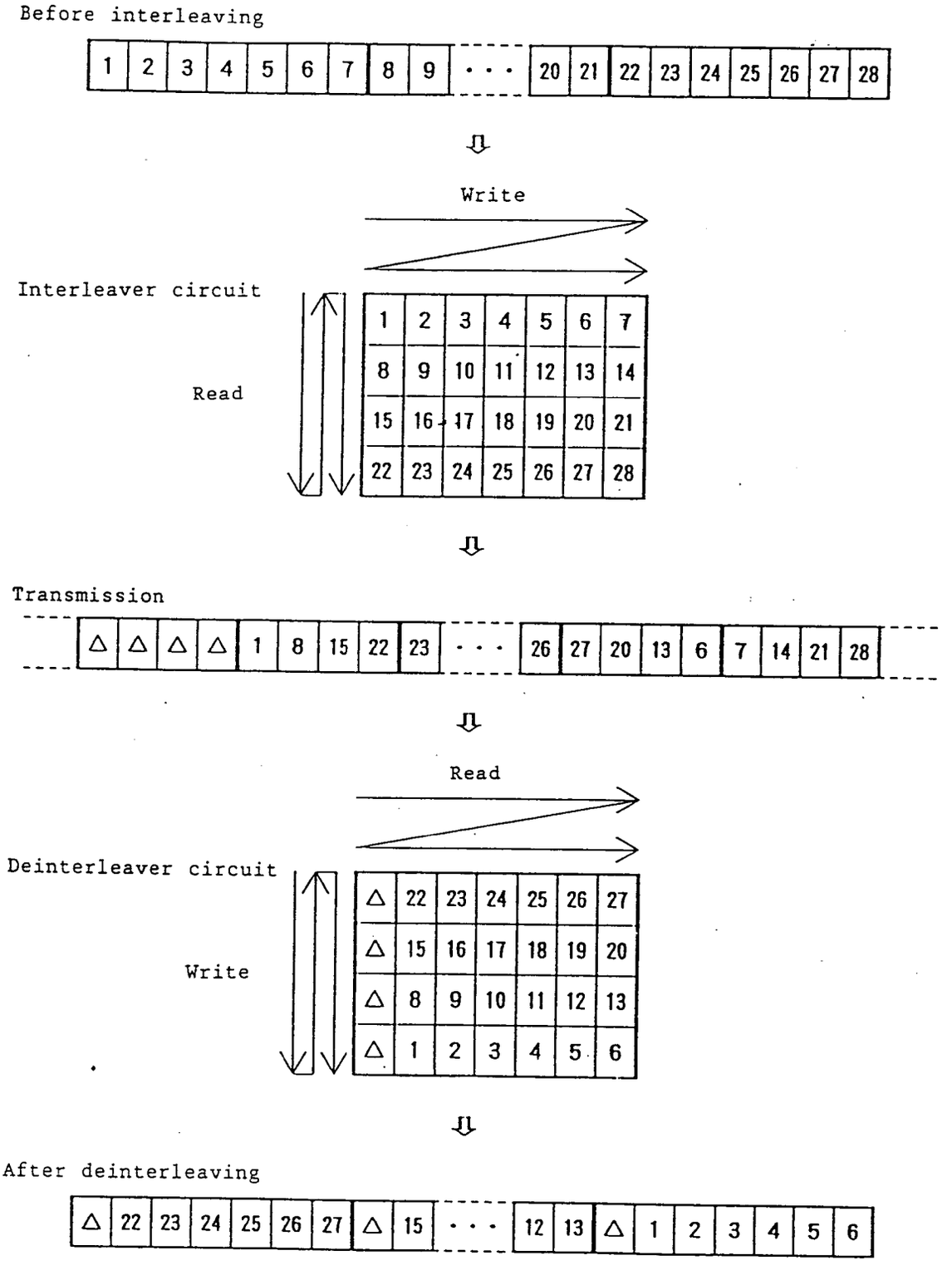
Before interleaving
1 2 3 4 5 6 7 8 9 · · · 20 21 22 23 24 25 26 27 28
Write
Interleaver circuit
Read
1 2 3 4 5 6 7
8 9 10 11 12 13 14
15 16 17 18 19 20 21
22 23 24 25 26 27 28
Transmission
△ △ △ △ 1 8 15 22 23 · · · 26 27 20 13 6 7 14 21 28
Read
Deinterleaver circuit
Write
△ 22 23 24 25 26 27
△ 15 16 17 18 19 20
△ 8 9 10 11 12 13
△ 1 2 3 4 5 6
After deinterleaving
△ 22 23 24 25 26 27 △ 15 · · · 12 13 △ 1 2 3 4 5 6

Fig. 8

Prior Art