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(71) Applicant: **NEC CORPORATION**
7-1, Shiba 5-chome
Minato-ku
Tokyo (JP)

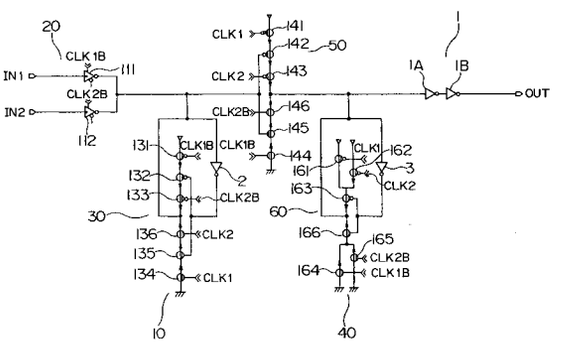
(72) Inventor: **Nishizawa, Takahiko, c/o NEC Corporation**
7-1, Shiba 5-chome
Minato-ku,
Tokyo (JP)

(74) Representative: **Glawe, Delfs, Moll & Partner**
Patentanwälte
Postfach 26 01 62
D-80058 München (DE)

(54) Memory circuit having a plurality of input signals.

(57) Disclosed is a multi-input memory circuit comprising a first input gate (20) for selecting one of a plurality of data signals, a first inverting gate (2) for receiving the output of the first input gate as an input, a first feedback gate (30), which has a structure of a vertical lamination inverter, receives a plurality of clock signals (CLK1,CLK2), inverted signals (CLK1B,CLK2B) of those clock signals and the output of the first inverting gate (2), and has its output terminal connected to the output terminal of the first input gate (20), and a second input gate (50), which has a vertical lamination inverter structure, and receives a plurality of clock signals, inverted signals of those clock signals and the output of the first input gate (20), and a second feedback gate (60), which has a horizontal lamination inverter structure, receives a plurality of clock signals, inverted signals of those clock signals and the output of the second inverting gate (3), and has its output terminal connected to the output terminal of the second input gate (50). With this structure, a system of matching the phases of control signals for the individual gates with one another is latently incorporated in the multi-input edge-trigger type memory circuit, thereby preventing data dropout.

FIG. 2



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EUROPEAN SEARCH REPORT

Application Number
EP 94 10 1614

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
A	ELECTRONICS LETTERS, vol.23, no.23, November 1987, ENAGE GB pages 1221 - 1222 ORTON 'NOVEL CMOS LATCH WITH CLOCK HYSTERESIS' * the whole document * ---	1,5,7	G11C7/00
A	EP-A-0 115 834 (TOSHIBA) * abstract * * page 3, line 25 - page 4, line 30; figures 1,2 * ---	1,5,7	
A	EP-A-0 416 576 (TOSHIBA MICRO ELECTRONICS CORP.) * column 1, line 5 - column 1, line 30; figures 1,2 * -----	1,5,7	
			TECHNICAL FIELDS SEARCHED (Int.Cl.5)
			G11C H03K

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	29 March 1995	Stecchina, A

CATEGORY OF CITED DOCUMENTS

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