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(54) Liquid crystal display apparatus.

(57) A liquid crystal display apparatus comprises a liquid crystal element adapted to be driven by a plurality of row electrodes and column electrodes in which a plurality of row electrodes are simultaneously selected, a column voltage generating circuit to apply to each of the column electrodes voltages based on orthogonal conversion signals which are obtained by converting, with use of an orthogonal function, picture signals corresponding to the positions of the simultaneously selected row electrodes of the display element, and a row voltage generating circuit to apply voltages based on row electrode selection pattern signals formed with an orthogonal function to the simultaneously selected row electrodes, wherein the row voltage generating circuit comprises a row electrode selection means to address sequentially the each simultaneously selected row electrodes, and a row voltage generating means to apply voltages in response to the corresponding data in the row electrode selection pattern signals to the each row electrodes selected by the row electrode selection means.

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FIGURE 1

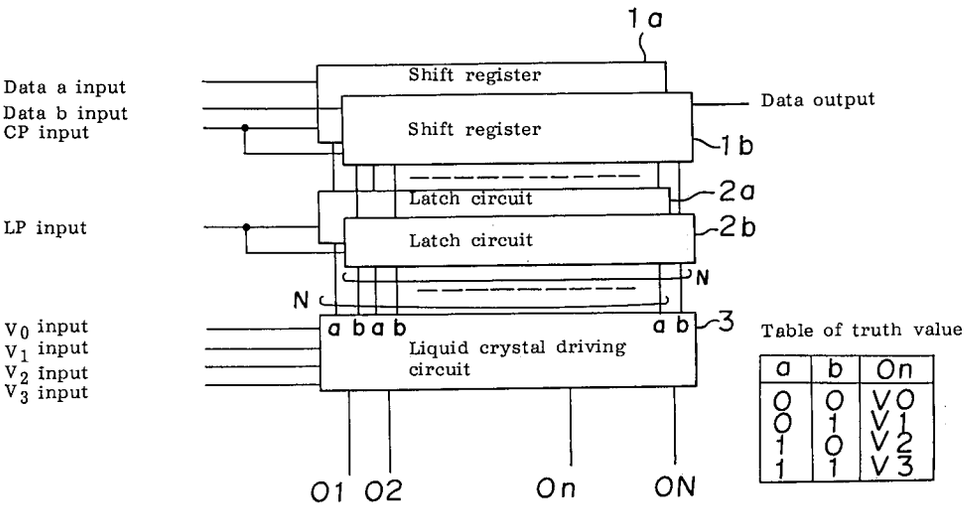


Table of truth value

a	b	On
0	0	V0
0	1	V1
1	0	V2
1	1	V3

The present invention relates to a liquid crystal display apparatus in which a liquid crystal display element having a fast responding characteristic is used. In particular, the present invention relates to a passive matrix type liquid crystal display apparatus wherein row selection voltages are generated by a multiple line selection method.

Heretofore, a liquid crystal display element responding to the effective value of a voltage applied, such as a supertwisted nematic (STN) liquid crystal element has been practically used. In order to improve the switching speed for a display, a liquid crystal element having a fast responding characteristic has been desired. However, the liquid crystal element having a fast responding characteristic had a problem that an optical difference was small between an ON state and an OFF state whereby contrast was poor.

As a generally used liquid crystal driving method, there is a successive line addressing method which selects and drives for each scanning line, each element of a liquid crystal element in which the elements are arranged in a matrix form. When the successive line addressing method is used for a liquid crystal element having a response time of about 200 msec which is not so high, the response time is relatively long in comparison with the period of the waveform of a voltage for the successive line addressing method. However, when the response time is short as about 20-100 msec, the response time becomes close to the period of the waveform of the voltage for the successive line addressing method. As a result, it happens that a pixel which is in an ON state in a selection period in the successive line addressing returns to be in an OFF state during a non-selection period. Namely, the difference of brightness between the ON state and the OFF state is small. Such phenomenon is called a frame response.

In order to eliminate the frame response, it is considered to increase the frequency of the voltage for the successive line addressing in response to an increased response speed of the liquid crystal element. However, a high frequency causes uniformity in a display because the frequency spectrum of a voltage waveform applied to the element becomes high.

As a driving method to eliminate the above-mentioned problem, a multiple line selection method (MLS method) for selecting a plurality of scanning lines as a batch is proposed. When a plurality of scanning lines are simultaneously selected for driving, a period of selection signals applied to a single row electrode can be shortened without changing the pulse width of the selection signals. As the multiple line selection method, there are a method of simultaneously selecting all scanning lines as described in SID '92 DIGEST (1992) P. 228 and a method of simultaneously selecting a plurality of scanning lines which are less than all scanning lines described in SID '92 DIGEST (1992) P. 238.

In either method, when the two levels of the selection signals are expressed as +1 and -1, the time sequence of each of the selection signals given to the scanning lines simultaneously selected is an orthogonal function formed by +1 and -1. When data corresponding to ON and OFF of a display are expressed by +1 and -1, the signal lines for providing display data are supplied with voltages based on a result of comparison of the orthogonal function with each of the data.

In a successive line addressing method using 1/N duty driving and an alternating voltage in two frames, the first through the N th row electrodes which correspond to the scanning lines are scanned by positive selection outputs, and then, the first through the N th row electrodes are scanned by negative selection outputs whereby an alternating waveform is performed. Thus, a display sequence is finished. Namely, each of the row electrodes is scanned twice in a display sequence constituted by two frames. In this case, a single row electrode is selected at once, and accordingly, it is enough to use a single row electrode driver for controlling the polarity of voltage applied.

On the other hand, when the MLS method is used wherein the selection period and the frame period are the same as those in the successive line driving method, each of the scanning lines can be scanned 2L times in a single display sequence wherein L is the number of scanning lines simultaneously selected. In this case, if selection signals for the scanning lines are distributed in the single display sequence, the period of the selection signals applied to the row electrode can be short. Namely, the reduction of the optical difference (between an ON state and an OFF state) of the liquid crystal element can be suppressed in comparison with a case of the successive line driving method. Accordingly, a driving method applicable to a fast responding element can be realized. In this case, however, it is necessary to control independently the polarity of the row electrodes corresponding to a plurality of selected scanning lines. Figure 11 shows an example of the waveform of row electrodes when L = 3. In Figure 11, R1-R9 respectively show row electrodes.

If conventional row electrode drivers are used to control independently the polarity of voltages applied to an L number of row electrodes simultaneously selected, an L number of drivers are needed. When the value L is taken large, the scale of the circuit becomes large to thereby make the liquid crystal display apparatus expensive. In other words, the value of L has to be an appropriate

value while the frame response be minimized.

The inventors of this application proposed a driving method of liquid crystal wherein an L number of scanning lines are simultaneously selected and the polarity of the row electrodes is effectively controlled, in Japanese Unexamined Patent Publication Nos. 27904/1994, 27907/1994 and USP 5,262,881. The proposed methods will be described in brief.

Supposing that voltages applied to each of the row electrodes are either $+V_r$ or $-V_r$ ($V_r>0$) when selection signals are active, and are 0 in a non-selection time. An N number of row electrodes are divided into an L number of groups, and an L number of row electrodes in a group are simultaneously selected. For simplification, assuming that N is an integer multiplied by L, and $N = M \times L$. Namely, the number of groups is M. Further, groups consisting of simultaneously selected row electrodes are referred to as row electrode subgroups. Row electrodes forming a single row electrode subgroup are not always necessary that they are continuously arranged. A row electrode subgroup may be formed by gathering row electrodes positioned separately.

Selection voltages applied to the row electrodes forming the m th (m is any one of 1-M) row electrode subgroup selected, can be expressed by the arrangement of the L order of vectors in time sequence, the vectors being based on voltages applied to the row electrodes. The arrangement of the vectors in time sequence is referred to as a selection voltage matrix. Further, column vectors which form a selection voltage matrix are referred to as selection voltage vectors. After the determination of the selection voltage matrix, each element of the selection voltage vectors which form a selection voltage matrix is applied as voltages to the corresponding row electrodes. The voltage is applied successively to each of the row electrode with respect to the all selection voltage vectors, whereby the selection of a single row electrode subgroup is completed.

In the following, explanation is made as to a method of forming the selection voltage matrix. First, a matrix (orthogonal matrix) $A = [\alpha 1, \alpha 2, ..., \alpha k]$ comprising L rows and K columns, which has an element of $+V_r$ or $-V_r$ and in which the product of a matrix and a transposed matrix of the same assumes a scalar multiple of a unit matrix, is selected, where αq ($q = 1$-K) are appropriate column vectors having an L number of elements, and K is an integer of $K \geq L$ (q is a natural number). When K is determined to be excessively large, the number of selection pulses necessary to select the row electrodes is large. Accordingly, it is preferable that K may be the smallest value as possible.

Figure 12 shows a concrete example of a matrix A wherein L = 4, 8 and K = 4, 8. As a result of driving a liquid crystal element with use of several kinds of matrices, it was confirmed that use of the Hadamard's matrices shown in Figures 12(a) and (c) could control ununiformity of display. In a case of $L \neq 2^p$, the L-row-K-column matrix A can be formed by removing an optional (K-L) rows from a K order matrix wherein the product of a matrix and a transposed matrix of the same forms a scalar multiple of the unit matrix.

In the above-mentioned Japanese Unexamined Patent Publication No. 27904/1994 and 27907/1994, there is statement that as the selection voltage matrix a matrix of vectors wherein the selection voltage vectors composed of at least $\alpha 1, \alpha 2, ..., \alpha k, -\alpha 1, -\alpha 2, ..., -\alpha k$ are arranged, is selected. Namely, the selection voltage matrix composed of the 2K number of vectors wherein each of the vectors appears once in the selection voltage matrix can be selected. By using such method of selection, the driving of the liquid crystal element in an alternating form is generally obtainable.

The number of the column vectors forming the selection voltage matrix may be increased. For instance, when L=2, all possible conditions of electric potential in the row electrode subgroups is $2^4 = 16$. Accordingly, selection voltage matrices including 16 kinds of selection voltage vectors can be formed. Further, the order of the arrangement in time sequence of the selection voltage is optional. The order may be substituted or shifted each time when the selection of a row electrode subgroup is finished, or it may be substituted each time when a display sequence is finished. It is preferable to carry out the substitution to control ununiformity of display.

Description will be made as to timing to apply the selection voltages expressed by the selection voltage vectors to each of the row electrodes. In order to suppress the frame response of the fast responding liquid crystal element, it is desirable that the selection signals are dispersed in a display sequence to reduce the length of a non-selection period with respect to each of the row electrodes. In other words, the selection signals (voltages) should not be continuously applied to a row electrode subgroup in accordance with each pattern which is shown by selection voltage vectors, but the voltages composed of a single or some selection voltage vectors should be applied to a row electrode subgroup, and the same voltages be used for controlling another row electrode subgroup. Generally, an increased number of the division of the selection voltage vectors is effective to suppress the frame response since the non-selection period can be reduced. Further, it is preferable to uniformly disperse the selection signals. Thus,

after the voltages composed of one or some selection voltage vectors have been applied to a row electrode subgroup, the voltages are applied to another row electrode subgroup.

Signals applied to column electrodes to which display signals are provided are determined as follows. Supposing that a series of data β are composed of selected voltage vectors wherein an element of $+V_r$ is 1 and an element of $-V_r$ is 0, and a series of data γ correspond to each of selected row electrodes, among data to be applied to row electrodes. Exclusive OR is applied to elements between the series of β and the series of γ. And then, an arithmetical sum is obtainable from a result of the application of the operations. Accordingly, when there are an i number of elements which have different values, the arithmetical sum is i. Then, voltage to be applied to the row electrode is Vi.

In this case, Vi is selected from an (L+1) number of voltage levels where $V_O < V1 < ... < V_L$. The absolute value of the voltage levels is determined by a threshold voltage and so on of the liquid crystal element. It is desirable that the values are selected so that the column voltages form an alternating form. When $V_i = ((2i-L)/L)V_c$, and $V_r = -(N^{1/2}/L)V_c$, the ratio V_{ON}/V_{OFF} of the voltage effective value can be the maximum where V_c is the maximum value in voltages applied to the column electrodes. Conditions other than the above-mentioned conditions may be employed. Namely, V_i and V_r may be adjusted so that the best contrast ratio is obtainable in the vicinity of the conditions.

When display data are not shown by two values, but has a gradation degree, the gradation degree can be obtained by a frame modulation method. Further, an amplitude modulation method as proposed in Japanese Application No. 269560/1992 may be used.

The above description concerns a case of $N = M \times L$. However, when the number of row electrodes which form each row electrode subgroups can not be made equal, it is considered to use dummy row electrodes so that the number of row electrodes forming each row electrode subgroups is equal.

It is an object of the present invention to provide a liquid crystal display apparatus having a row electrode driver (a row electrode voltage generating circuit) suitable for a driving method wherein an L number of scanning lines are simultaneously selected to effectively control the polarity of the low electrodes.

According to an aspect of the present invention, there is provided a liquid crystal display apparatus comprising:

a liquid crystal element adapted to be driven by a plurality of row electrodes and column electrodes in which a plurality of row electrodes are simultaneously selected,

a column voltage generating circuit to apply to each of the column electrodes voltages based on orthogonal conversion signals which are obtained by converting, with use of an orthogonal function, picture signals corresponding to the positions of the simultaneously selected row electrodes of the display element, and

a row voltage generating circuit to apply voltages based on row electrode selection pattern signals formed with an orthogonal function to the simultaneously selected row electrodes, characterized in that

the row voltage generating circuit comprises:

a row electrode selection means to address sequentially the each simultaneously selected row electrodes, and

a row voltage generating means to apply voltages in response to the corresponding data in the row electrode selection pattern signals to the each row electrodes selected by the row electrode selection means.

In the above-mentioned invention, the row voltage generating means simultaneously applies voltages having the polarities indicated by row electrode selection patterns to each of the row electrodes in row electrode subgroups addressed by the row electrode selection means.

As an embodiment of the liquid crystal display apparatus of the present invention, the row voltage generating means comprises a row electrode selection pattern setting means to output row electrode selection pattern signals corresponding to voltages applied to each row electrodes to be selected, and a row electrode driving means to apply voltages in response to patterns set by the row electrode selection pattern setting means to the each row electrodes addressed by the row electrode selection means.

In the above-mentioned embodiment, the row electrode selection pattern setting means supplies simultaneously to the row electrode driving means voltage patterns to be applied to each of the row electrodes in row electrode subgroups addressed by the row electrode selection means.

As an embodiment of the liquid crystal display apparatus of the present invention, the row electrode driving means includes a liquid crystal driving circuit which receives an N number (N: the total number of the row electrodes) of selection signals each corresponding to each of the row electrodes; which receives an N number of voltage setting signals each corresponding to each of the row electrodes; and which applies row voltages corresponding to the voltage setting signals to the row electrodes addressed by the selection signals; the row electrode selection means includes a selection

signals parallel output device which renders each of the selection signals corresponding to each of the selected row electrodes to be active and renders each of the selection signals corresponding to each of the non-selected row electrodes to be non-active whereby each of the selection signals is supplied to the liquid crystal driving circuit; and the row electrode selection pattern setting means includes a voltage setting signal parallel output device to supply, as voltage setting signals, the corresponding data in the row electrode selection pattern signals corresponding to the each selected row electrodes to the liquid crystal driving circuit.

In the above-mentioned embodiment, each of the parallel output devices supplies, as a batch, information indicative of row electrodes which form row electrode subgroups to be selected and information indicative of voltage patterns to be applied to the row electrodes, to the liquid crystal driving circuit. In this embodiment of the liquid crystal display apparatus of the present invention mentioned just above, the number of parallel outputs from the selection signal parallel output device is equal to the number of parallel outputs from the voltage setting signal parallel output device. In this case, each of the parallel output devices has the same number of stages so that the determination and control of the row electrode selection patterns can be further simplified.

In an embodiment of the liquid crystal display apparatus of the present invention, the number of the parallel outputs from the selection signal parallel output device and the number of the parallel outputs from the voltage setting signal parallel output device are equal to the total number N of the row electrodes. In this case, each of the parallel output devices has the same number of spaces N so that the determination and control of the shift electrodes selection patterns can be further simplified.

In an embodiment of the liquid crystal display apparatus of the present invention, the selection signal parallel output device includes a latch circuit which latches selection pattern signals based on selection signals to be supplied to the liquid crystal driving circuit, by means of latch pulses which are in synchronism with a timing for switching the selection of a group consisting of the simultaneously selected row electrodes, whereby the latched selection signal patterns are outputted to the liquid crystal driving circuit, and the voltage setting signal parallel output device includes a latch circuit which latches the row electrode selection pattern signals by means of the latch pulses to output the latched signals to the liquid crystal driving circuit.

In this embodiment, the latch circuits latch information which makes the selection of the row electrodes in the row electrode subgroups to be selected active, and latch information which makes the selection of other row electrodes non-active whereby information indicative of the selection and non-selection with respect to all row electrodes is supplied to the liquid crystal driving circuit.

In an embodiment of the liquid crystal display apparatus of the present invention, the selection signal parallel output device includes a shift register which shifts data indicative of an active period of the selection signals and which has a tap output for each stage connected to the latch circuit, and the voltage setting signal parallel output device includes a shift register which shifts a train of the row electrode selection patterns and which has a tap output for each stage connected to the latch circuit.

In this embodiment, the shift registers successively shift the selection signal patterns so that the information which makes the selection of the row electrodes in the row electrode subgroups to be selected active, is latched by the latch circuits at a latch timing.

In an embodiment of the liquid crystal display apparatus of the present invention, the frequency of a shift clock to be supplied to the shift register of the voltage setting signal parallel output device is higher than the frequency of a shift clock to be supplied to the shift register of the selection signal parallel output device.

In this embodiment, the shift register of the voltage setting signal parallel output device shifts the data at a speed higher than that of the shift register for shifting the selection signal patterns and supplies different patterns from those applied to a row electrode subgroup, to the next row electrode subgroup.

In an embodiment of the liquid crystal display apparatus of the present invention, the selection signal parallel output device has parallel outputs whose number is natural number times as M where M is the number of groups consisting of the simultaneously selected row electrodes, and the voltage setting signal parallel output device has parallel outputs whose number is natural number times as L where L is the number of row electrodes which form each groups.

In this embodiment, the voltage setting signal parallel output device has parallel outputs whose number is based on the number L of simultaneously selected row electrodes, and the selection signal parallel output devices has parallel outputs whose number is based on the number M of the row electrode subgroups. Accordingly, the size of each of the parallel output devices can be small.

In an embodiment of the liquid crystal display apparatus of the present invention, the selection signal parallel output device has an M number of parallel outputs, and the voltage setting signal par-

allel output device has an L number of parallel outputs.

In this embodiment, the voltage setting signal parallel output device has parallel outputs whose number is equal to an L number of the simultaneously selected row electrodes, and the selection signal parallel output device has parallel outputs whose number is equal to an M number of the row electrode subgroups. Accordingly, the size of each of the parallel output devices can be small.

In an embodiment of the liquid crystal display apparatus of the present invention, the voltage setting signal parallel output device includes a latch circuit which latches the row electrode selection pattern signals by means of latch pulses which are in synchronism with a timing of switching the selection of the groups consisting of the simultaneously selected row electrodes whereby the latched signals are outputted to the liquid crystal driving circuit.

In this embodiment, the latch circuit latches the row electrode selection patterns to be applied to a row electrode subgroup when the row electrode subgroup is selected, and the latched row electrode selection patterns are supplied to the liquid crystal driving circuit.

In an embodiment of the liquid crystal display apparatus of the present invention, the voltage setting signal parallel output device includes a shift register which shifts a train of the row electrode selection patterns and which has a tap output for each stage connected to the latch circuit.

In this embodiment, the shift register shifts row electrode selection patterns formed in series so that row electrode selection patterns to be applied to a row electrode subgroup are latched at a latch timing of the latch circuit.

In an embodiment of the liquid crystal display apparatus of the present invention, the selection signal parallel output device includes a shift register which shifts data indicative of an active period of the selection signals by means of latch pulses which are in synchronism with a timing of switching the selection of the groups consisting of the simultaneously selected row electrodes, and which supplies, as a selection signal for each groups, a tap output for each stage to the liquid crystal driving circuit.

In this embodiment, the selection signal parallel output device makes the output corresponding to a row electrode subgroup active so that the liquid crystal driving circuit can select row electrodes contained in a row electrode subgroup when the row electrode subgroup is selected.

In an embodiments of the liquid crystal display apparatus of the present invention, the selection signal parallel output device includes a latch circuit which latches selection signal patterns based on selection signals to be supplied to the liquid crystal driving circuit, by means of latch pulses which are in synchronism with a timing for switching the selection of groups consisting of simultaneously selected row electrodes, whereby the latched selection signal patterns are outputted to the liquid crystal driving circuit.

In this embodiment, the latch circuit latches the information which makes the selection of the row electrode subgroup active and information which makes another row electrode subgroup non-active when the row electrode subgroup is selected, whereby the latched information is supplied to the liquid crystal driving circuit.

In an embodiment of the liquid crystal display apparatus of the present invention, the selection signal parallel output device includes a shift register which shifts data indicative of an active period of the selection signals by shift pulses having a period equal to a period for selecting and switching a group consisting of simultaneously selected row electrodes, and supplies the tap output of each stage of the register to the latch circuit.

In this embodiment, the shift register successively shifts the selection signal patterns so that the information which makes the selection of row electrode subgroups to be selected active is latched by the latch circuit at a latch timing.

In drawings:

Figure 1 is a block diagram showing the construction of a row voltage generating circuit in the liquid crystal display apparatus according to a first embodiment of the present invention;

Figure 2 is a timing chart showing a signal waveform at each section in the first embodiment;

Figure 3 is a block diagram showing the construction of the row voltage generating circuit in the liquid crystal display apparatus according to a second embodiment of the present invention;

Figure 4 is a timing chart showing an example of row voltages in the second embodiment;

Figure 5 is a timing chart showing an example of a signal waveform at each section in the second embodiment;

Figure 6 is a block diagram showing the construction of the row voltage generating circuit in the liquid crystal display apparatus according to the third embodiment of the present invention;

Figure 7 is a timing chart showing an example of the row voltages in the third embodiment;

Figure 8 is a timing chart showing an example of a signal waveform at each section in the third embodiment;

Figure 9(a) is a block diagram showing the construction of the row voltage generating circuit in the liquid crystal display apparatus according to the fourth embodiment of the present invention;

Figure 9(b) is a timing chart showing an example of a signal waveform at each section in the fourth embodiment;

Figure 10(a) is a block diagram showing the construction of the row voltage generating circuit in the liquid crystal display apparatus according to the fifth embodiment of the present invention;

Figure 10(b) is a timing chart showing an example of a signal waveform at each section of the fifth embodiment;

Figure 11 is a timing chart showing an example of the row voltages in a case of L = 3; and

Figure 12(a)-(c) are diagrams showing an example of a selection voltage matrix A wherein L = 4, 8 and K = 4, 8.

Preferred embodiments of the liquid crystal display apparatus of the present invention will be described with reference to the drawings.

Figure 1 is a block diagram showing the construction of a row voltage generating circuit in the liquid crystal display apparatus according to the first embodiment of the present invention.

A shift register 1a has an N number of stages (N: the number of all row electrodes). The shift register 1a shifts data $\underline{a}$ which are formed by arranging in series each row electrode selection pattern corresponding to each selection voltage vector according to the timing of shift clock pulses (CP). An example of the row electrode selection pattern is explained with reference to Figure 12. In a matrix composed of +1 and -1 as elements, the row electrode selection pattern is such a pattern shown by each column in the matrix wherein the element of -1 is replaced by 0, for instance.

A latch circuit 2a having a bit width of N bits latches outputs generated at each stage of the shift register 1a, and supplies each of the outputs to each $\underline{a}$ input terminal of a liquid crystal driving circuit 3 having an N number of outputs.

A shift register 1b has an N number of stages (N: the number of all row electrodes). The shift register 1b shifts data $\underline{b}$ which are active in a selection period of row electrodes, according to the timing of CP.

A latch circuit 2b having a bit width of N bits latches outputs generated from each of the stages of the shift register 1b, and supplies each of the outputs to each $\underline{b}$ input terminal of the liquid crystal driving circuit 3. Namely, selection signal patterns are supplied from the latch circuit 2b to the liquid crystal driving circuit 3. The n th tap output of the latch circuits 2a, 2b corresponds to the n th row electrode. The liquid crystal driving circuit 3 is supplied with voltages of $+V_r$, 0, $-V_r$. The liquid crystal driving circuit 3 determines row voltages to be any of $+V_r$, 0, and $-V_r$ depending on a combination of input data $\underline{a}$ and $\underline{b}$.

A liquid crystal element is connected to the output side of the liquid crystal driving circuit 3 although the liquid crystal element is not shown in Figure 1. There is a case that when the number of row electrodes simultaneously selected is L, L does not correspond to a value multiplied by L. In such case, an output On (n: 1-N) from the liquid crystal driving circuit 3 contains a dummy output. A column voltage generating circuit (not shown) applies to each of the column electrodes voltages based on orthogonal conversion signals which are obtained by converting, with an orthogonal function, picture signals corresponding to the positions of simultaneously selected row electrodes on a display element. For instance, as described above, exclusive OR between the row electrode selection patterns and the picture signals for the columns corresponding to the selected row electrodes is taken, and an arithmetical sum of the exclusive OR operations is obtainable. Then, column voltages based on the arithmetical sum are applied to the column electrodes.

In the first embodiment, a row electrode selection means is constituted by the shift register 1b and the latch circuit 2b. A row voltage generating means is constituted by the shift register 1a, the latch circuit 2a and the liquid crystal driving circuit 3. The latch circuit 2b is shown as an example of a selection signal parallel output device, and the latch circuit 1a is shown as an example of a voltage setting signal parallel output device.

The operation of the liquid crystal display apparatus of the first embodiment will be described wherein L = 3.

Figure 11 shows signal waveforms of row electrodes R1-R9 among row electrodes Rn. Assuming that a group of R1-R3, a group of R4-R6 and a group R7-R9 are respectively selected simultaneously. Each row electrode subgroup includes three row electrodes. In this embodiment, when the first row electrode subgroup through the M th row electrode subgroup are scanned once (hereinbelow, referred to as one frame), the same row electrode selection pattern is set for each of the row electrode subgroups. When the scanning is conducted for the frame predetermined times, a display sequence for picture is finished.

As shown in Figure 2, the period of the latch pulses supplied to the latch circuits 2a, 2b is equal to a period of selecting each row voltage. During one period of the latch pulses, an L (3 in this embodiment) clock pulses are produced. The data $\underline{b}$ has an active section (a high level section) which corresponds to the selection time. The data $\underline{a}$ corresponding to the row electrode selection pattern has an active section which corresponds to three periods of clock pulses.

The data a are shifted in the shift register 1a by the clock pulses and the data b are shifted in the shift register 1b by the clock pulses. One latch pulse is produced each time when an L number of clock pulses are produced. The latch circuit 2a latches each data in the shift register 1a. The latch circuit 2b latches each data in the shift register 1b. An N number of outputs of the latch circuit 2a are inputted to the corresponding number of a input terminals of the liquid crystal driving circuit 3. An N number of outputs of the latch circuit 2b are inputted to the corresponding b input terminals of the liquid crystal driving circuit 3.

Four kinds of voltages V0-V3 are inputted to the liquid crystal driving circuit 3. For instance, V0 or V2 indicates 0, and V1 and V3 indicate $-V_r$ and $+V_r$ respectively. The liquid crystal driving circuit 3 is composed of a level shifter, an analogue switch and so on. The n th a input and the n th b input correspond respectively to a voltage applied to the n th row electrode. Namely, the liquid crystal driving circuit 3 makes the voltage to the n th row electrode to be a voltage corresponding to a non-selection state when the n th b input is in a low level. When the n th b input is in a high level, a voltage corresponding to the polarity of the n th a input is applied to the n th row electrode. For instance, when the a input is in a high level, a voltage $+V_r$ is applied. On the other hand, when in a low level, a voltage $-V_r$ is applied.

The above-mentioned relation can be expressed by a table of truth value. Namely, the liquid crystal driving circuit 3 selects either one among the voltages V0-V3 depending a combination of (a, b) inputs. For instance, when (a, b) = (0, 0) (0, 1), (1, 0) or (1, 1), V0, V1, V2 or V3 is selected respectively. The shift registers 1a, 1b have respectively an L number of stages, all row electrodes are selected once when the N number of clock pulses are inputted. During the selection of the row electrodes, the same row electrode selection pattern is applied to each of the row electrode subgroups. Then, the row electrode selection pattern is changed, namely, the data a are changed to execute the above-mentioned processing. The data a are formed by, for instance, a table in which plural kinds of row electrode selection patterns are set, a selection circuit to select one among the row electrode selection patterns at the time of initiating each cycle and a P-S converter to convert a selected row electrode selection pattern into serial signals.

In this embodiment, description has been made as to a case that the number of outputs of the latch circuits 2a, 2b is N. However, a value other than N may be used. For instance, in a case of N/2, a single display picture may be divided into two separate portions to be driven.

Further, description has been made as to a case that the latch circuits 2a, 2b are used as parallel output devices. However, another construction may be used. For instance, the latch circuits 2a, 2b may be omitted while the number of stages of the shift registers 1a, 1b is N × L, and the i × L th (i: 1-N) tap output is supplied to the liquid crystal driving circuit 3.

Further, the row electrode selection patterns and the selection signal patterns may be set in the latch circuits 2a, 2b without using the shift registers 1a, 1b. For instance, a selection signal pattern for making only the first row electrode subgroup active and a row electrode selection pattern corresponding to the first row electrode subgroup, a selection signal pattern for making only the second row electrode subgroup active and a row electrode selection pattern corresponding to the second row electrode subgroup, ..., a selection signal pattern for making only the M th row electrode subgroup active and a row electrode selection pattern corresponding to the M th row electrode subgroup may be stored in a ROM whereby the selection signal patterns and the row electrode selection patterns in the ROM are read by using address signals obtained by counting the clock pulses. In this case, consumption power can be reduced because the clock pulses having a high frequency are unnecessary. Further, the row electrode selection patterns to be applied to each row electrode subgroups in one frame can be optionally determined.

The second embodiment of the present invention will be described. In the first embodiment, the same row electrode selection pattern is applied to each row electrode subgroups until the scanning of one frame is finished. However, the row electrode selection pattern may be changed in one frame. Figure 3 is a block diagram showing the construction of a row voltage generating circuit according to a second embodiment of the present invention. In the second embodiment, the frequency of shift clock signals CPa supplied to the shift register 1a is higher than the frequency of shift clock signals CPb supplied to the shift register 1b. Accordingly, a row electrode selection pattern which is different from the row electrode selection pattern set when a row electrode subgroup has been selected just before the one frame can be set for a row electrode subgroup selected this time.

The operation of the second embodiment will be described wherein L = 3.

As shown in Figure 4, among row electrodes Rn, a group of R1-R3, a group of R4-R6, a group of R7-R9 and so on are those groups to be simultaneously selected. Each of the row electrode subgroups includes three row electrodes. In this embodiment, the frequency of the shift clock signals CPa is twice as high as the frequency of the shift

clock signals CPb as shown in Figure 5. Further, an L number (3 in the second embodiment) of the shift clock signals CPb are produced in one period of latch pulse signals.

The operations of the shift registers 1a, 1b, the latch circuits 2a, 2b and the liquid crystal driving circuit 3 are the same as those in the first embodiment except that a series of data are successively inputted so that a row electrode selection pattern to be applied to the m th row electrode subgroup appears at each corresponding stage of the shift register 1a when a high level is provided to each b input terminal in the liquid crystal driving circuit 3 corresponding to the m th row electrode subgroup.

By supplying the data a to satisfy the above-mentioned condition, it is possible to optionally determine the row electrode selection pattern applied to each electrode subgroups in one cycle. Such data a can be formed by, for instance, a table in which a series of data are set in parallel, a read circuit for reading the data in the table and a P-S converter.

The frequency of the clock pulse signals CPa is not limited to the frequency of two times as the clock pulse signals CPb. Namely, the relation among the frequency of the latch pulses LP, the clock pulse signals CPa, CPb in the second embodiment is generally expressed as follows:

CPa/CPb = k, CPb/LP = L (k is an integer of at least 2)

Thus, the row electrode selection patterns can be shifted each time when a row electrode subgroup is selected.

In the second embodiment, description has been made as to a case that the number of outputs of the latch circuits 2a, 2b is N. However, a value other than N may be used. For instance, in a case of N/2, a single display picture may be divided into two independent portions to be driven.

Further, description has been made as to a case that the latch circuits 2a, 2b are used as parallel output devices. However, another construction may be used. For instance, shift registers 1a, 1b having an N × L number of stages may be used while the latch circuits 2a, 2b are omitted, and the n × L th (n: 1-N) tap output is supplied to the liquid crystal driving circuit 3.

Further, the row electrode selection patterns and the selection signal patterns may be set in the latch circuits 2a, 2b while the shift registers 1a, 1b are omitted.

Figure 6 is a block diagram showing the construction of the row voltage generating circuit in the liquid crystal display apparatus according to a third embodiment of the present invention. In Figure 6, the data a are shifted by clock pulses in a shift register 11 having an L number of stages. The tap output of each of the stages of the shift register 11 is latched by latch pulses in a latch circuit 12. The data b are shifted by latch pulses in a shift register 13 having an M number of stages.

Parallel outputs from the latch circuit 12 are connected to an N number of a input terminals of the liquid crystal driving circuit 3. For instance, the i th (i: 1-L) output of the latch circuit 12 is connected to the i th, the L + i th, the 2L + i th, ..., the (M-1) L + i th a input terminals. On the other hand, m th (m: 1-M) stage output is connected to the (J-1) L th - the jL th b input terminals, i.e., is connected to an M number of input terminals where N = L × M.

In the third embodiment, a row electrode selection means is constituted by the shift register 13. A row voltage generating means is constituted by the shift register 11, the latch circuit 12 and the liquid crystal driving circuit 3. The shift register 13 is shown as an example of a selection signal parallel output device, and the latch circuit 12 is shown as an example of a voltage setting signal parallel output device.

The operation of the third embodiment will be described with reference to a timing chart in Figure 8 wherein L = 7. The data a to be inputted are such one obtained by forming a single row electrode selection pattern in series. The shift register 11 shifts the successively inputted data by clock pulses. On the other hand, data capable of selecting only an L number of row electrodes are inputted as the data b.

When a latch pulse is produced, the latch circuit 12 takes the data in the shift register 11. Since seven clock pulses are produced between the last latch pulse and the present latch pulse, a single row electrode selection pattern is set in the shift register 11. Accordingly, data obtained by forming the row electrode selection pattern in series are inputted to the first through seventh a input terminals, the eighth through the fourteenth a input terminals, ..., and the (N-6) th through the N th a input terminals in the liquid crystal driving circuit 3. On the other hand, the shift register 13 takes the data b by a latch pulse, and shifts the content by 1 bit. For instance, when a high level is set at the first stage of the shift register 13, a high level is given to the first through the seventh b input terminals in the liquid crystal driving circuit 3. Namely, an instruction is given to the liquid crystal driving circuit 3 so that the first row electrode subgroup including the first through the seventh row electrodes becomes active. The liquid crystal driving circuit 3 applies a voltage($+V_r$ or $-V_r$) based on the polarity of the data inputted to the first through the seventh a input terminals to the first through the seventh row electrodes. In the same manner as the case of the first and second embodiments, the liquid crystal driving circuit 3 conducts processing

according to the table of truth value.

During the selection time to each row electrodes, the shift register sets a row electrode selection pattern to be applied to the next row electrode subgroup. When a latch pulse is produced, the set pattern is set to the first through the seventh a input terminals, the eighth through the fourteenth a input terminals, ..., and the (N-6)th through the N th a input terminals. On the other hand, the shift register 13 shifts the content of data by a latch pulse, and accordingly, a high level is produced for a stage next to the stage in which a high level is provided at the last time.

Accordingly, the condition of the b input terminals is so determined as to select the row electrode subgroup next to the subgroup which has been selected last time. Accordingly, the liquid crystal driving circuit 3 applies a voltage ($+V_r$ or $-V_r$) based on the polarity of the data inputted to the eighth through the fourteenth a input terminals to the row electrode subgroup including the eighth through the fourteenth row electrodes, for instance.

Thus, the voltage based on the row electrode selection pattern is applied to the row electrodes which constitute each row electrode subgroups. In this case, a pattern different from the row electrode selection pattern applied to a row electrode subgroup may be set for the row electrode subgroup to be selected next. Of course, the same pattern may be used.

The data a can be formed by, for instance, a table in which row electrode selection patterns are stored, a selection circuit for selecting a pattern from the table and a P-S converter. The data can be directly set in the latch circuit 12 without P-S conversion. In this case, the shift register 11 may be omitted. Further, consumption power can be reduced because clock pulses of a high frequency are unnecessary.

In this embodiment, the selection signal parallel output device is constituted by the shift register 13. However, a latch circuit for latching the selection signal pattern by a latch pulse may be used. In this case, a shift register may be provided in the front stage in the latch circuit. The shift register performs the same function as the shift register 13 used in this embodiment. In this case, the phase of shift pulses supplied to the shift register may be shifted from the phase of the latch pulses to thereby effectively reduce noises.

Further, the row voltage generating circuit of this embodiment may be included in a LCD controller circuit provided at the front stage of a driver.

A fourth embodiment of the present invention will be described. There is a case that the number of row electrodes of a display panel formed of liquid crystal display elements is greater than N. In this case, the number of electrodes to be driven can be increased by using a plural number of row voltage generating circuits as shown in Figure 3 or Figure 6. Figure 9(a) shows an embodiment of a row voltage generating circuit in which two row voltage generating circuits shown in Figure 1, Figure 3 or Figure 6 are used. In a case of using the row voltage generating circuit shown in Figure 3, clock pulse signals CPa, CPb are inputted in placed of clock pulses CP. Figure 9(b) shows an example of output waveforms, i.e. row electrode driving waveforms wherein L = 3.

Data a, shift clock pulses (CP or CPa, CPb) and latch pulses LP are commonly inputted to two row voltage generating circuits 5a, 5b. A selection signal pattern is inputted as data b, to the shift register 1b or 13 (reference to Figure 1, Figure 3 or Figure 6) of the row voltage generating circuit 5a. The output of the data b of the shift register is supplied to the input of the data b of the row voltage generating circuit 5b.

With such arrangement of connection, the row voltage generating circuit of this embodiment operates in the same manner as in the embodiments described above, and a display panel having row electrodes whose number is larger than N but smaller than 2N can be driven. In the same idea, when three or more row voltage generating circuits are serially connected, the number of row electrodes to be driven can be further increased. In this case, the number of row electrodes to be simultaneously selected is L.

A fifth embodiment of the present invention will be described. The number of row electrodes to be simultaneously selected can be increased by using a plural number of row voltage generating circuits as shown in Figure 1, Figure 3 or Figure 6. Figure 10(a) shows an example of construction wherein the number of row electrodes to be simultaneously selected is increased to 2L by using two row voltage generating circuits shown in Figure 1, Figure 3 or Figure 6. When the row voltage generating circuit shown in Figure 3 is used, clock pulse signals CPa, CPb are inputted in place of the clock pulses CP. Figure 10(b) shows an example of output waveforms, i.e. row electrode driving waveforms where L = 3.

Data b, shift clock pulses (CP or CPa, CPb) and latch pulses (LP) are commonly inputted to two row voltage generating circuits 5c, 5d. Into the row voltage generating circuit 5c, a row electrode selection pattern is inputted as data a. Into the other row voltage generating circuit 5d, a different row electrode selection pattern is inputted as data a'. An input of the data a may be the same as an input of the data a'.

With the above-mentioned arrangement connection, the same operation as in the case of above-mentioned embodiment is obtainable, and

the display panel can be driven while the row electrodes of a 2L number are simultaneously selected. In the same idea, when two or more row voltage generating circuits are used, row electrodes of 3L, 4L, ..., can be simultaneously selected.

As described above, according to the present invention, the liquid crystal display apparatus comprises a row electrode selection means to successively address each simultaneously selected row electrodes and a row voltage generating means to apply voltages based on the corresponding data in row electrode selection pattern signals to the each row electrodes selected by the row electrode selecting means. Accordingly, in a case of driving the liquid crystal display apparatus by simultaneously selecting an L number of row electrodes, a row electrode driving circuit having a simpler structure can be realized in comparison with a case of controlling respectively voltage polarities applied to each N number of row electrodes.

Further, by constructing the liquid crystal display apparatus of the present invention to include a row voltage generating circuit which comprises a row electrode pattern setting means to output row electrode selection pattern signals corresponding to voltages applied to each row electrodes selected, and a row electrodes driving means to apply voltages based on patterns determined by the row electrode pattern setting means, to the each row electrodes addressed by the row electrode selection means, it is possible to easily set desired voltage patterns to be applied to an L number of simultaneously selected row electrodes.

Further, by constructing the liquid crystal display apparatus to include a selection signal parallel output device which makes selection signals corresponding to row electrodes selected active, and makes selection signals corresponding to the row electrodes other than the selected row electrodes non-active, the selection signals being supplied to the liquid crystal driving circuit, and a voltage setting signal parallel output device to supply, as voltage setting signals, the corresponding data in row electrode selection pattern signals, corresponding to each row electrodes to be selected, to the liquid crystal driving circuit, the liquid crystal driving circuit can easily determine voltage patterns to be applied to each row electrodes to be selected and the other each row electrodes.

When the number of parallel outputs of the selection signal parallel output device is made equal to the number of parallel outputs of the voltage setting signal parallel output device in the liquid crystal display apparatus, the construction for simultaneously selecting row electrodes can be simplified.

When the number of parallel outputs of the selection signal parallel output device and the number of parallel outputs of the voltage setting signal parallel output device are made equal to the number of all row electrodes N, the construction for simultaneously selecting row electrodes can be simplified.

By constructing the liquid crystal display apparatus to include a latch circuit which latches selection signal patterns based on selection signals supplied to the liquid crystal driving circuit to output the latched patterns to the liquid crystal driving circuit, and a latch circuit which latches the row electrode pattern signals to output the latched signals to the liquid crystal driving circuit, the row electrode selection patterns to be applied to each row electrodes to be selected and the other each row electrodes can be certainly supplied to the liquid crystal driving circuit.

By constructing the liquid crystal display apparatus to include a shift register for shifting data indicative of an active period of selection signals and a shift register for shifting a train of the row electrode selection patterns, data can be supplied with a small bit width at an input time. The above structure can reduce the number of input pins of a driver.

By constructing the liquid crystal display apparatus so that the frequency of a shift clock to be supplied to the shift register in the voltage setting signal parallel output device is higher than the frequency of a shift clock to be supplied to the shift register in the selection signal parallel output device, a voltage pattern which is different from a voltage pattern applied to the row electrodes constituting a row electrode subgroup can be easily applied to the row electrodes constituting a row electrode subgroup to the selected next.

By constructing the liquid crystal display apparatus to include a voltage setting signal parallel output device having parallel outputs whose number is as natural number times as the number of simultaneously selected row electrodes L, and a selection signal parallel output device having parallel outputs whose number is as natural number times as the number of row electrode subgroups M, desired voltage patterns can be formed for an L number of row electrodes which are simultaneously selected, while the construction is more simplified. Further, it is possible to drive a plurality of pictures.

By constructing the liquid crystal display apparatus to include a voltage setting signal parallel output device having parallel outputs which are equal to the number of simultaneously selected row electrodes L and a selection signal parallel output device having parallel outputs which are equal to the number of row electrode subgroups M, desired voltage patterns can be formed for an L number of row electrodes which are simultaneously selected, while the construction is more simplified.

By constructing the liquid crystal display apparatus to include a latch circuit which latches row electrode pattern signals by latch pulses in synchronism with a timing to select and switch groups consisting of simultaneously selected row electrodes, and outputs the latched signals to the liquid crystal driving circuit, row electrode selection patterns to be applied to row electrode subgroups can be certainly supplied to the liquid crystal driving circuit.

By constructing the liquid crystal display apparatus to include a shift register for shifting a train of row electrode selection patterns, influence of noises of the liquid crystal display element to a device for setting the row electrode selection patterns can be reduced.

By constructing the liquid crystal display apparatus to include a shift register which shifts data indicative of an active period of selection signals by latch pulses, and supplies the latched data to the liquid crystal driving circuit, influence of noises of the liquid crystal element to a device for setting the row electrode selection patterns can be reduced.

By constructing the liquid crystal display apparatus to include a latch circuit which latches selection signal patterns by latch pulses, and outputs the latched signal patterns to liquid crystal driving circuit, information indicative of row electrode subgroups to be selected can be certainly supplied to the liquid crystal driving circuit.

Further, by constructing the liquid crystal display apparatus to include a shift register which shifts data indicative of an active period of selection signals, and supplies the shifted data to a latch circuit, influence of noises of the liquid crystal display element to a device for setting the row electrode setting patterns can be reduced.

Claims

1. A liquid crystal display apparatus comprising:

a liquid crystal element adapted to be driven by driving a plurality of row electrodes and column electrodes in which a plurality of row electrodes are simultaneously selected,

a column voltage generating circuit to apply to each column electrodes voltages based on orthogonal conversion signals which are obtained by converting, with use of an orthogonal function, picture signals corresponding to the positions of the simultaneously selected row electrodes of the display element, and

a row voltage generating circuit to apply voltages based on row electrode selection pattern signals formed with an orthogonal function to the simultaneously selected row electrodes, characterized in that

the row voltage generating circuit comprises:

a row electrode selection means to address sequentially the each simultaneously selected row electrodes, and

a row voltage generating means to apply voltages in response to the corresponding data in the row electrode selection pattern signals to the each row electrodes selected by the row electrode selection means.

2. The liquid crystal display apparatus according to Claim 1, wherein the row voltage generating means comprises a row electrode selection pattern setting means to output row electrode selection pattern signals corresponding to voltages applied to each row electrodes to be selected, and a row electrode driving means to apply voltages in response to patterns set by the row electrode selection pattern setting means to the each row electrodes addressed by the row electrode selection means.

3. The liquid crystal display apparatus according to Claim 2, wherein

the row electrode driving means includes a liquid crystal driving circuit which receives an N number (N: the total number of the row electrodes) of selection signals each corresponding to each of the row electrodes; which receives an N number of voltage setting signals each corresponding to the each of the row electrodes; and which applies row voltages corresponding to the voltage setting signals to the row electrodes determined by the selection signals,

the row electrode selection means includes a selection signals parallel output device which renders each of the selection signals corresponding to each of the selected row electrodes to be active and renders each of the selection signals corresponding to each of the non-selected row electrodes to be non-active whereby each of the selection signals is supplied to the liquid crystal driving circuit, and

the row electrode selection pattern setting means includes a voltage setting signal parallel output device to supply, as voltage setting signals, the corresponding data in the row electrode selection pattern signals corresponding to the each selected row electrodes to the liquid crystal driving circuit.

4. The liquid crystal display apparatus according to Claim 3, wherein the number of parallel outputs from the selection signal parallel out-

put device is equal to the number of parallel outputs from the voltage setting signal parallel output device.

5. The liquid crystal display apparatus according to Claim 4, wherein the number of the parallel outputs from the selection signal parallel output device and the number of the parallel outputs from the voltage setting signal parallel output device are equal to the total number N of the row electrodes.

6. The liquid crystal display apparatus according to Claim 4, wherein

the selection signal parallel output device includes a latch circuit which latches selection pattern signals based on selection signals to be supplied to the liquid crystal driving circuit, by means of latch pulses which are in synchronism with a timing for switching the selection of a group consisting of the simultaneously selected row electrodes, whereby the latched selection signal patterns are outputted to the liquid crystal driving circuit, and

the voltage setting signal parallel output device includes a latch circuit which latches the row electrode selection pattern signals by means of the latch pulses to output the latched signals to the liquid crystal driving circuit.

7. The liquid crystal display apparatus according to Claim 6, wherein

the selection signal parallel output device includes a shift register which shifts data indicative of an active period of the selection signals and which has a tap output for each stage connected to the latch circuit, and

the voltage setting signal parallel output device includes a shift register which shifts a train of the row electrode selection patterns and which has a tap output for each stage connected to the latch circuit.

8. The liquid crystal display apparatus according to Claim 7, wherein the frequency of a shift clock to be supplied to the shift register of the voltage setting signal parallel output device is higher than the frequency of a shift clock to be supplied to the shift register of the selection signal parallel output device.

9. The liquid crystal display apparatus according to Claim 3, wherein

the selection signal parallel output device has parallel outputs whose number is a natural number multiplied by M where M is the number of groups consisting of the simultaneously selected row electrodes, and

the voltages setting signal parallel output device has parallel outputs whose number is a natural number multiplied by L where L is the number of row electrodes which form each groups.

10. The liquid crystal display apparatus according to Claim 9, wherein

the selection signal parallel output device has an M number of parallel outputs where M is the number of groups consisting of the simultaneously selected row electrodes, and

the voltage setting signal parallel output device has an L number of parallel outputs where L is the number of row electrodes which form each groups.

11. The liquid crystal display apparatus according to Claim 9, wherein the voltage setting signal parallel output device includes a latch circuit which latches the row electrode selection pattern signals by means of latch pulses which are in synchronism with a timing of switching the selection of the groups consisting of the simultaneously selected row electrodes whereby the latched signals are outputted to the liquid crystal driving circuit.

12. The liquid crystal display apparatus according to Claim 11, wherein the voltage setting signal parallel output device includes a shift register which shifts a train of the row electrode selection patterns and which has a tap output for each stage connected to the latch circuit.

13. The liquid crystal display apparatus according to Claim 9, wherein the selection signal parallel output device includes a shift register which shifts data indicative of an active period of the selection signals by means of latch pulses which are in synchronism with a timing of switching the selection of the groups consisting of the simultaneously selected row electrodes, and the shift register supplies, as the selection signal for each of the groups, a tap output for each stage to the liquid crystal driving circuit.

FIGURE 1

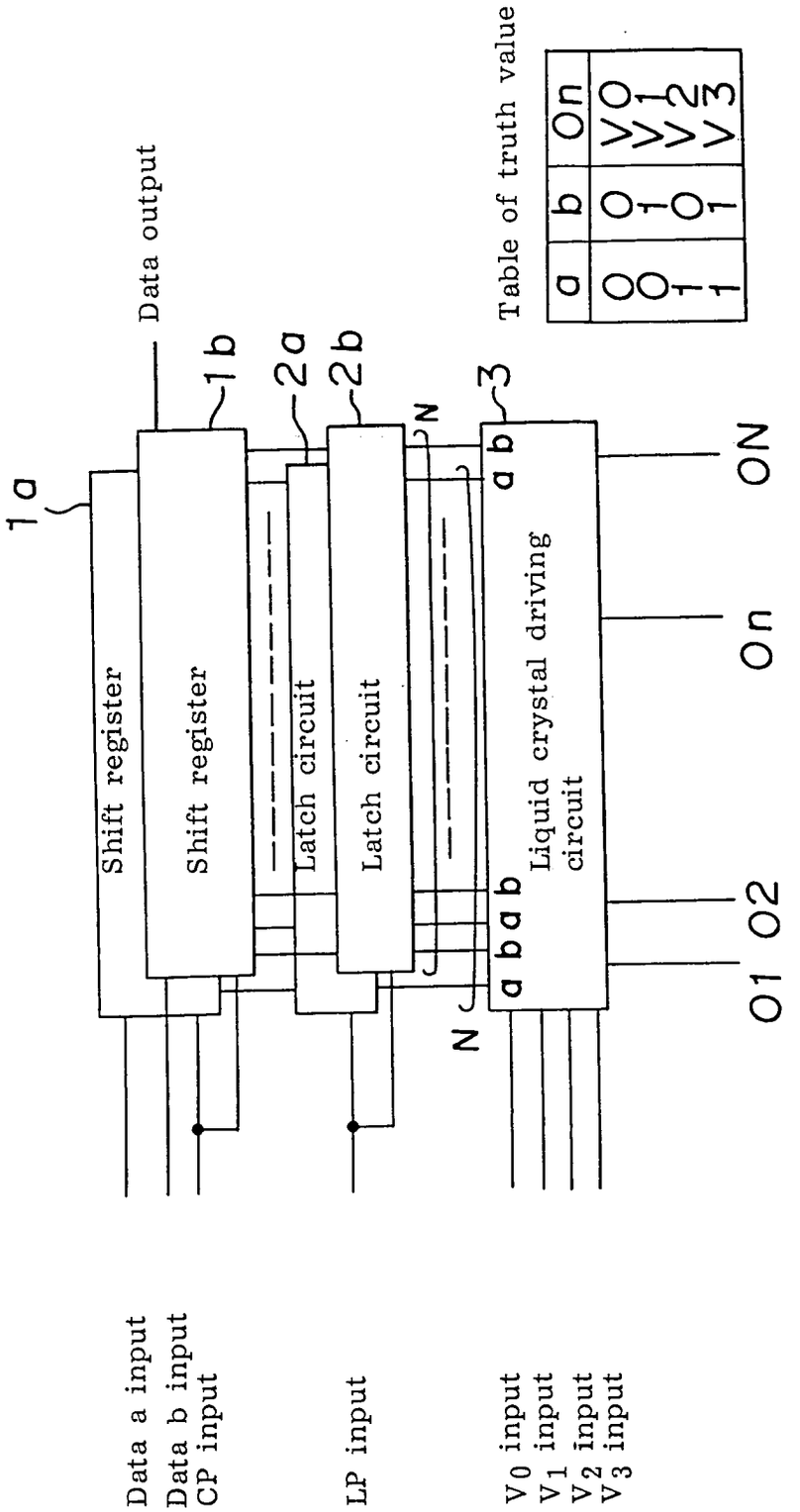
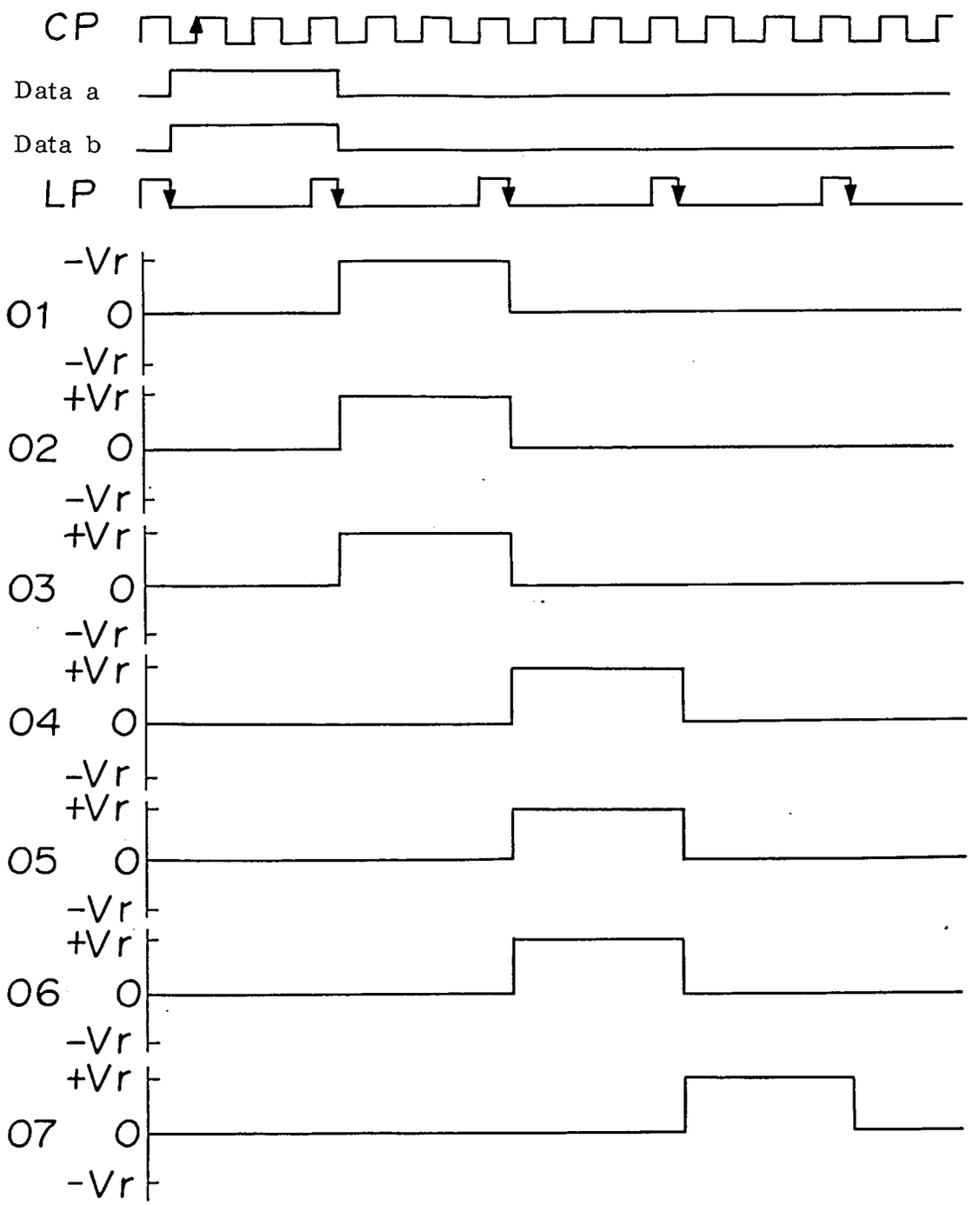


Table of truth value

a	b	On
0	0	V0
0	1	V1
1	0	V2
1	1	V3

FIGURE 2


CP
Data a
Data b
LP
-Vr
01
0
-Vr
+Vr
02
0
-Vr
+Vr
03
0
-Vr
+Vr
04
0
-Vr
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05
0
-Vr
+Vr
06
0
-Vr
+Vr
07
0
-Vr

FIGURE 3

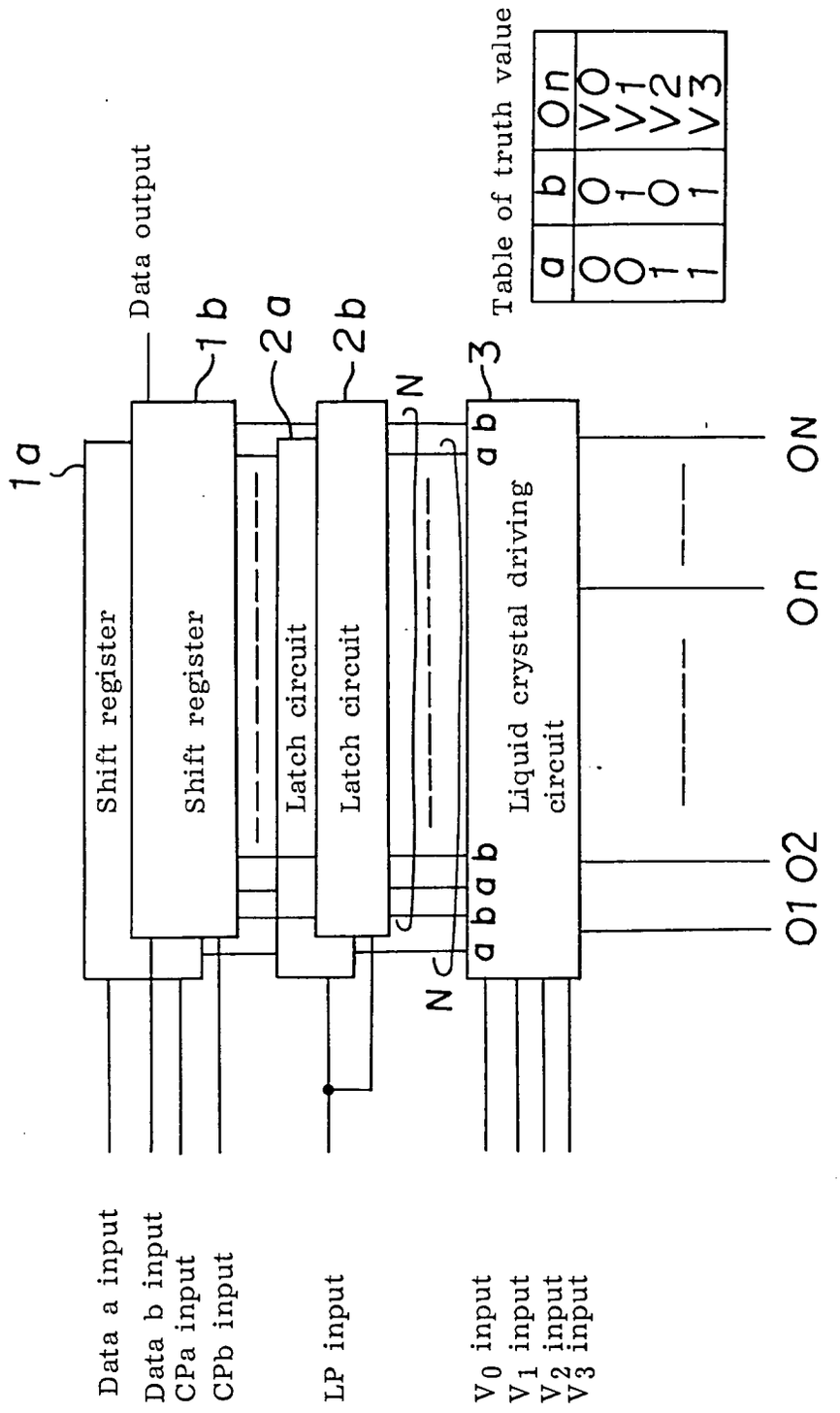
Data output
1a
1b
2a
2b
3
N
Shift register
Shift register
Latch circuit
Latch circuit
Liquid crystal driving circuit
a b
a b a b
Data a input
Data b input
CPa input
CPb input
LP input
V0 input
V1 input
V2 input
V3 input
O1 O2
On
ON
Table of truth value
a b On
0 0 V0
0 1 V1
1 0 V2
1 1 V3

FIGURE 4

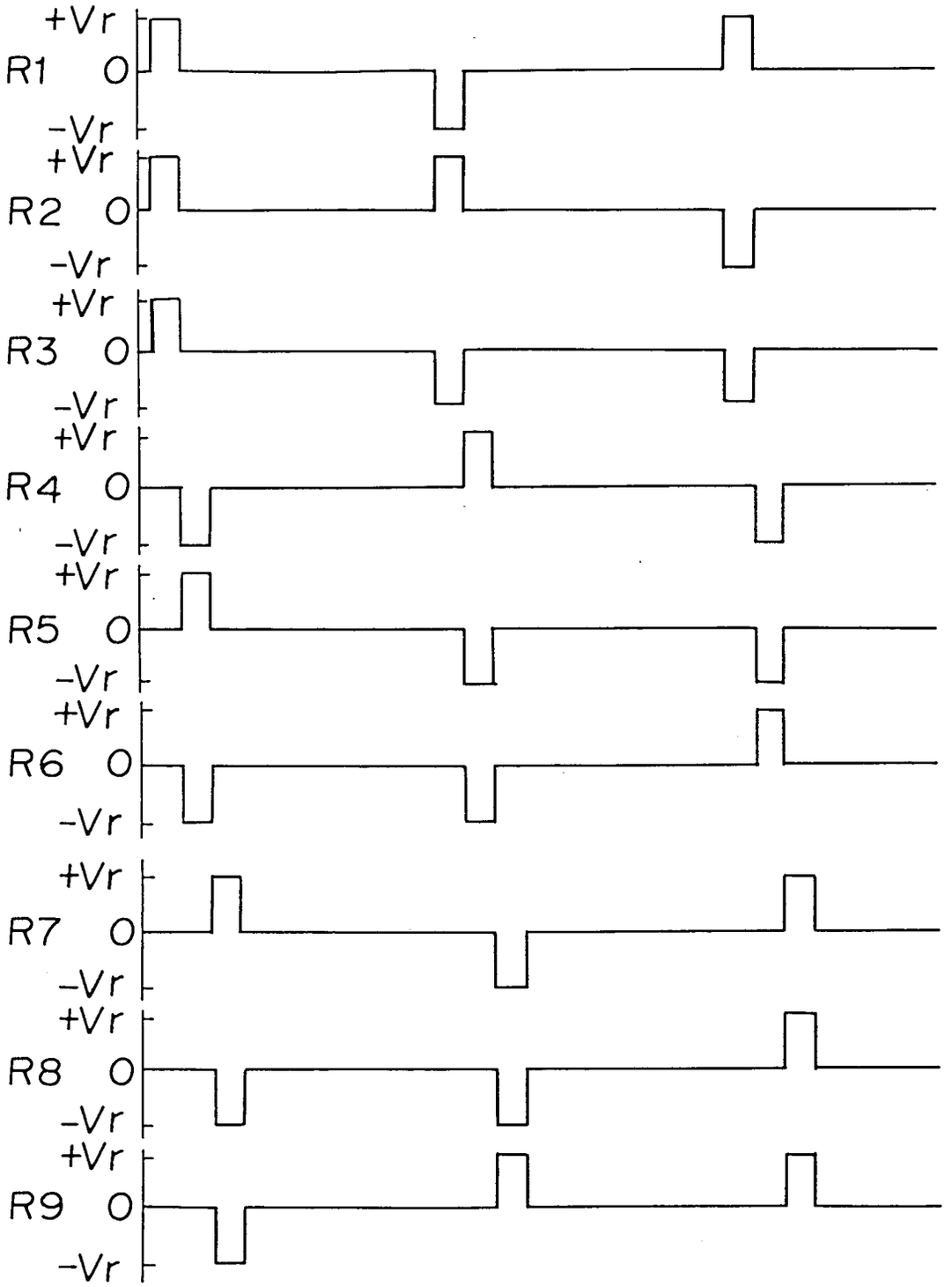
+Vr
R1 0
-Vr
+Vr
R2 0
-Vr
+Vr
R3 0
-Vr
+Vr
R4 0
-Vr
+Vr
R5 0
-Vr
+Vr
R6 0
-Vr
+Vr
R7 0
-Vr
+Vr
R8 0
-Vr
+Vr
R9 0
-Vr

FIGURE 5

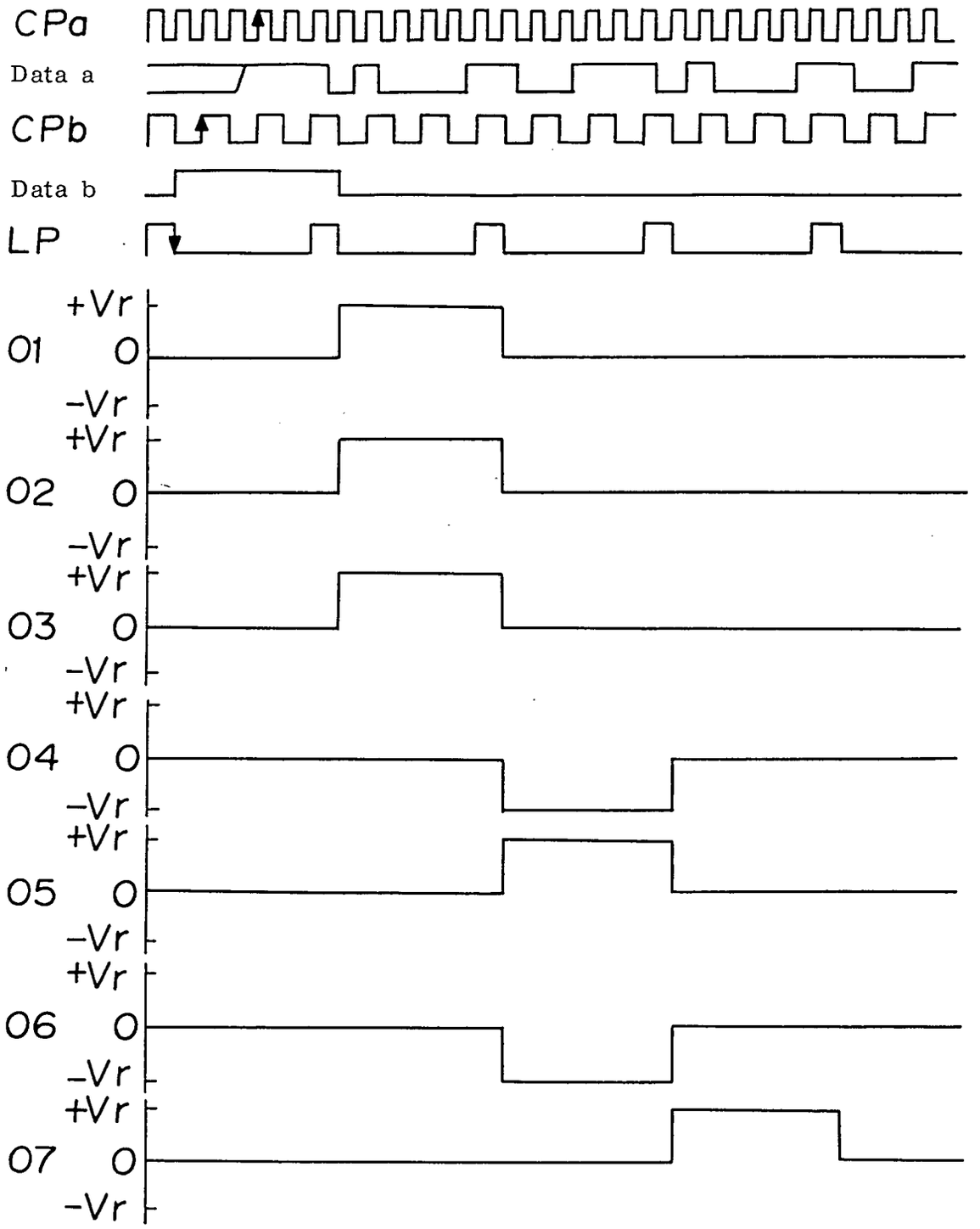
CPa
Data a
CPb
Data b
LP
+Vr
01
0
-Vr
+Vr
02
0
-Vr
+Vr
03
0
-Vr
+Vr
04
0
-Vr
+Vr
05
0
-Vr
+Vr
06
0
-Vr
+Vr
07
0
-Vr

FIGURE 6

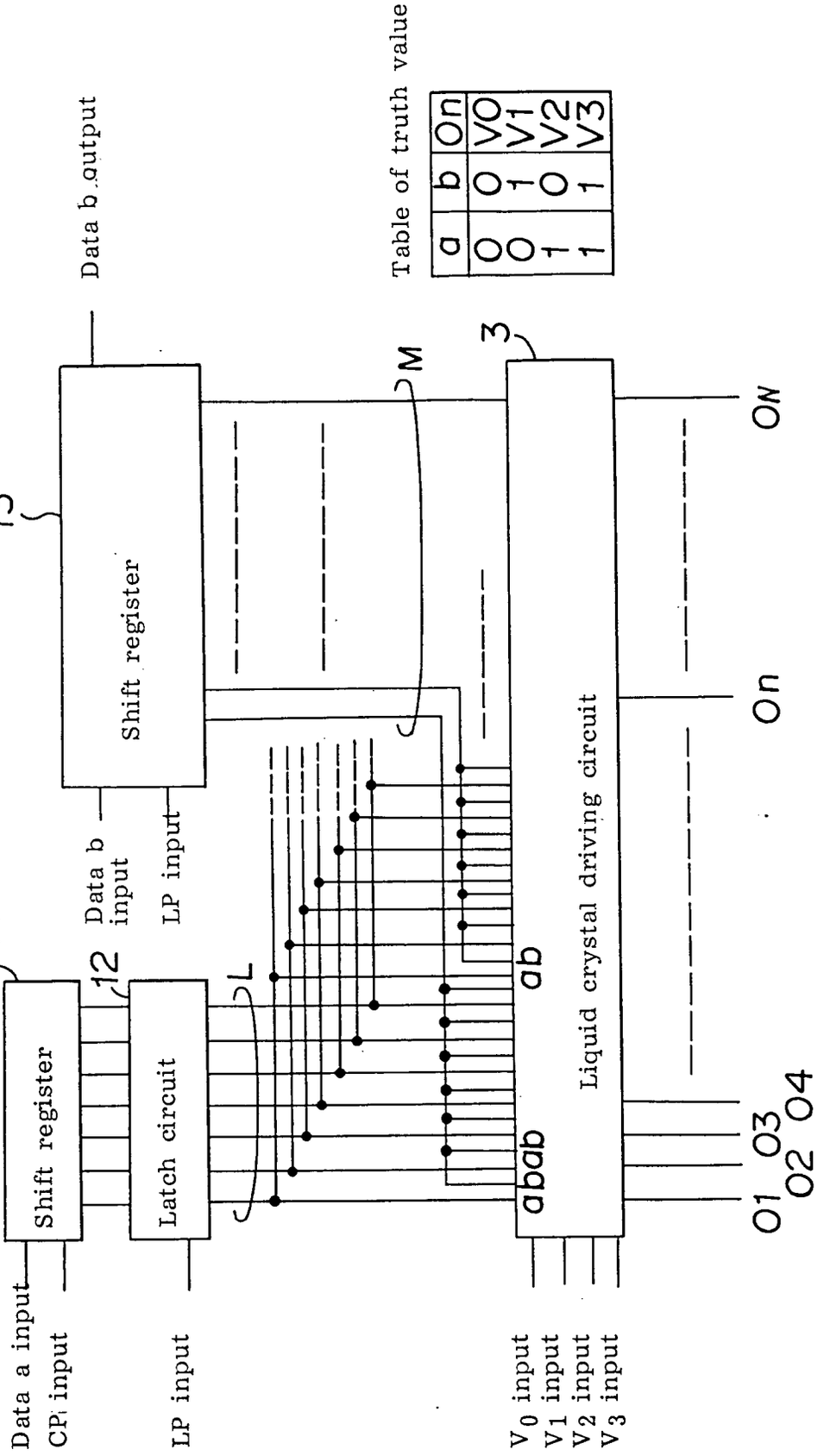
Table of truth value
a b On
0 0 V0
0 1 V1
1 0 V2
1 1 V3
Data b output
Shift register
13
M
3
ON
On
11
12
Data b input
LP input
L
Shift register
Latch circuit
ab
abab
Liquid crystal driving circuit
01 03
02 04
Data a input
CP input
LP input
V0 input
V1 input
V2 input
V3 input

FIGURE 7

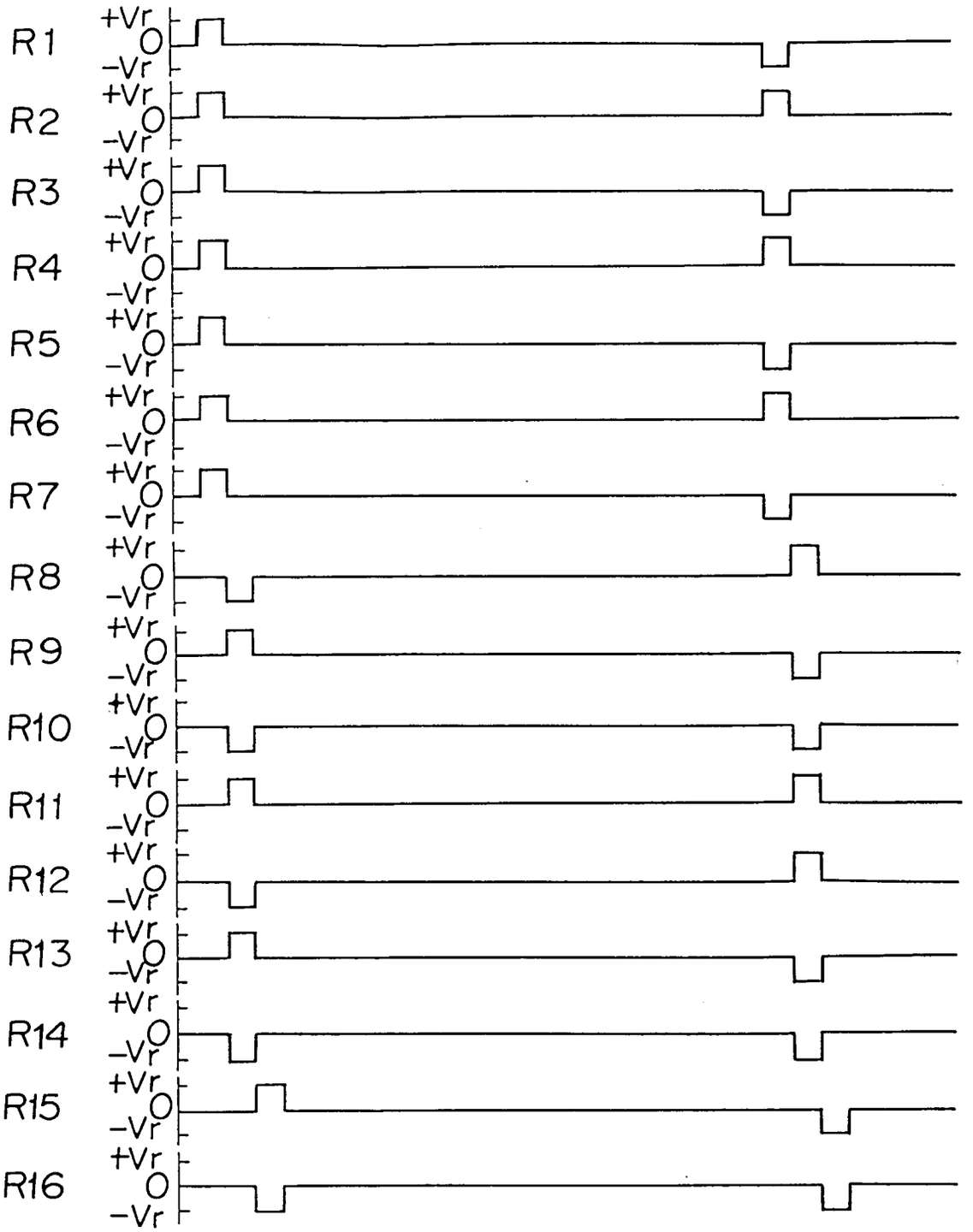

FIGURE 8

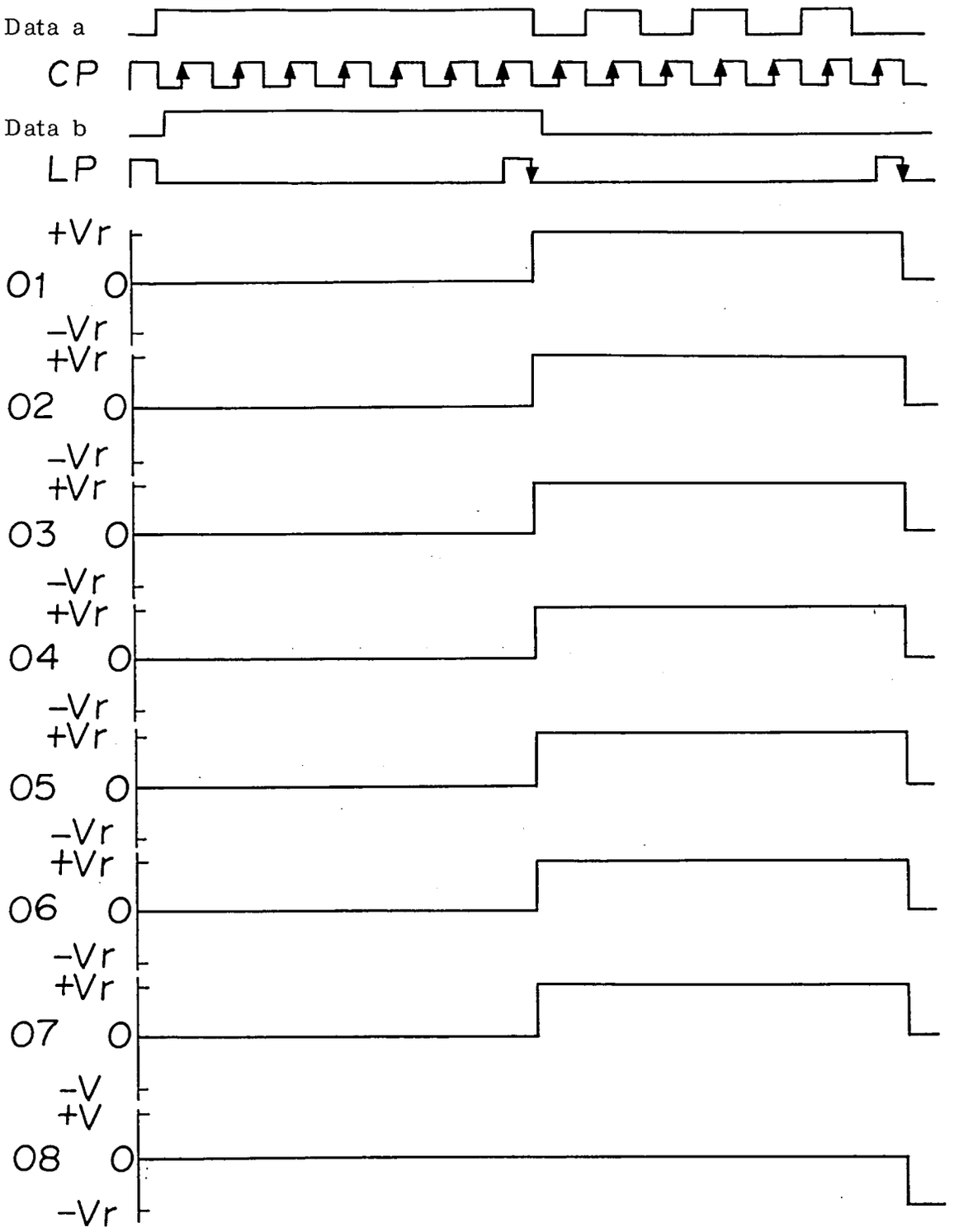
Data a
CP
Data b
LP
+Vr
01
0
-Vr
+Vr
02
0
-Vr
+Vr
03
0
-Vr
+Vr
04
0
-Vr
+Vr
05
0
-Vr
+Vr
06
0
-Vr
+Vr
07
0
-V
+V
08
0
-Vr

FIGURE 9 (a)

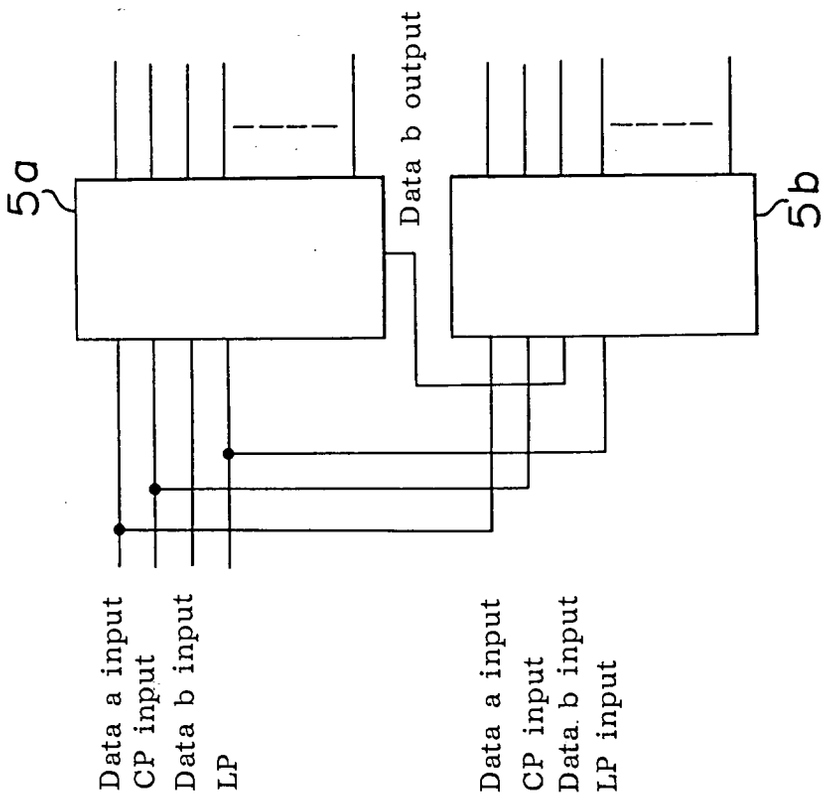

FIGURE 9 (b)

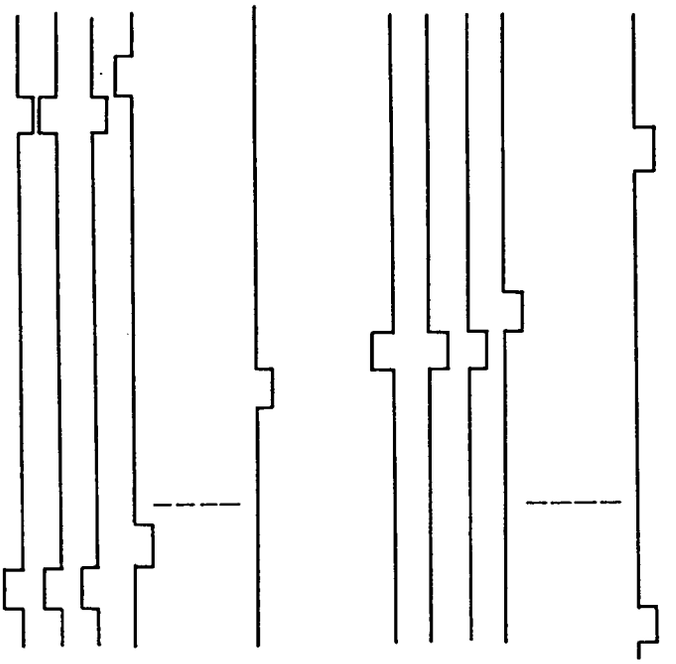

FIGURE 10(a)

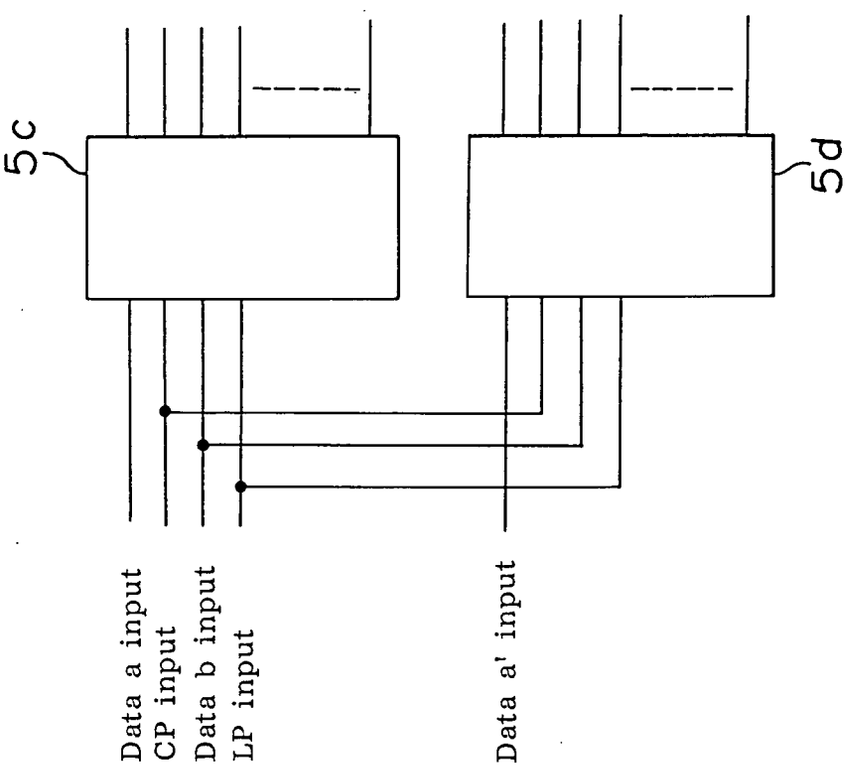

FIGURE 10(b)

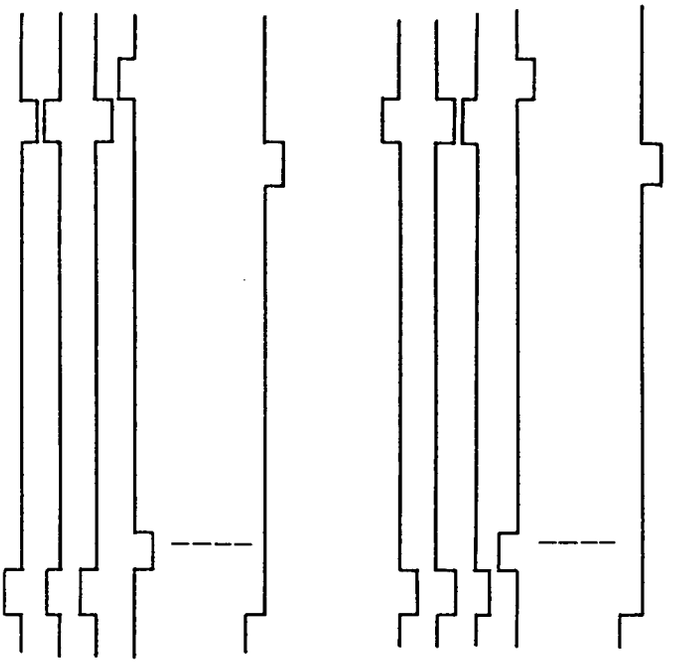

FIGURE 11

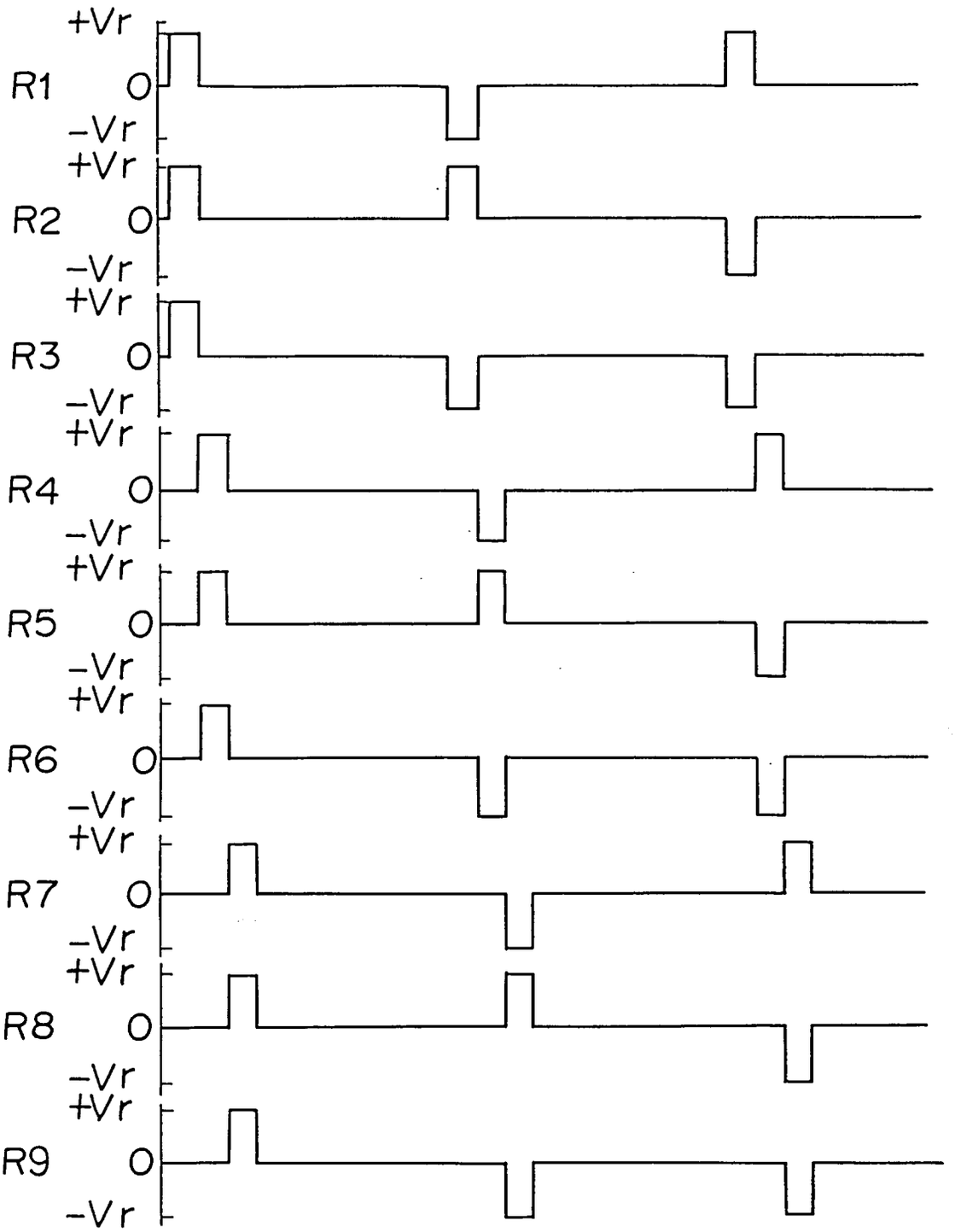
+Vr
R1
0
-Vr
+Vr
R2
0
-Vr
+Vr
R3
0
-Vr
+Vr
R4
0
-Vr
+Vr
R5
0
-Vr
+Vr
R6
0
-Vr
+Vr
R7
0
-Vr
+Vr
R8
0
-Vr
+Vr
R9
0
-Vr

FIGURE 12(a)

$$Vr \cdot \begin{bmatrix} 1 & 1 & 1 & 1 \\ 1 & -1 & 1 & -1 \\ 1 & 1 & -1 & -1 \\ 1 & -1 & -1 & 1 \end{bmatrix}$$

FIGURE 12(b)

$$Vr \cdot \begin{bmatrix} 1 & 1 & 1 & -1 \\ 1 & 1 & -1 & 1 \\ 1 & -1 & -1 & -1 \\ -1 & 1 & -1 & -1 \end{bmatrix}$$

FIGURE 12(c)

$$Vr \cdot \begin{bmatrix} 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\ 1 & -1 & 1 & -1 & 1 & -1 & 1 & -1 \\ 1 & 1 & -1 & -1 & 1 & 1 & -1 & -1 \\ 1 & -1 & -1 & 1 & 1 & -1 & -1 & 1 \\ 1 & 1 & 1 & 1 & -1 & -1 & -1 & -1 \\ 1 & -1 & 1 & -1 & -1 & 1 & -1 & 1 \\ 1 & 1 & -1 & -1 & -1 & -1 & 1 & 1 \\ 1 & -1 & -1 & 1 & -1 & 1 & 1 & -1 \end{bmatrix}$$

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 94 10 4742

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
A	EP-A-0 507 061 (IN FOCUS SYSTEMS) * abstract; figures 10-14 * * page 17, line 40 - page 20, line 58 *	1	G09G3/36
A	EP-A-0 522 510 (ASAHI GLASS COMPANY) * abstract; figures 6,13 * * page 21, line 30 - page 22, line 22 *	1	
D,A	& JP-A-6 027 904 (...)	1	
A	DISPLAYS, vol.14, no.2, 1993, JORDAN HILL, OXFORD, GB pages 74 - 85 T. SCHEFFER ET AL. 'Active Addressing of STN displays for high-performance video applications' * the whole document *	1	

TECHNICAL FIELDS SEARCHED (Int.Cl.5)

G09G

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	1 July 1994	Saam, C

CATEGORY OF CITED DOCUMENTS

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