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(54) **Integrated analog-digital boundary interface.**

(57) Invention relates to an integrated analog-digital boundary interface for time multiplexed communication systems. The analog-digital boundary interface consists of an integrated AFE circuit (17) in which functioning of A/D and D/A converters are combined. The solution according to the invention is efficient and advantageous from the point of view of interference control and complexity.

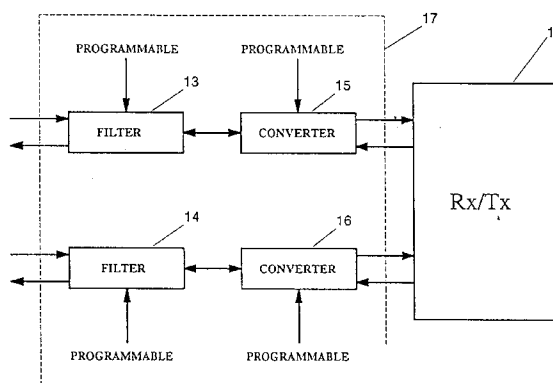


Fig. 4

This invention relates to an integrated analog-digital boundary interface for time multiplexed communication systems.

In digital communication applications, for example GSM or digital AMPS mobile phones, there is an analog-digital boundary interface on carrier or intermediate frequency. At this boundary interface, both A/D and D/A conversions are carried out for symbol signals.

In time multiplexed digital cellular systems (TDMA, Time Division Multiple Access), such as GSM and digital AMPS, transmitting and receiving alternate in time slots. In digital transmitters one or more D/A converters are used and likewise in the receivers one or more A/D converters, are used.

The prior art is described with reference to the accompanying drawings in which:

Figure 1 is a block diagram of a prior art digital carrier frequency receiver.

Figure 2 is a block diagram of a prior art digital carrier frequency transmitter.

Figure 3 is a block diagram of a prior art Analog Front End (AFE) circuit used in digital communication systems.

The diagram shown in figure 1 is a block diagram of a prior art digital carrier frequency receiver. An incoming carrier frequency signal is brought to A/D converters 3, 4 through filters 1, 2. The converted signal is brought to a digital receiver 5.

The diagram shown in figure 2 is a block diagram of a prior art digital carrier frequency transmitter. A digital transmitter 6 transmits the signal to D/A converters 7, 8. The converted signal is brought to filters 9, 10, which output the carrier frequency signal.

The diagram shown in figure 3 is a block diagram of a prior art digital communication system's Analog Front End (AFE) circuit. The filters 1, 2, 9, 10 and converters 3, 4, 7, 8 have been integrated on the common AFE integrated circuit (IC) 12. The digital receiver/transmitter unit is marked with reference numeral 11.

In the Analog Front End (AFE) circuit 12 there are one or more A/D converters 3, 4 in a receiver branch and one or more D/A converters 7, 8 in a transmitter branch. In the same circuit there are also typically receiver filters 1, 2 and corresponding transmitter filters 9, 10 for the intermediate frequency carrier. As the circuit is commonly integrated with CMOS technology, all the functions can be laid out on the same integrated circuit 12. This takes up a lot of the chip area of the circuit 12. A complex circuit causes a lot of coupling interference and noise and makes the circuit itself sensitive to other interference sources.

According to the present invention there is provided an integrated analog-digital boundary interface having a circuit for transmitting and receiving signals in burst mode during respective predetermined time slots comprising a converter programmable to func-

tion as an A/D converter during periods corresponding to the predetermined receiving time slots and as a D/A converter during periods corresponding to the predetermined transmitting time slots.

An advantage of this invention is that by using the respective outputting and receiving periods a single programmable converter can be utilised as an A/D converter during a first period and a D/A converter during a second period with a beneficial reduction in the number of components used in the circuit board. The reduction in complexity also alleviates the previously mentioned interference problems.

The analog-digital boundary interface may further include a programmable filter. This further reduces the number of components with additional improvements in interference and space saving.

An embodiment of the present invention will now be described with reference to the accompanying drawings in which:

Figure 4 is a block diagram of an Analog Front End (AFE) circuit of a digital communication system according to an embodiment of the present invention.

Figure 5 is a block diagram of a Serial Approximation Register type A/D converter according to an embodiment of the present invention.

Figure 6a is a block diagram of a programmable Serial Approximation Register type converter capable of functioning as an A/D converter.

Figure 6b is a block diagram corresponding to that of Figure 6a with the converter functioning as a D/A converter.

The diagram shown in figure 4 is a block diagram of an Analog Front End circuit of a communication system according to an embodiment of the present invention. The programmable filters 13, 14 and programmable converters 15, 16 are integrated to the same Analog Front End integrated circuit 17. The digital receiver/transmitter unit is marked with the reference numeral 11.

In time multiplexed communication systems the transmitting and receiving operations can be implemented using some of the same circuit elements of the integrated Analog Front End circuit 17 in both the receiving branch and the transmitting branch.

A good quality D/A converter is an integral component of a Serial Approximation Register type A/D converter. In this application the transmitter and the receiver operate in separate time slots (time multiplexed), so only one good quality programmable converter 15, 16 is needed in this circuit for each pair of conventional A/D and D/A converters.

The diagram shown in figure 5 is a block diagram of a Serial Approximation Register (SAR) type A/D converter. The SAR-type A/D converter comprises a D/A converter 18, a serial approximation register 19 and an operational amplifier (comparator) 20.

The diagram shown in figure 6 is a block diagram of a programmable, generic Serial Approximation

Register type converter. The programmable SAR-type converter 15, 16 comprises a D/A converter 18, a serial approximation register 19 and an operational amplifier (comparator) 20.

During receiving periods the generic converter 15, 16 is programmed as an A/D converter. There can be several converters 15, 16 operating in parallel. During transmitting periods the converter 15, 16 functions as a D/A converter. Generality causes an inevitable decrease in performance, but this can be compensated for in advance during the design phase. The programmable bi-directional converter 15, 16 also requires a larger area on the integrated circuit than a dedicated and optimized one-directional converter, but there is a significant total area saving in the system.

When the time division of the time multiplexed communication system is utilized at implementation level, some of the connections can be designed to be programmable, as shown previously, and their use can also be changed to comply with the requirements of a particular time slot. A considerable amount of circuit board or integrated circuit area can thereby be saved along with a reduction in the complexity and interference sensitivity of the circuit.

The branch filters 13, 14 are usually integrated by CMOS technology using Switched Capacitor (SC) technology. The frequency response of this kind of filter 13, 14 can be easily programmed and such methods are well known. A programmable, generic converter 15, 16 is connected to a programmable, generic filter 13, 14 by a switch network that is programmable to take a receiving or transmitting state. The time needed for the circuit to change from the receiving state to the transmitting state, or vice versa, is a fraction of the time available for this operation in, for example, GSM or digital AMPS type cellular systems.

The invention is not limited to carrier frequency or intermediate frequency applications, but is applicable to any time division communication system. The AFE circuit 17 can also provide other independent functions which this invention does not affect.

The communication system's time multiplexing is carried to implementation level by taking full advantage of the time slots allocated to the transmit and receive periods. In the AFE circuit 17 the surface area of the integrated circuit and cost is reduced by implementing both the carrier frequency filtration or the intermediate frequency filtration and the bi-directional conversions (A/D and D/A) with programmable, generic circuit element or elements. By utilising programmable elements in this manner, there is also less interference or noise than in prior art circuits, since there are less functioning circuit elements in use. In the AFE circuit 17 according to an embodiment of this invention there are no separate branches for receiving and transmitting as these functions are accomplished by the common programmable circuits.

The invention can be applied to any time division communication system, such as, for example, GSM or digital AMPS digital cellular applications. The invention is a cost-effective manner for the implementation of the above mentioned TDMA type systems.

Claims

1. An integrated analog-digital boundary interface having a circuit (17) for transmitting and receiving signals in burst mode during respective predetermined time slots comprising a converter (15,16) programmable to function as an A/D converter during periods corresponding to the predetermined receiving time slots and as a D/A converter during periods corresponding to the predetermined transmitting time slots..
2. An analog-digital boundary interface according to claim 1 wherein the converter comprises a plurality of programmable converters.
3. An analog-digital boundary interface according to claim 1 or claim 2 wherein the circuit further comprises a programmable filter (13, 14) for filtering signals received and transmitted by the circuit (17).
4. An analog-digital boundary interface according to any preceding claim wherein the interface forms part of a time division multiplexed communication system.
5. An analog-digital boundary interface according to claim 3 when dependent on claim 2 wherein a programmable filter is provided for each programmable converter.
6. An analog-digital boundary interface according to any preceding claim wherein the circuit is an analog front end circuit.

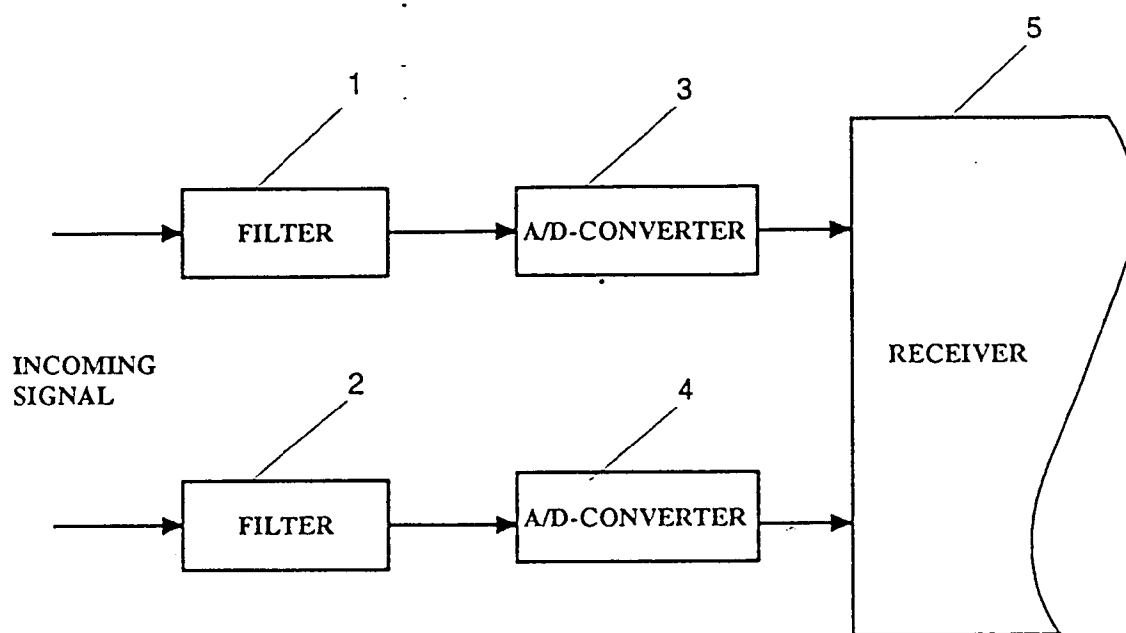


Fig. 1

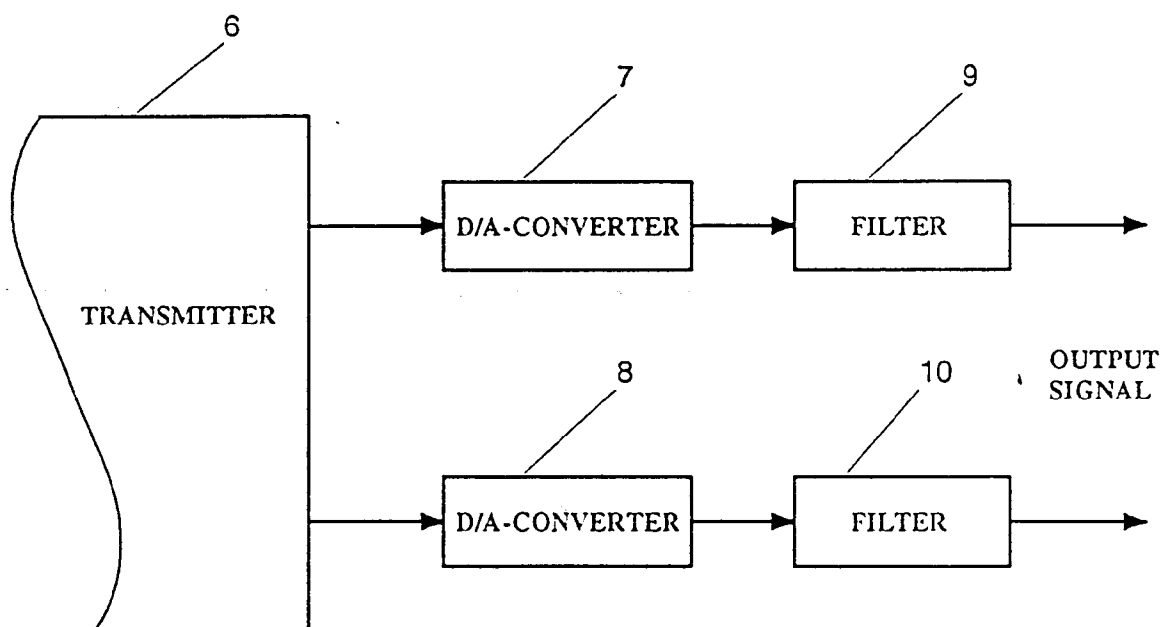


Fig. 2

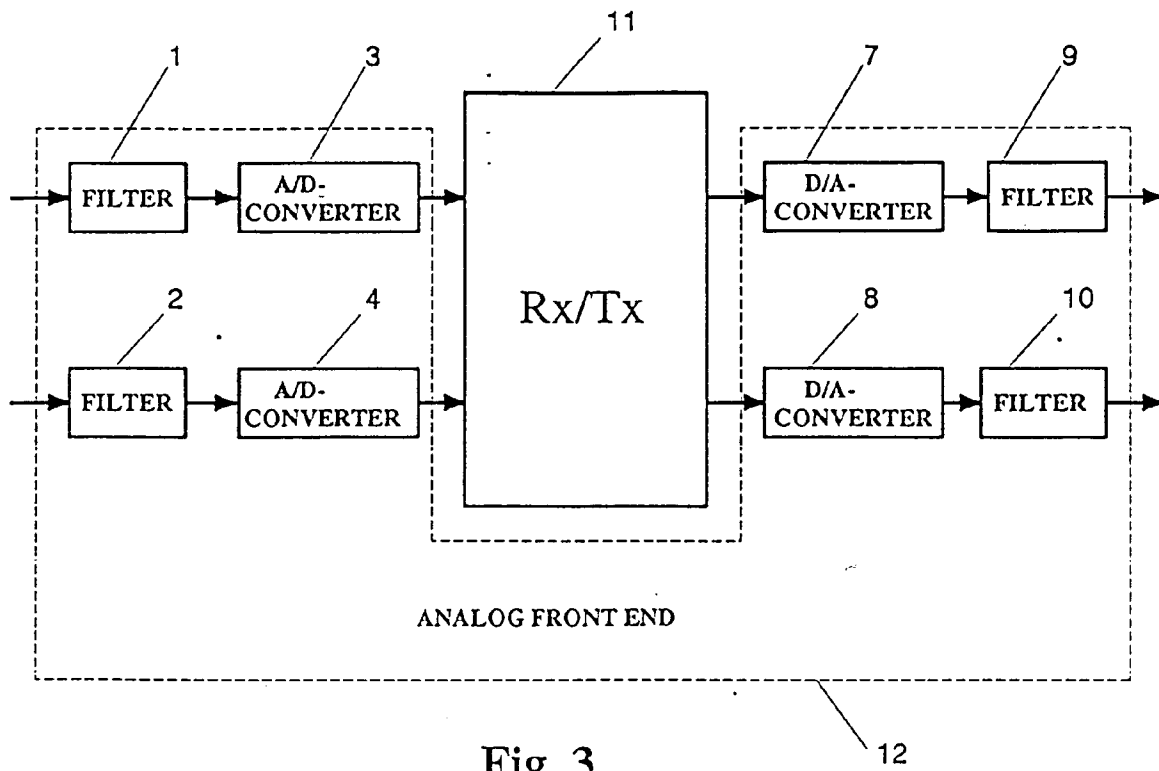


Fig. 3

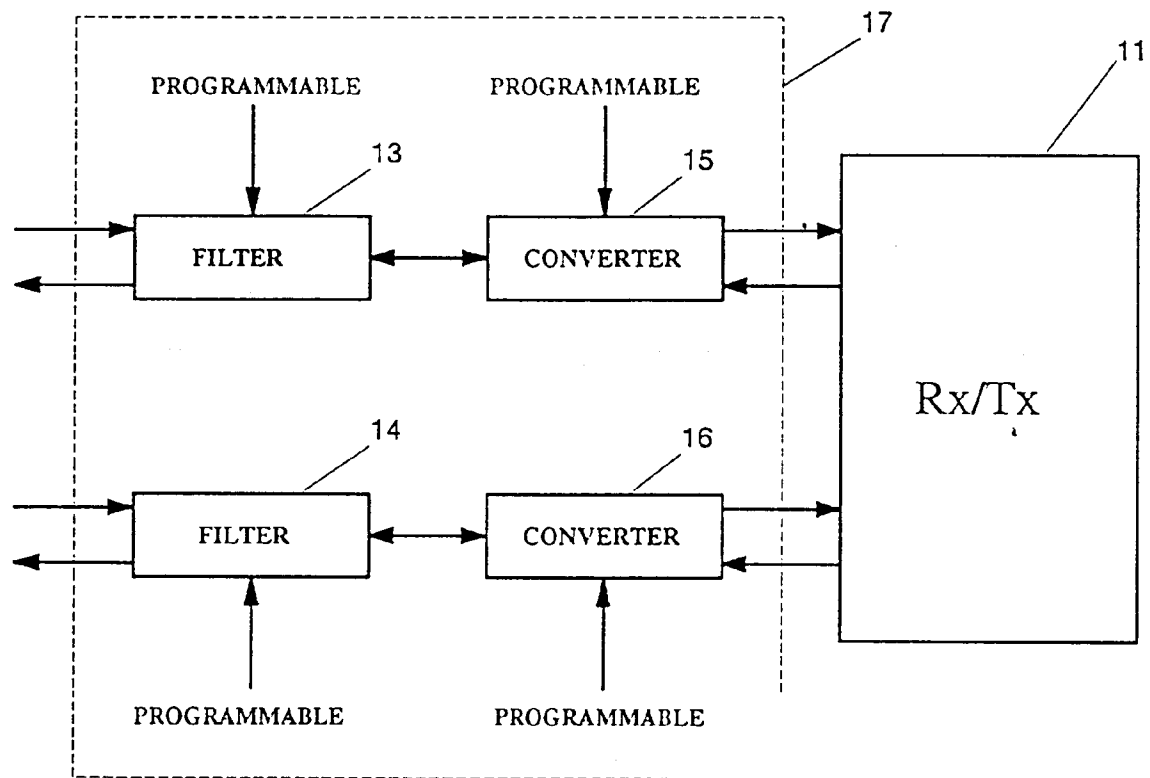


Fig. 4

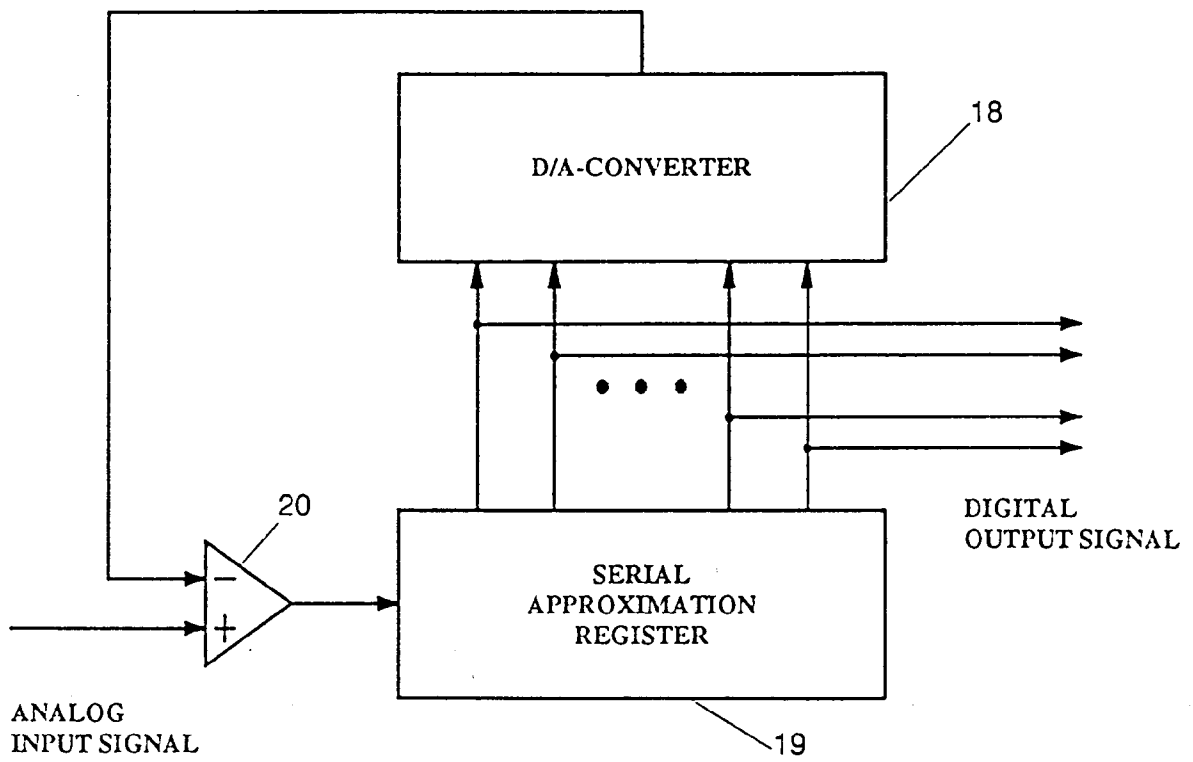


Fig. 5

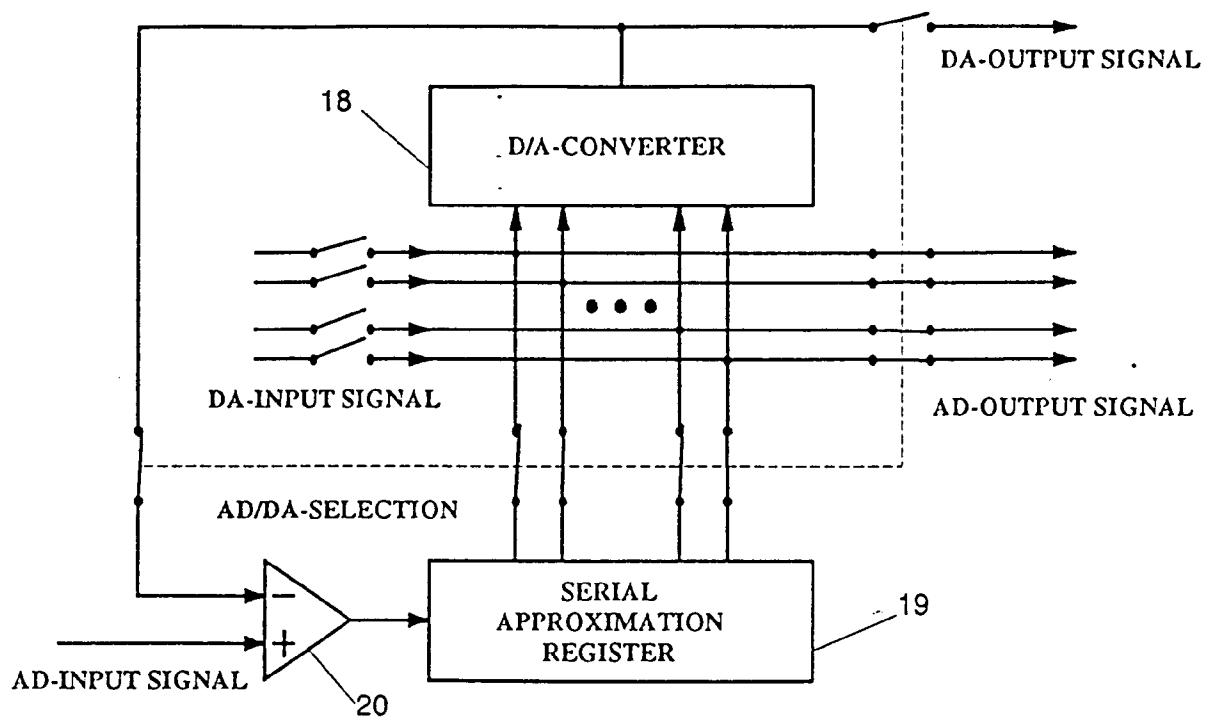


Fig. 6 a

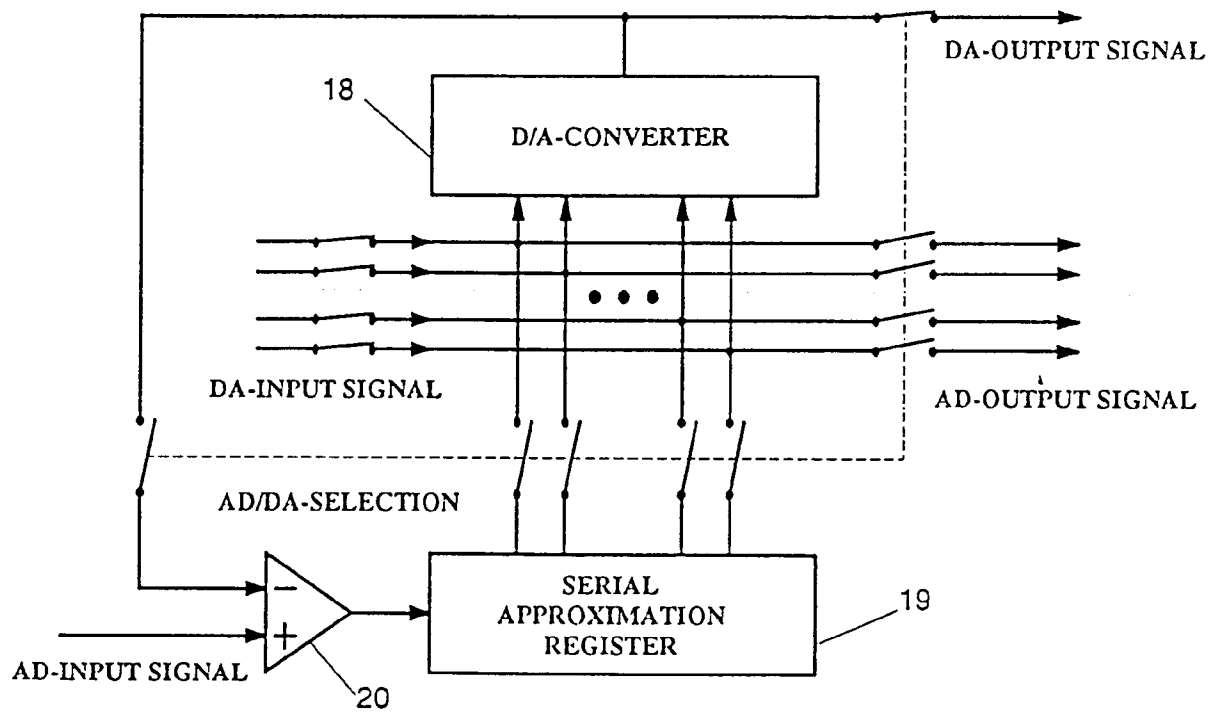


Fig. 6 b