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(54) Soft error immune CMOS static RAM cell

(57) Soft error immunity of a storage cell is greatly increased by division of a storage node into at least two portions and location of those portions on opposite sides of an isolation structure, such as a well of a conductivity type opposite to that of the substrate in which transistors of the memory cell may also be formed. The isolation structure thus limits collection of charge to only one of the portions of the storage node and reduces charge collection efficiency to a level where a critical amount of charge cannot be collected in all but a statistically negligible number of cases when such charge is engendered by impingement by ionizing radiation, such as energetic alpha particles. The layout of the memory cell having this feature also advantageously provides a simplified topology for the formation of additional ports comprising word line access transistors and bit lines.

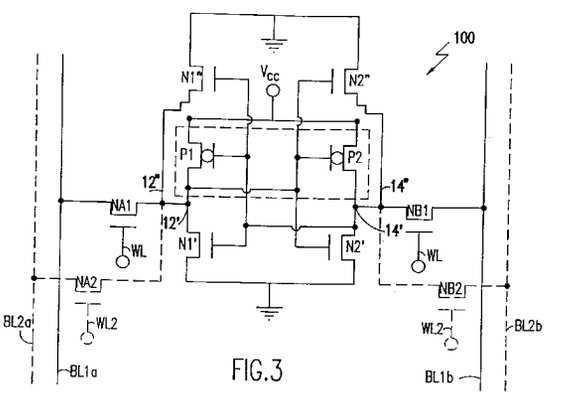

FIG.3

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EUROPEAN SEARCH REPORT

Application Number
EP 94 48 0022

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
A	IBM TECHNICAL DISCLOSURE BULLETIN, vol. 32, no. 8B, January 1990 NEW YORK US, pages 64-65, XP 000082487 'PROCESS FOR SELF-ALIGNED COMMON TWO-GATE, SIX-TRANSISTOR, COMPLEMENTARY METAL OXIDE SILICON STATIC RANDOM-ACCESS MEMORY' * the whole document *	1-13	G11C11/412

TECHNICAL FIELDS SEARCHED (Int.Cl.5)

G11C

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	26 January 1996	Burgaud, C

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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