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(54) Driving circuit for display apparatus.

(57) A driving circuit of the invention is used for driving a display apparatus which includes pixels and data lines for applying voltages to the pixels and which displays an image with multiple gray scales in accordance with video data consisting of a plurality of bits. The driving circuit includes : an oscillating voltage specifying section for specifying one of a plurality of oscillating signals having respective duty ratios which are different from each other in accordance with video data consisting of bits selected from the plurality of bits, and for outputting the specified oscillating signal T and an oscillating signal $\overline{T}$ which is obtained by inverting the specified oscillating signal T ; a gray-scale voltage specifying section for producing gray-scale voltage specifying signals which specify a first gray-scale voltage and a second gray-scale voltage among a plurality of gray-scale voltages supplied from a gray-scale voltage supply section, in accordance with video data consisting of bits other than the selected bits of the plurality of bits ; and an output section for outputting the first gray-scale voltage and the second gray-scale voltage specified by the gray-scale voltage specifying signals to the data lines, in accordance with the oscillating signal T and the oscillating signal $\overline{T}$.

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BACKGROUND OF THE INVENTION

1. Field of the Invention:

The present invention relates to a driving circuit for a display apparatus. More particularly, the present invention relates to a driving circuit for an active matrix type liquid crystal display apparatus which displays an image with multiple gray scales in accordance with digital video signals.

2. Description of the Related Art:

An active matrix type liquid crystal display apparatus includes a display panel and a driving circuit for driving the display panel. The display panel includes a pair of glass substrates and a liquid crystal layer formed between the pair of glass substrates. On one of the pair of glass substrates, a plurality of gate lines and a plurality of data lines are formed. The driving circuit is disposed for every pixel in the display panel, and the driving circuit applies a driving voltage to the liquid crystal of the display panel. The driving circuit includes a gate driver for individually selecting one of a plurality of switching elements connected to the gate lines and the data lines, and a data driver for supplying a video signal corresponding to an image to pixel electrodes via the selected switching element.

Figure **11** shows a configuration of a part of a data driver in a prior art driving circuit. The circuit **110** shown in Figure **11** outputs a video signal to one of a plurality of data lines. Accordingly, the data driver requires circuits **110** the number of which is equal to the number of data lines provided in a display panel. For simplicity of explanation, it is herein assumed that video data consists of three bits (D_0, D_1, D_2). On such an assumption, the video data may have eight values of 0 to 7, and a signal voltage supplied to each pixel is one of eight levels V_0-V_7.

The circuit **110** includes a sampling flip-flop $\mathbf{M_{SMP}}$, a holding flip-flop $\mathbf{M_H}$, a decoder **DEC**, and analog switches $\mathbf{ASW_0}$-$\mathbf{ASW_7}$. To each of the analog switches $\mathbf{ASW_0}$-$\mathbf{ASW_7}$, a corresponding one of external source voltages V_0-V_7 of respective eight levels which are different from each other is supplied. In addition, to the analog switches $\mathbf{ASW_0}$-$\mathbf{ASW_7}$, control signals S_0-S_7 are supplied from the decoder **DEC**, respectively. Each of the control signals S_0-S_7 is used for switching the ON/OFF state of the analog switch.

Next, the operation of the circuit **110** is described. At the rising of a sampling pulse T_{SMPn} corresponding to the nth pixel, the sampling flip-flop $\mathbf{M_{SMP}}$ gets video data (D_0, D_1, D_2), and holds the video data therein. When such video data sampling for one horizontal period is completed, an output pulse signal OE is applied to the holding flip-flop $\mathbf{M_H}$. Upon receiving the output pulse signal OE, the holding flip-flop $\mathbf{M_H}$ gets the video data (D_0, D_1, D_2) from the sampling flip-flop $\mathbf{M_{SMP}}$, and transfers the video data to the decoder **DEC**.

The decoder **DEC** decodes the video data (D_0, D_1, D_2), and produces a control signal for turning on one of the analog switches $\mathbf{ASW_0}$-$\mathbf{ASW_7}$ in accordance with the respective values (0-7) of the video data (D_0, D_1, D_2). As a result, one of the external source voltages V_0-V_7 is output to a data line $\mathbf{O_n}$. For example, in the case where the value of the video data held in the holding flip-flop $\mathbf{M_H}$ is 3, the decoder **DEC** outputs a control signal S_3 which turns on the analog switch $\mathbf{ASW_3}$. As a result, the analog switch $\mathbf{ASW_3}$ becomes into the ON-state, and V_3 of the external source voltages V_0-V_7 is output to the data line $\mathbf{O_n}$.

Such a prior art data driver involves a problem in that, as the number of bits in video data increases, the circuit configuration becomes complicated and the size of the circuit is increased. This is because the prior art data driver requires gray-scale voltages the number of which is equal to the gray scales to be displayed. For example, in the case where the video data consists of 4 bits for displaying 16 gray-scale images, the number of required gray-scale voltages is: $2^4 = 16$. Similarly, in the case where the video data consists of 6 bits for displaying 64 gray-scale images, the number of required gray-scale voltages is: $2^6 = 64$. In the case of 8-bit video data for displaying 256 gray-scale images, the number of required gray-scale voltages is: $2^8 = 256$. As described above, the prior art data driver requires a large number of gray-scale voltages as the number of bits of video data increases. This causes the circuit configuration to be complicated and the circuit size to be increased. Moreover, interconnections between voltage source circuits and analog switches are also complicated.

For the above-mentioned reasons, the actual application of such a prior art data driver is limited to 3-bit video data or 4-bit video data.

In order to solve such prior art problems, there have been proposed methods and circuits for driving a display apparatus in Japanese Laid-Open Patent Publication Nos. 4-136983, 4-140787, and 6-27900. Please note that Japanese Laid-Open Patent Publication No. 6-27900 is not a prior art reference of this application, because Japanese Laid-Open Patent Publication No. 6-27900 was laid-open on February 4, 1994.

Figure **12** shows a configuration for a part of a driving circuit disclosed in Japanese Laid-Open Patent Pub-

lication No. 6-27900. The circuit **120** shown in Figure **12** outputs a video signal to one of a plurality of data lines. Accordingly, the data driver requires circuits **120** the number of which is equal to the number of data lines provided in a display panel. It is herein assumed that video data consists of 6 bits (D_0, D_1, D_2, D_3, D_4, D_5). On such an assumption, the video data may have 64 values of 0-63, and a signal voltage applied to each pixel is one of nine gray-scale voltages V_0, V_8, V_{16}, V_{24}, V_{32}, V_{40}, V_{48}, V_{56}, and V_{64}, and a plurality of interpolated voltages which are produced from the gray-scale voltages V_0, V_8, V_{16}, V_{24}, V_{32}, V_{40}, V_{48}, V_{56}, and V_{64}.

The circuit **120** includes a sampling flip-flop $\mathbf{M_{SMP}}$, a holding flip-flop $\mathbf{M_H}$, a selection control circuit **SCOL**, and analog switches $\mathbf{ASW_0}$-$\mathbf{ASW_8}$. To each of the analog switches $\mathbf{ASW_0}$-$\mathbf{ASW_8}$, a corresponding one of gray-scale voltages V_0, V_8, V_{16}, V_{24}, V_{32}, V_{40}, V_{48}, V_{56}, and V_{64} of respective levels which are different from each other. To the analog switches $\mathbf{ASW_0}$-$\mathbf{ASW_8}$, control signals S_0, S_8, S_{16}, S_{24}, S_{32}, S_{40}, S_{48}, S_{56}, and S_{64} are supplied from the selection control circuit **SCOL**, respectively. Each of the control signals are used to switch the ON/OFF state of the analog signal.

To the selection control circuit **SCOL**, clock signals t_1, t_2, t_3, and t_4 are supplied. As is shown in Figure **13**, the clock signals t_1, t_2, t_3, and t_4 have duty ratios which are different from each other. The selection control circuit **SCOL** receives 6-bit video data d_5, d_4, d_3, d_2, d_1, and d_0, and outputs one of control signals S_0, S_8, S_{16}, S_{24}, S_{32}, S_{40}, S_{48}, S_{56}, and S_{64} in accordance with the value of the received video data. The relationship between the input and the output of the selection control circuit **SCOL** is determined by using a logical table.

Table 1 shows a logical table for the selection control circuit **SCOL**. The 1st to 6th columns of Table 1 indicate values of bits d_5, d_4, d_3, d_2, d_1, and d_0 of the video data, respectively. The 7th to 15th columns of Table 1 indicate values of control signals S_0, S_8, S_{16}, S_{24}, S_{32}, S_{40}, S_{48}, S_{56}, and S_{64}, respectively. Each blank in the 7th to 15th columns in Table 1 means that the value of the control signal is 0. In addition, "t_i" indicates that the value of the control signal is 1 when the value of the clock signal t_i is 1, and the value of the control signal is 0 when the value of the clock signal t_i is 0. Also, "$\bar{t}_i$" indicates that the value of the control signal is 0 when the value of the clock signal t_i is 1, and the value of the control signal is 1 when the value of the clock signal t_i is 0. Herein, i = 1, 2, 3, and 4.

Table 1

d_5	d_4	d_3	d_2	d_1	d_0	S_0	S_8	S_{16}	S_{24}	S_{32}	S_{40}	S_{48}	S_{56}	S_{60}
0	0	0	0	0	0	1	0							
0	0	0	0	0	1	t_1	$\overline{t_1}$							
0	0	0	0	1	0	t_2	$\overline{t_2}$							
0	0	0	0	1	1	t_3	$\overline{t_3}$							
0	0	0	1	0	0	t_4	$\overline{t_4}$							
0	0	0	1	0	1	$\overline{t_3}$	t_3							
0	0	0	1	1	0	$\overline{t_2}$	t_2							
0	0	0	1	1	1	$\overline{t_1}$	t_1							
0	0	1	0	0	0	0	1	0	0	0	0	0	0	0
0	1	1	1	1	0				$\overline{t_3}$	t_3				
0	1	1	1	1	1				$\overline{t_2}$	t_2				
									$\overline{t_1}$	t_1				
1	0	0	0	0	0					1	0			
1	0	0	0	0	1					t_1	$\overline{t_1}$			
1	0	0	0	1	0					t_2	$\overline{t_2}$			
1	0	0	0	1	1					t_3	$\overline{t_3}$			
1	0	0	1	0	0					t_4	$\overline{t_4}$			
1	0	0	1	0	1					$\overline{t_3}$	t_3			
1	0	0	1	1	0					$\overline{t_2}$	t_2			
1	0	0	1	1	1					$\overline{t_1}$	t_1			
1	0	1	0	0	0	0	0	0	0		1	0	0	0
1	1	0										$\overline{t_3}$	t_3	
1	1	0	0	0	0							$\overline{t_2}$	t_2	0
												$\overline{t_1}$	t_1	0
1	1	1	0	0	0								1	0
1	1	1	0	0	1								t_1	$\overline{t_1}$
1	1	1	0	1	0								t_2	$\overline{t_2}$
1	1	1	0	1	1								t_3	$\overline{t_3}$
1	1	1	1	0	0								t_4	$\overline{t_4}$
1	1	1	1	0	1								$\overline{t_3}$	t_3
1	1	1	1	1	0								$\overline{t_2}$	t_2
1	1	1	1	1	1								$\overline{t_1}$	t_1

As is seen from Table 1, when the value of the video data is a multiple of 8, one of the gray-scale voltages V_0, ..., V_{64} is output to the data line $\mathbf{O_n}$. When the value of the video data is not a multiple of 8, an oscillating voltage which oscillates between a pair of gray-scale voltages V_0, ..., V_{64} at a duty ratio of one of the clock signals t_1, t_2, t_3, and t_4 is output to the data line $\mathbf{O_n}$. The data driver **120** produces seven different oscillating voltages between respective adjacent gray-scale voltages, in accordance with the logical table of Table 1. Thus, it is possible to attain 64 gray-scale images by using only 9 levels of gray-scale voltages.

The following equations are logical equations which define the relationships among the video data d_5, d_4, d_3, d_2, d_1, and d_0, the clock signals t_1, t_2, t_3, and t_4, and the control signals S_0, S_8, S_{16}, S_{24}, S_{32}, S_{40}, S_{48}, S_{56}, and S_{64} shown in Table 1.

$$S_0 = \{0\} + \{1\}t_1 + \{2\}t_2 + \{3\}t_3 + \{4\}t_4 + \{5\}"t_3" + (6)"t_2" + \{7\}"t_1" \quad (1)$$

$$S_8 = \{1\}"t_1 + \{2\}"t_2" + \{3\}"t_3" + \{4\}"t_4" + \{5\}t_3 + \{6\}t_2 + \{7\}t_1 + \{8\} + \{9\}t_1 + \{10\}t_2 + \{11\}t_3 + \{12\}t_4 + \{13\}"t_3" + \{14\}"t_2" + \{15\}"t_1" \quad (2)$$

$$S_{16} = \{9\}"t_1 + \{10\}"t_2" + \{11\}"t_3" + \{12\}"t_4" + \{13\}t_3 + \{14\}t_2 + \{15\}t_1 + \{16\} + \{17\}t_1 + \{18\}t_2 + \{19\}t_3 + \{20\}t_4 + \{21\}"t_3" + \{22\}"t_2" + \{23\}"t_1" \quad (3)$$

Similarly, the control signals S_{24}, S_{32}, S_{40}, and S_{48} are defined. The control signals S_{56} and S_{64} are defined as follows.

$$S_{56} = \{49\}"t_1" + \{50\}"t_2" + \{51\}"t_3" + \{52\}"t_4" + \{53\}t_3 + \{54\}t_2 + \{55\}t_5 + \{56\} + \{57\}t_1 + \{58\}t_2 + \{59\}t_3 + \{60\}t_4 + \{61\}"t_3" + \{62\}"t_2" + \{63\}"t_1" \quad (4)$$

$$S_{64} = \{57\}"t_1" + \{58\}"t_2" + \{59\}"t_3" + \{60\}"t_4" + \{61\}t_3 + \{62\}t_2 + \{63\}t_1 \quad (5)$$

In the above equations, {i} indicates a value when the binary data (d_5, d_4, d_3, d_2, d_1, d_0) is represented in the decimal notation. For example, {1} = (d_5, d_4, d_3, d_2, d_1, d_0) = (0, 0, 0, 0, 0, 1). In addition, "t_i" indicates a signal which is inverted from the signal t_i.

On the basis of the above logical equations, logical circuits shown in Figures **14** and **15** are obtained. The selection control circuit **SCOL** is constructed by the logical circuits shown in Figures **14** and **15**.

The logical circuit shown in Figure **14** produces 64 kinds of gray-scale selection data {0} - {63} in accordance with the value of 6-bit video data (d_5, d_4, d_3, d_2, d_1, d_0). The logical circuit shown in Figure **15** produces control signals S_0, S_8, S_{16}, S_{24}, S_{32}, S_{40}, S_{48}, S_{56}, and S_{64}, based on the gray-scale selection data {0} - {63} and the clock signals t_1, t_2, t_3, and t_4. For example, a case where the video data (d_5, d_4, d_3, d_2, d_1, d_0) = (0, 0, 0, 0, 0, 1) is input to the selection control circuit **SCOL** is explained. In such a case, the logical circuit shown in Figure **14** outputs the gray-scale selection data {1}. The logical circuit shown in Figure **15** receives the gray-scale selection data {1} and alternately outputs the control signal S_0 and the control signal S_8 at a duty ratio of the clock signal t_1. As a result, the gray-scale voltage V_0 and the gray-scale voltage V_8 are alternately output via the analog switch $\mathbf{ASW_0}$ and the analog switch $\mathbf{ASW_8}$ at the duty ratio of the clock signal t_1 to the data line $\mathbf{O_n}$.

The actual data driver requires the selection control circuits **SCOL** the number of which is equal to the number of data lines. Thus, the circuit scale of the selection control circuit **SCOL** largely affects the chip size of the integrated circuit on which the data driver is installed. If the circuit scale of the selection control circuit **SCOL** becomes large, the cost for the integrated circuit is increased. Moreover, if the number of bits of video data increases in order to realize an image with a larger number of gray scales, the circuit scale of the data driver is further increased. This also increases the size and the production cost of the integrated circuit.

SUMMARY OF THE INVENTION

The driving circuit of this invention is used for driving a display apparatus including pixels and data lines for applying voltages to the pixels and which displays an image with multiple gray scales in accordance with video data consisting of a plurality of bits. The driving circuit includes: oscillating voltage specifying means for specifying one of a plurality of oscillating signals having respective duty ratios which are different from each other in accordance with video data consisting of bits selected from the plurality of bits, and for outputting the specified oscillating signal T and an oscillating signal $\overline{T}$ which is obtained by inverting the specified oscillating signal T; gray-scale voltage specifying means for producing gray-scale voltage specifying signals which specify a first gray-scale voltage and a second gray-scale voltage among a plurality of gray-scale voltages supplied from gray-scale voltage supply means, in accordance with video data consisting of bits other than the selected bits of the plurality of bits; and output means for outputting the first gray-scale voltage and the second gray-scale voltage specified by the gray-scale voltage specifying signals to the data lines, in accordance with the oscillating signal T and the oscillating signal $\overline{T}$.

In one embodiment of the invention, the first gray-scale voltage and the second gray-scale voltage are adjacent ones of the plurality of gray-scale voltages.

In another embodiment of the invention, the plurality of oscillating signals include oscillating signals having

duty ratios of 8:0, 7:1, 6:2, 5:3, 4:4, 3:5, 2:6, and 1:7, respectively.

According to another aspect of the invention, a driving circuit for driving a display apparatus including pixels and data lines for applying voltages to the pixels and which displays an image with multiple gray scales in accordance with video data consisting of a plurality of bits is provided. The driving circuit includes: control signal generating means for generating a plurality of control signals in accordance with video data consisting of a plurality of bits; and a plurality of switching means, each of the plurality of switching means being supplied with a corresponding one of the plurality of control signals and a corresponding one of a plurality of gray-scale voltages generated by gray-scale voltage generating means, the gray-scale voltage supplied to the switching means being output to the data lines via the switching means in accordance with the control signal, wherein the control signal generating means includes: oscillating voltage specifying means for specifying one of a plurality of oscillating signals having respective duty ratios which are different from each other in accordance with video data consisting of bits selected from the plurality of bits, and for outputting the specified oscillating signal T and an oscillating signal $\overline{T}$ which is obtained by inverting the specified oscillating signal T; gray-scale voltage specifying means for producing gray-scale voltage specifying signals which specify a first gray-scale voltage and a second gray-scale voltage among the plurality of gray-scale voltages, in accordance with video data consisting of bits other than the selected bits of the plurality of bits; and output means for outputting a first control signal which oscillates at substantially the same duty ratio as that of the oscillating signal T to one of the switching means which is supplied with the first gray-scale voltage specified by the gray-scale voltage specifying signals and for outputting a second control signal which oscillates at substantially the same duty ratio as that of the oscillating signal $\overline{T}$ to one of the switching means which is supplied with the second gray-scale voltage specified by the gray-scale voltage specifying signals.

In one embodiment of the invention, the first gray-scale voltage and the second gray-scale voltage are adjacent ones of the plurality of gray-scale voltages.

In another embodiment of the invention, the plurality of oscillating signals include oscillating signals having duty ratios of 8:0, 7:1, 6:2, 5:3, 4:4, 3:5, 2:6, and 1:7, respectively.

In another embodiment of the invention, the switching means is an analog switch.

According to the driving circuit of the invention, a pair of gray-scale voltages are selected (specified) among a plurality of gray-scale voltages, and one of a plurality of oscillating signals is specified. The driving circuit outputs a voltage signal which oscillates between the specified pair of gray-scale voltages at the oscillating frequency of the specified oscillating signal. Therefore, a plurality of interpolated gray scales can be realized between a plurality of applied gray-scale voltages.

According to the driving circuit of the invention, by using the gray-scale voltage specifying means and the oscillating signal specifying means, it is possible to always realize an image display with multiple gray scales in both cases where the driving circuit directly outputs one of the plurality of gray-scale voltages and where the driving circuit alternately outputs the specified pair of gray-scale voltages.

Accordingly, it is unnecessary to provide an additional driving circuit depending on the cases where the driving circuit directly outputs one of the plurality of gray-scale voltages and where the driving circuit alternately outputs the specified pair of gray-scale voltages. As a result, it is possible to simplify the configuration of the driving circuit, and the size of the driving circuit can be minimized.

Thus, the invention described herein makes possible the advantage of providing a driving circuit for a display apparatus, which has a simplified and small construction, and which can display an image with multiple gray scales in accordance with multi-bit video data.

This and other advantages of the present invention will become apparent to those skilled in the art upon reading and understanding the following detailed description with reference to the accompanying figures.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure **1** is a diagram showing a construction of a liquid crystal display apparatus.

Figure **2** is a timing chart illustrating the relationship among input data, sampling pulses, and an output pulse in one horizontal period.

Figure **3** is a timing chart illustrating the relationship among input data, an output pulse, an output voltage, and a gate pulse in one vertical period.

Figure **4** is a timing chart illustrating the relationship among input data, an output pulse, an output voltage, a gate pulse, and a voltage applied to a pixel in one vertical period.

Figure **5** shows waveforms of an output voltage oscillating in one output period.

Figure **6** is a diagram showing a part of a configuration for a data driver in a driving circuit in an example according to the invention.

Figure **7** is a diagram showing a part of a configuration of a selection control circuit **SCOL** in the driving

circuit in the example according to the invention.

Figure **8** is a diagram showing another part of the configuration of the selection control circuit **SCOL** in the driving circuit in the example according to the invention.

Figure **9** is a diagram showing another part of the configuration of the selection control circuit **SCOL** in the driving circuit in the example according to the invention.

Figure **10** is a diagram showing another part of the configuration of the selection control circuit **SCOL** in the driving circuit in the example according to the invention.

Figure **11** is a diagram showing a part of a configuration for a data driver in a conventional driving circuit.

Figure **12** is a diagram showing a part of a configuration of a data driver in a driving circuit of a related art.

Figure **13** shows waveforms of signals t_1-t_4 supplied to a selection control circuit **SCOL**.

Figure **14** is a diagram showing a part of a configuration of a selection control circuit **SCOL** in the conventional driving circuit.

Figure **15** is a diagram showing another part of the configuration of a selection control circuit **SCOL** in the conventional driving circuit.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Hereinafter, the present invention will be described by way of illustrative examples in accordance with the accompanying drawings. In the following description, a matrix type liquid crystal display apparatus is used as an example of a display apparatus. It is appreciated that the present invention is applicable to other types of display apparatus.

Figure **1** shows a construction of a matrix type liquid crystal display apparatus. The liquid crystal display apparatus shown in Figure **1** includes a display section **100** for displaying a video image, and a driving circuit **101** for driving the display section **100**. The driving circuit **101** includes a data driver **102** which provides video signals to the display section **100** and a scanning driver **103** which provides scanning signals to the display section **100**. The data driver may be called "a source driver" or "a column driver". The scanning driver may be called "a gate driver" or "a row driver".

The display section **100** includes an M x N array of pixels **104** (M pixels in each column and N pixels in each row; where M and N are positive integers), and also includes switching elements **105** respectively connected to the pixels **104**.

In Figure **1**, N data lines **106** are used for connecting respective output terminals **S(i)** (i = 1, 2, ...,N) of the data driver **102** to the corresponding switching elements **105**. Similarly, M scanning lines **107** are used for connecting respective output terminals **G(j)** (j = 1, 2, ...,M) of the scanning driver **103** to the corresponding switching elements **105**. As the switching elements **105**, thin film transistors (TFTs) can be used. Alternatively, other types of switching elements may also be used. The data line may be called "a source line" or "a column line". The scanning line may be called "a gate line" or "a row line".

The scanning driver **103** sequentially outputs a voltage which is kept at a high level during a specific time period from its output terminals **G(j)** to the corresponding scanning lines **107**. The specific time period is referred to as one horizontal period jH (where j is an integer of 1 to M). The total length of time obtained by adding up all the horizontal periods jH (i.e., 1H + 2H + 3H + ... + MH), a blanking period and a vertical synchronizing period is referred to as one vertical period.

When the level of the voltage which is output from the output terminal **G(j)** of the scanning driver **103** to the scanning line **107** is high, the switching element **105** connected to the output terminal **G(j)** is in the ON-state. When the switching element **105** is in the ON-state, the pixel **104** connected to the switching element **105** is charged in accordance with the voltage which is output from the output terminal **S(j)** of the data driver **102** to the corresponding data line **106**. The voltage of the thus charged pixel **104** remains unchanged for about one vertical period until it is charged again by the subsequent voltage to be supplied from the data driver **102**.

Figure **2** shows the relationship among digital video data DA, sampling pulses T_{smpi}, and an output pulse signal OE, during the jth horizontal period jH determined by a horizontal synchronizing signal H_{syn}. As can be seen from Figure **2**, while sampling pulses T_{smp1}, T_{smp2}, ..., T_{smpi}, ..., and T_{smpN} are sequentially applied to the data driver **102**, digital video data DA_1, DA_2 ..., DA_i ..., and DA_N are fed into the data driver **102** accordingly. The jth output pulse OE_j determined by the output pulse signal OE is then applied to the data driver **102**. On receiving the jth output pulse OE_j, the data driver **102** outputs voltages from its output terminals **S(i)** to the corresponding data lines **106**.

Figure **3** shows the relationship among the horizontal synchronizing signal H_{syn}, the digital video data DA, the output pulse signal OE, and the timing of outputs of the data driver **102** and scanning driver **103**, during one vertical period determined by a vertical synchronizing signal V_{syn}. In Figure **3**, a SOURCE(j) indicates a level range of voltages output from the data driver **102**, with such timing as shown in Figure **2** and in accordance

with the digital video data applied during the horizontal period jH. The SOURCE(j) is shown as a hatched rectangular area to indicate a level range of voltages output from all the N output terminals **S(1)** to **S(N)** of the data driver **102**. While the voltages indicated by the SOURCE(j) are applied to the data lines **106**, the voltage which is output from the jth output terminal **G(j)** of the scanning driver **103** to the jth scanning line **107** is changed to and kept at a high level, thereby turning on all the N switching elements **105** connected to the jth scanning line **107**. As a result, the N pixels **104** respectively connected to these N switching elements **105** are charged in accordance with the voltage applied to the corresponding data lines **106** from the data driver **102**.

The above-described process is repeated M times, i.e., for the 1st to Mth scanning lines **107**, so that an image corresponding to one vertical period is displayed. In the case of non-interlace type display apparatus, the produced image serves as a complete display image on the display screen thereof.

In this specification, the time interval between the jth output pulse OE_j and the (j+1)th output pulse OE_{j+1} in the output pulse signal OE is defined as "one output period". This means that one output period is equal to a period represented by SOURCE(j) shown in Figure **3**. In cases where usual line sequential scanning is performed, it is preferable that one output period is made equal to one horizontal period. The reason for this is as follows. While the data driver **102** outputs voltages corresponding to digital video data for one horizontal (scanning) line, to the data lines **106**, it also performs sampling of digital video data for the next horizontal line. The maximum allowable length of time during which these voltages can be output from the data driver **102** is equal to one horizontal period. Furthermore, except for special cases, as the output period becomes longer, the pixels can be charged more accurately. In the driving circuit described herein, therefore, one output period is equal to one horizontal period. According to the present invention, however, one output period is not necessarily required to be equal to one horizontal period.

Figure **4** shows, in addition to the timings of the respective signals shown in Figures **2** and **3**, the levels of voltages which are applied to the pixels P(j, i) (j = 1, 2, ..., M) in accordance with the timings.

Figure **5** shows an exemplary waveform for a voltage signal output from the data driver **102** to the data lines **106** in one output period. In the case of the conventional data driver, the voltage level of the voltage signal output to the data lines **106** is constant during one output period. On the other hand, from the data driver **102** in this example according to the invention, the voltage signal output to the data lines **106** includes an oscillating component which oscillates during one output period. As is shown in Figure **5**, the voltage signal is a pulse-like signal, and a ratio of a high-level period to a low-level period, i.e., a duty ratio n:m is selected as described below.

Figure **6** shows a configuration of a part of the data driver **102** in the driving circuit **101**. The circuit **60** shown in Figure **6** outputs a video signal from an nth output terminal **S(n)** to one data line **106**. The data driver **102** includes circuits **60** the number of which is equal to the number of the data lines **106** provided in the display section **100**. Herein, it is assumed that the video data consists of 6 bits (D_0, D_1, D_2, D_3, D_4, D_5). On such an assumption, the video data may have 64 kinds of values of 0 - 63, and a signal voltage applied to each pixel is one of nine gray-scale voltages V_0, V_8, V_{16}, V_{24}, V_{32}, V_{40}, V_{48}, V_{56}, and V_{64}, and interpolated voltages which are produced from any pair of the gray-scale voltages chosen from V_0, V_8, V_{16}, V_{24}, V_{32}, V_{40}, V_{48}, V_{56}, and V_{64}

The circuit **60** includes a sampling flip-flop $\mathbf{M_{SMP}}$ which performs the sampling operation, a holding flip-flop $\mathbf{M_H}$ which performs the holding operation, a selection control circuit **SCOL**, and analog switches $\mathbf{ASW_0}$-$\mathbf{ASW_8}$. To each of the analog switches $\mathbf{ASW_0}$-$\mathbf{ASW_8}$, a corresponding one of nine gray-scale voltages V_0, V_8, V_{16}, V_{24}, V_{32}, V_{40}, V_{48}, V_{56}, and V_{64} is supplied. The gray-scale voltages V_0-V_{64} have respective levels which are different from each other. The selection control circuit **SCOL** is provided with seven oscillating signals t_1-t_7. The oscillating signals t_1-t_7 have respective duty ratios which are different from each other.

As the sampling flip-flop $\mathbf{M_{SMP}}$ and the holding flip-flop $\mathbf{M_H}$, for example, D-type flip-flops can be used. It is appreciated that such sampling and holding flip-flops can be realized by using other types of circuit elements.

Next, by referring to Figure **6**, the operation of the circuit **60** is described. At the rising of a sampling pulse T_{SMPn} corresponding to the nth pixel, the sampling flip-flop $\mathbf{M_{SMP}}$ gets video data (D_0, D_1, D_2, D_3, D_4, D_5), and holds the video data therein. When such video data sampling for one horizontal period is completed, an output pulse signal OE is applied to the holding flip-flop $\mathbf{M_H}$. When the output pulse signal OE is applied, the video data held in the sampling flip-flop $\mathbf{M_{SMP}}$ is fed into the holding flip-flop $\mathbf{M_H}$ and output to the selection control circuit **SCOL**. The selection control circuit **SCOL** receives the video data, and produces a plurality of control signals in accordance with the value of the video data. The control signals are used for switching the ON/OFF states of the respective analog switches $\mathbf{ASW_0}$-$\mathbf{ASW_8}$. The video data input to the selection control circuit **SCOL** is represented by d_0, d_1, d_2, d_3, d_4, and d_5, and the control signals output from the selection control circuit **SCOL** are represented by S_0, S_8, S_{16}, S_{24}, S_{32}, S_{40}, S_{48}, S_{56}, and S_{64}.

Table 2 is a logical table for the lower three bits d_2, d_1, and d_0 of the 6-bit video data. The 1st to 3rd columns of Table 2 indicate the values of video data bits d_2, d_1, and d_0, respectively. The 4th to 11th columns of Table 2 indicate which oscillating signal is specified from the oscillating signals t_0-t_7. In the 4th to 11th columns of

Table 2, the oscillating signal which is indicated by a value of 1 is specified. For example, in the case of (d_2, d_1, d_0) = (0, 0, 0), the oscillating signal t_0 is specified. In this example, the oscillating signals t_0-t_7 are clock signals having duty ratios of 8:0, 7:1, 6:2, 5:3, 4:4, 3:5, 2:6, and 1:7, respectively. Herein, if an oscillating signal has a duty ratio of k:0 or 0:k (k is a natural number), the oscillating signal is defined as always being at a fixed level. The oscillating signals t_5, t_6, and t_7 are the signals obtained by inverting the oscillating signals t_3, t_2, and t_1.

Table 2

d_2	d_1	d_0	t_0	t_1	t_2	t_3	t_4	t_5	t_0	t_7
0	0	0	1							
0	0	1		1						
0	1	0			1					
0	1	1				1				
1	0	0					1			
1	0	1						1		
1	1	0							1	
1	1	1								1

From the logical table of Table 2, the following logical equation is obtained.

$$T = (0)t_0 + (1)t_1 + (2)t_2 + (3)t_3 + (4)t_4 + (5)t_5 + (6)t_6 + (7)t_7 \quad (6)$$

In the above equation, (i) indicates a value of binary data (d_2, d_1, d_0) which is represented in a decimal notation. That is, (0) = (d_2, d_1, d_0) = (0, 0, 0), (1) = (d_2, d_1, d_0) = (0, 0, 1), (2) = (d_2, d_1, d_0) = (0, 1, 0), (3) = (d_2, d_1, d_0) = (0, 1, 1), (4) = (d_2, d_1, d_0) = (1, 0, 0), (5) = (d_2, d_1, d_0) = (1, 0, 1), (6) = (d_2, d_1, d_0) = (1, 1, 0), and (7) = (d_2, d_1, d_0) = (1, 1, 1).

The oscillating signal t_0 is continually at a level of "1", so that Equation (6) can alternatively be represented as the following equation.

$$T = (0) + (1)t_1 + (2)t_2 + (3)t_3 + (4)t_4 + (5)t_5 + (6)t_6 + (7)t_7 \quad (7)$$

Table 3 is a logical table representing the relationships among the upper three bits d_5, d_4, and d_3 of the 6-bit video data, and the control signals S_0, S_8, S_{16}, S_{24}, S_{32}, S_{40}, S_{48}, S_{56}, and S_{64}. In Table 3, a variable T denotes a signal T which is defined by Equations (6) and (7). A variable $\overline{T}$ denotes an inverted signal $\overline{T}$ obtained by inverting the signal T.

Table 3

d_5	d_4	d_3	S_0	S_8	S_{16}	S_{24}	S_{32}	S_{40}	S_{48}	S_{56}	S_{64}
0	0	0	T	$\overline{T}$							
0	0	1		T	$\overline{T}$						
0	1	0			T	$\overline{T}$					
0	1	1				T	$\overline{T}$				
1	0	0					T	$\overline{T}$			
1	0	1						T	$\overline{T}$		
1	1	0							T	$\overline{T}$	
1	1	1								T	$\overline{T}$

From the logical table of Table 3, the following logical equations are obtained.

$$S_0 = [0]T \quad (8)$$

$$S_8 = [0]"T" + [8]T \quad (9)$$
$$S_{16} = [8]"T" + [16]T \quad (10)$$
$$S_{24} = [16]"T" + [24]T \quad (11)$$
$$S_{32} = [24]"T" + [32]T \quad (12)$$
$$S_{40} = [32]"T" + [40]T \quad (13)$$
$$S_{48} = [40]"T" + [48]T \quad (14)$$
$$S_{56} = [48]"T" + [56]T \quad (15)$$
$$S_{64} = [56]"T" \quad (16)$$

In the above equations, [i] indicates a value of binary data (d_5, d_4, d_3), where i = (8 × j), and j is a value of binary data (d_5, d_4, d_3) which is represented in a decimal notation. For example, [8] = (d_5, d_4, d_3) = (0, 0, 1). In addition, "T" denotes an inverted signal of the signal T.

In accordance with the respective logical equations which are described above, logical circuits **70**, **80**, **90**, and **95** shown in Figures **7** through **10** are obtained. The selection control circuit **SCOL** is constructed, for example, by the logical circuits **70**, **80**, **90**, and **95** shown in Figures **7** through **10**.

The logical circuit **70** shown in Figure **7** selectively outputs oscillating signal specifying signals (0)-(7) for specifying one of a plurality of oscillating signals t_0-t_7, in accordance with the lower 3 bits d_2, d_1, and d_0 of the video data. More specifically, the video data d_2, d_1, and d_0 and the inverted signals which are respectively obtained by inverting the video data d_2, d_1, and d_0 by inverter circuits $\mathbf{INV_0}$ and $\mathbf{INV_2}$ are input into AND circuits $\mathbf{AG_0}$-$\mathbf{AG_7}$ in such combinations that constitute 0-7 in binary notation. The oscillating signal specifying signals (0)-(7) are thus obtained as the outputs of the AND circuits $\mathbf{AG_0}$- $\mathbf{AG_7}$.

The logical circuit **80** shown in Figure **8** specifies one of the plurality of oscillating signals t_0-t_7 in accordance with the oscillating signal specifying signals, and produces the specified oscillating signal T and the inverted oscillating signal $\overline{T}$ which is obtained by inverting the specified oscillating signal T by an inverter circuit $\mathbf{INV_3}$. More specifically, the oscillating signal specifying signals (1)-(7) and the oscillating signals t_1-t_7 are input into AND circuits $\mathbf{BG_1}$-$\mathbf{BG_7}$, respectively, as is shown in Figure **8**. The oscillating signal specifying signal (0) and the outputs of the AND circuits $\mathbf{BG_1}$-$\mathbf{BG_7}$ are supplied to an OR circuit **CG**. The oscillating signal T and the inverted oscillating signal $\overline{T}$ are obtained as the output of the OR circuit **CG**.

The logical circuit **90** shown in Figure **9** selectively outputs gray-scale voltage specifying signals [0], [8], [16], [24], [32], [40], [48], and [56] for specifying a pair of gray-scale voltages from among a plurality of gray-scale voltages, in accordance with the upper three bits d_5, d_4, and d_3 of the video data. More specifically, the video data d_5, d_4, and d_3 and the inverted signals which are respectively obtained by inverting the video data d_5, d_4, and d_3 by inverter circuits $\mathbf{INV_4}$-$\mathbf{INV_6}$ are input to AND circuits $\mathbf{DG_0}$-$\mathbf{DG_7}$ in such combinations which constitute 0-7 in the binary notation. As the outputs of the AND circuits $\mathbf{DG_0}$-$\mathbf{DG_7}$, the gray-scale voltage specifying signals [0], [8], [16], [24], [32], [40], [48], and (56] are obtained.

The logical circuit **95** shown in Figure **10** selectively outputs the control signals S_0-S_{64}, in accordance with the gray-scale voltage specifying signals [0], [8], [16], [24], [32], [40], [48], and [56], the oscillating signal T, and the inverted oscillating signal $\overline{T}$. More specifically, the gray-scale voltage specifying signals [0], [8], [16], [24], [32], [40], [48], and [56], and the oscillating signal T are input into AND circuits $\mathbf{EG_0}$, $\mathbf{EG_2}$, $\mathbf{EG_4}$, $\mathbf{EG_6}$, $\mathbf{EG_8}$, $\mathbf{EG_{10}}$, $\mathbf{EG_{12}}$, and $\mathbf{EG_{14}}$, respectively. The gray-scale voltage specifying signals [0], [8], [16], [24], [32], [40], [48], and [56] and the inverted oscillating signal $\overline{T}$ are input into AND circuits $\mathbf{EG_1}$, $\mathbf{EG_3}$, $\mathbf{EG_5}$, $\mathbf{EG_7}$, $\mathbf{EG_9}$, $\mathbf{EG_{11}}$, $\mathbf{EG_{13}}$, and $\mathbf{EG_{15}}$, respectively. The outputs of the AND circuits $\mathbf{EG_1}$ and $\mathbf{EG_2}$ are coupled to the inputs of an OR circuit $\mathbf{FG_1}$, respectively. The outputs of the AND circuits $\mathbf{EG_3}$ and $\mathbf{EG_4}$ are coupled to the inputs of an OR circuit $\mathbf{FG_2}$, respectively. The outputs of the AND circuits $\mathbf{EG_5}$ and $\mathbf{EG_6}$ are coupled to an OR circuit $\mathbf{FG_3}$, respectively. The outputs of the AND circuits $\mathbf{EG_7}$ and $\mathbf{EG_8}$ are coupled to the inputs of an OR circuit $\mathbf{FG_4}$, respectively. The outputs of the AND circuits $\mathbf{EG_9}$ and $\mathbf{EG_{10}}$ are coupled to the inputs of an OR circuit $\mathbf{FG_5}$, respectively. The outputs of the AND circuits $\mathbf{EG_{11}}$ and $\mathbf{EG_{12}}$ are coupled to the inputs of an OR circuit $\mathbf{FG_6}$, respectively. The outputs of the AND circuits $\mathbf{EG_{13}}$ and $\mathbf{EG_{14}}$ are coupled to the inputs of an OR circuit $\mathbf{FG_7}$, respectively. As the outputs of the AND circuit $\mathbf{EG_0}$, the OR circuits $\mathbf{FG_1}$-$\mathbf{FG_7}$, and the AND circuit $\mathbf{EG_{15}}$, the control signals S_0, S_8, S_{16}, S_{24}, S_{32}, S_{40}, S_{48}, S_{56} and S_{64} are obtained.

The control signals S_0, S_8, S_{16}, S_{24}, S_{32}, S_{40}, S_{48}, S_{56}, and S_{64} are supplied to the corresponding analog switches $\mathbf{ASW_0}$-$\mathbf{ASW_8}$. Each of the control signals S_0, S_8, S_{16}, S_{24}, S_{32}, S_{40}, S_{48}, S_{56}, and S_{64} has either a high-level value or a low-level value. For example, if the control signal is at a high level, the corresponding analog switch is controlled to be in the ON-state. If the control signal is at a low level, the corresponding analog switch is controlled to be in the OFF-state. Alternatively, the relationship between the level of the control signal and the ON/OFF state of the analog signal can be set in a reverse manner.

As described above, in the case where video data consists of a plurality of bits, a waveform of an oscillating voltage is specified in accordance with video data consisting of at least one bit selected from the plurality of bits. Then, in accordance with video data consisting of bits other than the above selected bit(s), a pair of gray-

scale voltages are specified from a plurality of gray-scale voltages. As a result, a voltage signal of an appropriate level can be output for every value of video data. The oscillating voltage is used for realizing a plurality of interpolated gray-scale voltages between the specified pair of gray-scale voltages which are specified from among the plurality of gray-scale voltages.

In the case where the value of the video data is a multiple of 8, only one of the plurality of gray-scale voltages may be output. In such a case, the duty ratio n:m of the oscillating signal or the control signal is interpreted to be k:0 or 0:k (k is a natural number).

Alternatively, regardless of whether the value of the video data is a multiple of 8 or not, the specified pair of gray-scale voltages among the plurality of gray-scale voltages may be alternately output.

As described above, the selection control circuit **SCOL** according to the invention constructed of the logical circuits **70**, **80**, **90**, and **95** shown in Figures **7** through **10** has a simplified construction as compared with the conventional selection control circuit **SCOL** shown in Figure **12** which is constructed of the logical circuits shown in Figures **14** and **15**. According to the invention, it is possible to display an image with multiple gray scales, such as 64 gray scales, by using a driving circuit having a more simplified construction. For example, in order to realize a display image with 64 gray scales, only 9 kinds of gray-scale voltages are required.

The actual data driver requires selection control circuits **SCOL** the number of which is equal to the number of data lines. Thus, the circuit scale of the selection control circuits **SCOL** largely affects the chip size of an integrated circuit (LSI) on which a data driver is installed. According to the invention, it is possible to significantly reduce the size of the integrated circuit including the selection control circuits **SCOL**. As a result, the production cost of the integrated circuit can be reduced. In cases where the number of bits of video data is increased in order to realize an image with a larger number of gray scales, such miniaturization of the circuit scale of the data driver is of great use. Accordingly, it is possible to make further progress in the size and cost reduction of the integrated circuit.

According to the invention, it is possible to obtain one or more interpolated voltages from voltages supplied from given voltage sources, whereby the number of voltage sources can be greatly decreased as compared with a conventional driving circuit which requires a large number of voltage sources. If the voltage sources are provided from the outside of the driving circuit, the number of input terminals of the driving circuit can be reduced. If the driving circuit is constructed as an LSI, the number of input terminals of the LSI can be reduced. According to the invention, it is possible to realize a driving LSI for displaying an image with multiple gray scales which could not be realized by the prior art example because of the increase in the number of terminals. In the present invention, the following effects can be attained: (1) the production cost of a display apparatus and a driving circuit are largely reduced; (2) a driving circuit for multiple gray scales which could not be practically produced due to the chip size or the LSI installation can be readily produced; and (3) the power consumption is decreased because a large number of voltage sources are not required.

Various other modifications will be apparent to and can be readily made by those skilled in the art without departing from the scope and spirit of this invention. Accordingly, it is not intended that the scope of the claims appended hereto be limited to the description as set forth herein, but rather that the claims be broadly construed.

Claims

1. A driving circuit for driving a display apparatus which includes pixels and data lines for applying voltages to said pixels and which displays an image with multiple gray scales in accordance with video data consisting of a plurality of bits, said driving circuit comprising:

   oscillating voltage specifying means for specifying one of a plurality of oscillating signals having respective duty ratios which are different from each other in accordance with video data consisting of bits selected from said plurality of bits, and for outputting said specified oscillating signal T and an oscillating signal $\overline{T}$ which is obtained by inverting said specified oscillating signal T;

   gray-scale voltage specifying means for producing gray-scale voltage specifying signals which specify a first gray-scale voltage and a second gray-scale voltage among a plurality of gray-scale voltages supplied from gray-scale voltage supply means, in accordance with video data consisting of bits other than said selected bits of said plurality of bits; and

   output means for outputting said first gray-scale voltage and said second gray-scale voltage specified by said gray-scale voltage specifying signals to said data lines, in accordance with said oscillating signal T and said oscillating signal $\overline{T}$.

2. A driving circuit according to claim 1, wherein said first gray-scale voltage and said second gray-scale

voltage are adjacent ones of said plurality of gray-scale voltages.

3. A driving circuit according to claim 1, wherein said plurality of oscillating signals include oscillating signals having duty ratios of 8:0, 7:1, 6:2, 5:3, 4:4, 3:5, 2:6, and 1:7, respectively.

4. A driving circuit for driving a display apparatus which includes pixels and data lines for applying voltages to said pixels and which displays an image with multiple gray scales in accordance with video data consisting of a plurality of bits, said driving circuit comprising:

control signal generating means for generating a plurality of control signals in accordance with video data consisting of a plurality of bits; and

a plurality of switching means, each of said plurality of switching means being supplied with a corresponding one of said plurality of control signals and a corresponding one of a plurality of gray-scale voltages generated by gray-scale voltage generating means, said gray-scale voltage supplied to said switching means being output to said data lines via said switching means in accordance with said control signal,

wherein said control signal generating means includes:

oscillating voltage specifying means for specifying one of a plurality of oscillating signals having respective duty ratios which are different from each other in accordance with video data consisting of bits selected from said plurality of bits, and for outputting said specified oscillating signal T and an oscillating signal $\overline{T}$ which is obtained by inverting said specified oscillating signal T;

gray-scale voltage specifying means for producing gray-scale voltage specifying signals which specify a first gray-scale voltage and a second gray-scale voltage among said plurality of gray-scale voltages, in accordance with video data consisting of bits other than said selected bits of said plurality of bits; and

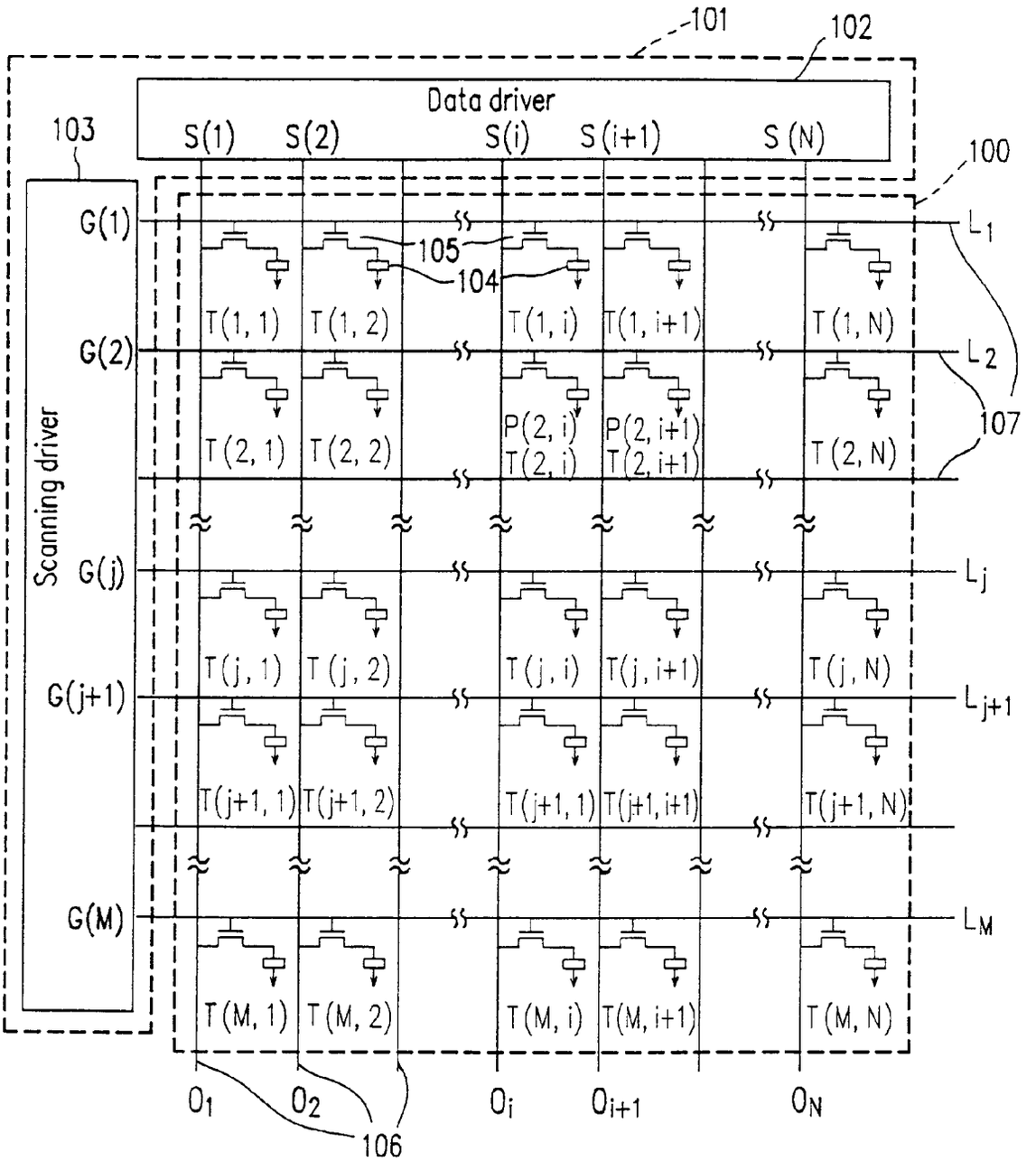
output means for outputting a first control signal which oscillates at substantially the same duty ratio as that of said oscillating signal T to one of said switching means which is supplied with said first gray-scale voltage specified by said gray-scale voltage specifying signals and for outputting a second control signal which oscillates at substantially the same duty ratio as that of said oscillating signal $\overline{T}$ to one of said switching means which is supplied with said second gray-scale voltage specified by said gray-scale voltage specifying signals.

5. A driving circuit according to claim 4, wherein said first gray-scale voltage and said second gray-scale voltage are adjacent ones of said plurality of gray-scale voltages.

6. A driving circuit according to claim 4, wherein said plurality of oscillating signals include oscillating signals having duty ratios of 8:0, 7:1, 6:2, 5:3, 4:4, 3:5, 2:6, and 1:7, respectively.

7. A driving circuit according to claim 4, wherein said switching means is an analog switch.

Fig.1


101
102
Data driver
S(1)
S(2)
S(i)
S(i+1)
S(N)
103
100
Scanning driver
G(1)
G(2)
G(j)
G(j+1)
G(M)
105
104
T(1, 1)
T(1, 2)
T(1, i)
T(1, i+1)
T(1, N)
T(2, 1)
T(2, 2)
P(2, i)
T(2, i)
P(2, i+1)
T(2, i+1)
T(2, N)
T(j, 1)
T(j, 2)
T(j, i)
T(j, i+1)
T(j, N)
T(j+1, 1)
T(j+1, 2)
T(j+1, 1)
T(j+1, i+1)
T(j+1, N)
T(M, 1)
T(M, 2)
T(M, i)
T(M, i+1)
T(M, N)
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L2
Lj
Lj+1
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107
O1
O2
Oi
Oi+1
ON
106

Fig.2

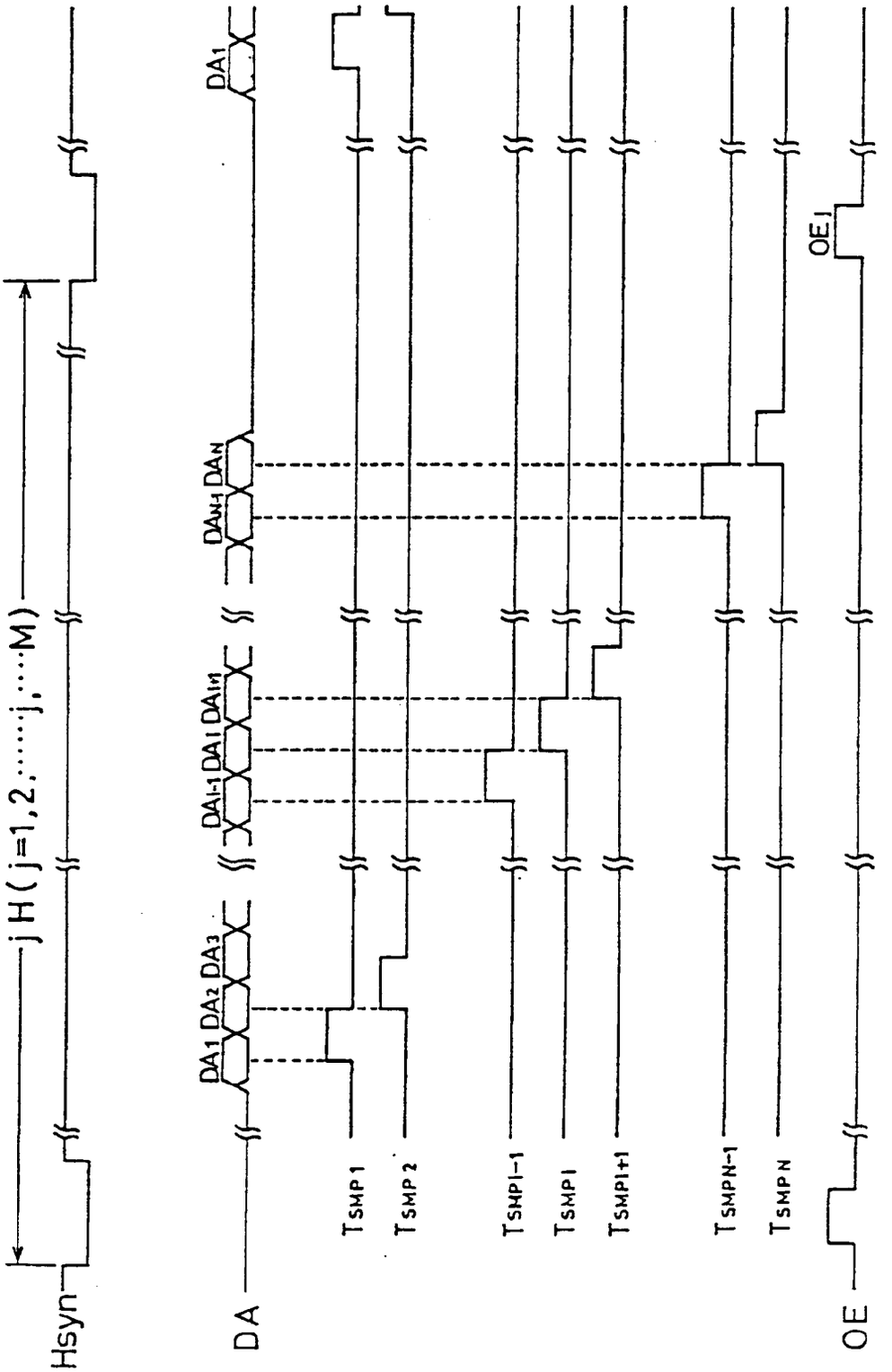

Hsyn
j H (j=1,2,·····j,····M)
DA
DA1 DA2 DA3
DA1-1 DA1 DA1+1
DAN-1 DAN
DA1
TSMP1
TSMP2
TSMPI-1
TSMPI
TSMPI+1
TSMPN-1
TSMPN
OE
OE1

Fig.3

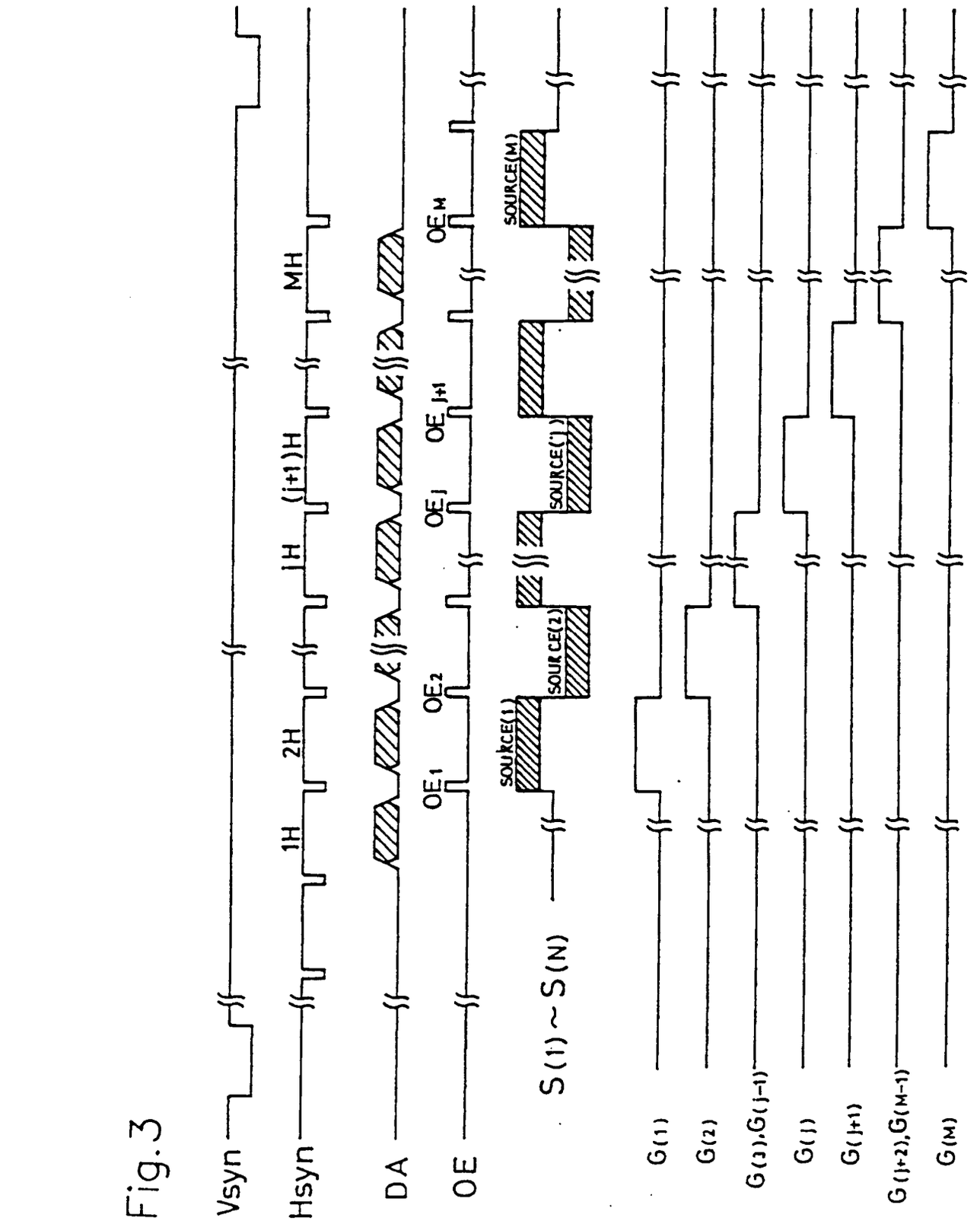

Vsyn
Hsyn
1H
2H
1H
(j+1)H
MH
DA
OE
OE1
OE2
OEj
OEj+1
OEM
S(1)~S(N)
SOURCE(1)
SOURCE(2)
SOURCE(j)
SOURCE(j+1)
SOURCE(M)
G(1)
G(2)
G(j),G(j-1)
G(j)
G(j+1)
G(j+2),G(M-1)
G(M)

Fig. 4

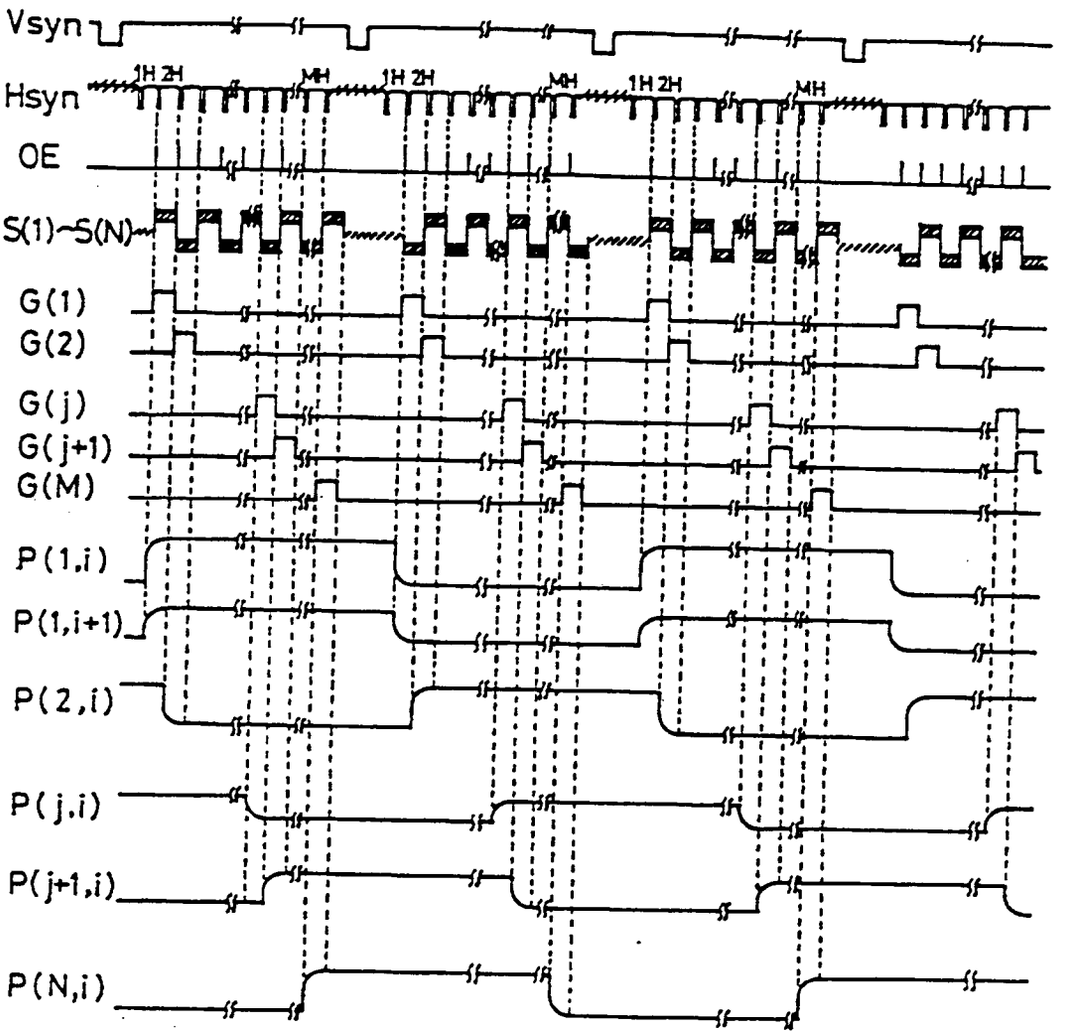

Vsyn
Hsyn
1H 2H
MH
OE
S(1)~S(N)
G(1)
G(2)
G(j)
G(j+1)
G(M)
P(1,i)
P(1,i+1)
P(2,i)
P(j,i)
P(j+1,i)
P(N,i)

Fig.5

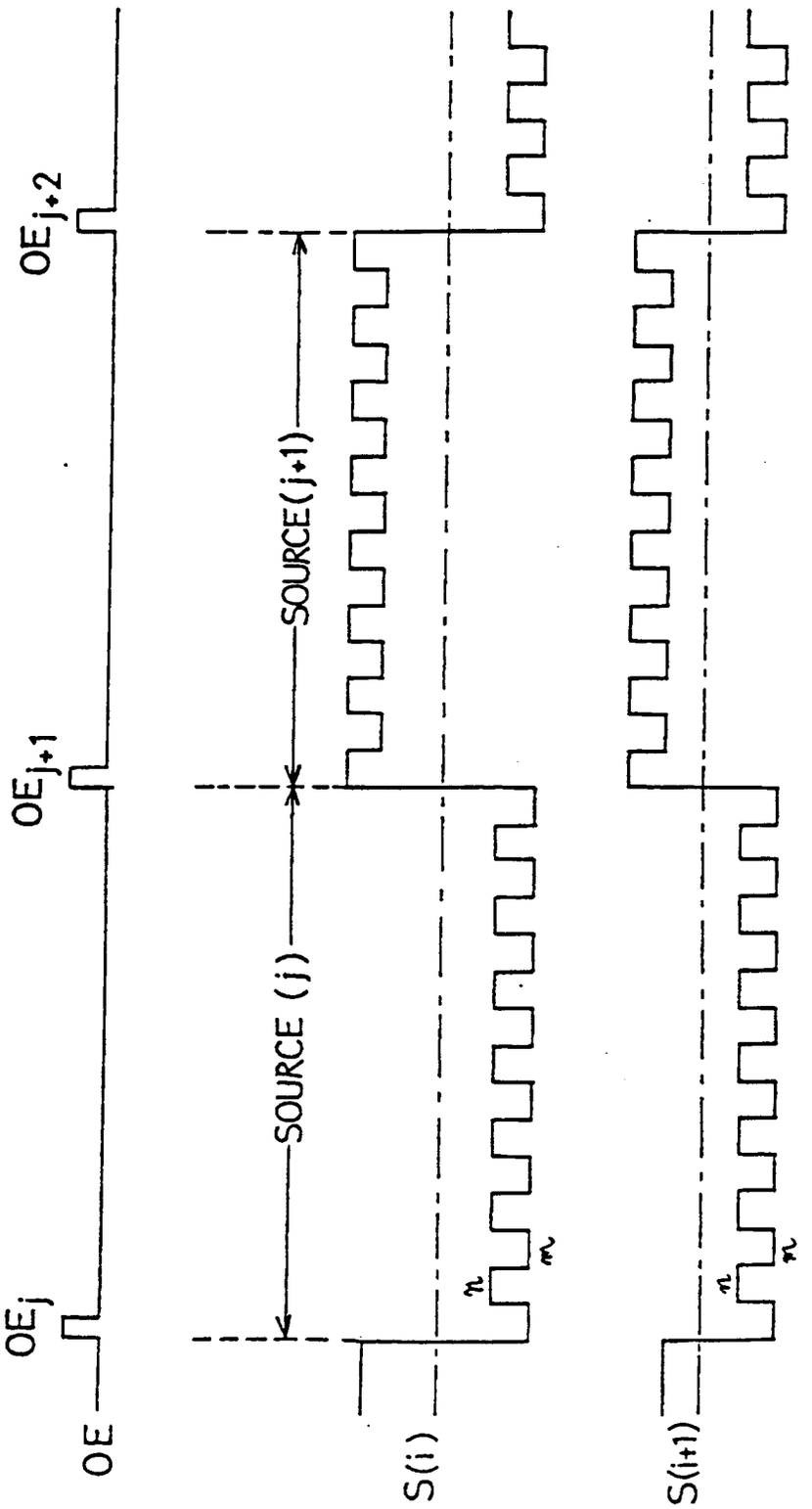


Fig.6

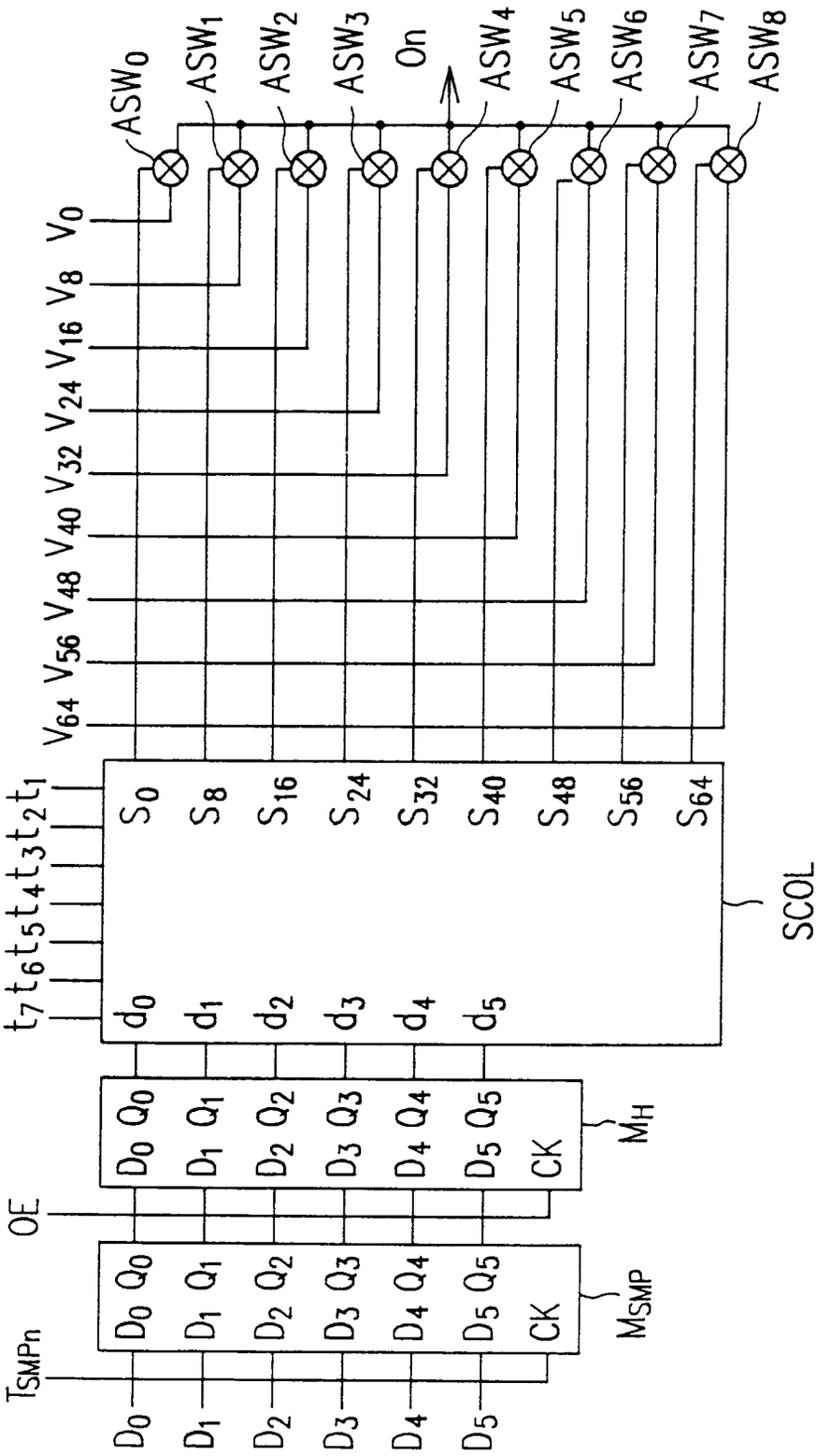

TSMPn
OE
MSMP
MH
SCOL
60
D0 D1 D2 D3 D4 D5
Q0 Q1 Q2 Q3 Q4 Q5
CK
t7 t6 t5 t4 t3 t2 t1
d0 d1 d2 d3 d4 d5
S0 S8 S16 S24 S32 S40 S48 S56 S64
V64 V56 V48 V40 V32 V24 V16 V8 V0
ASW0 ASW1 ASW2 ASW3 On ASW4 ASW5 ASW6 ASW7 ASW8

Fig.7

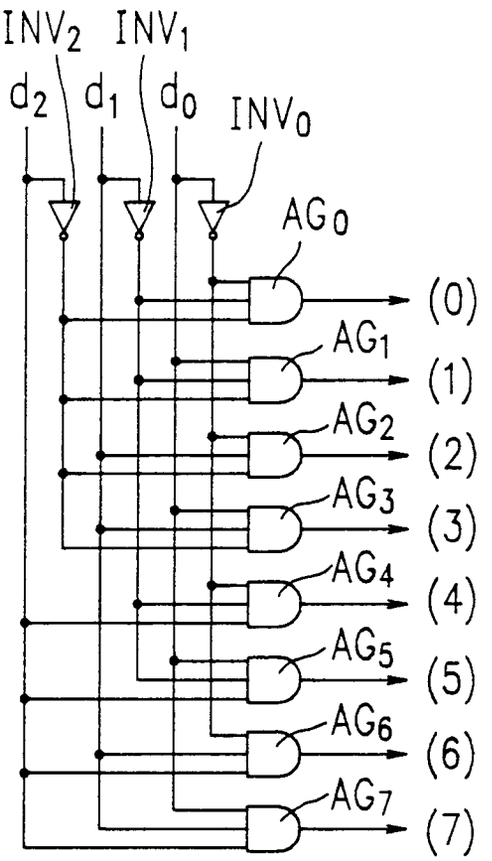

INV2
INV1
d2
d1
d0
INV0
AG0
AG1
AG2
AG3
AG4
AG5
AG6
AG7
(0)
(1)
(2)
(3)
(4)
(5)
(6)
(7)
70

Fig.8

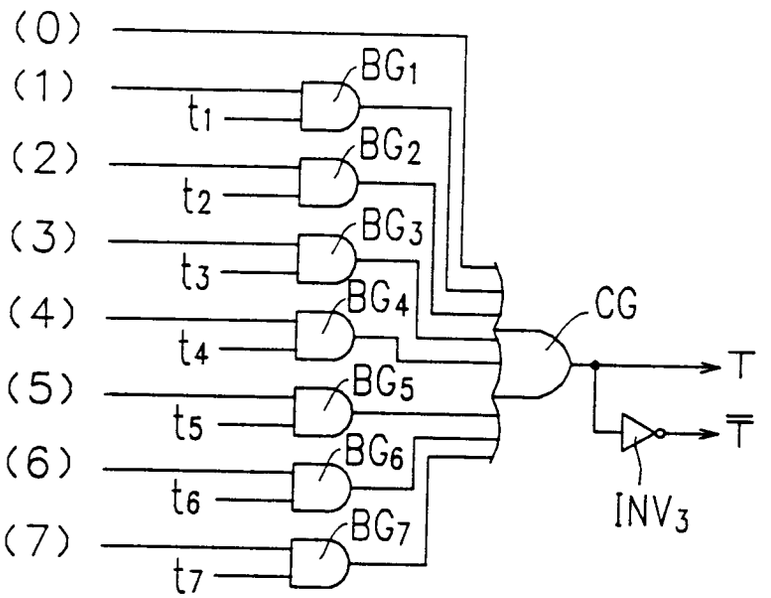
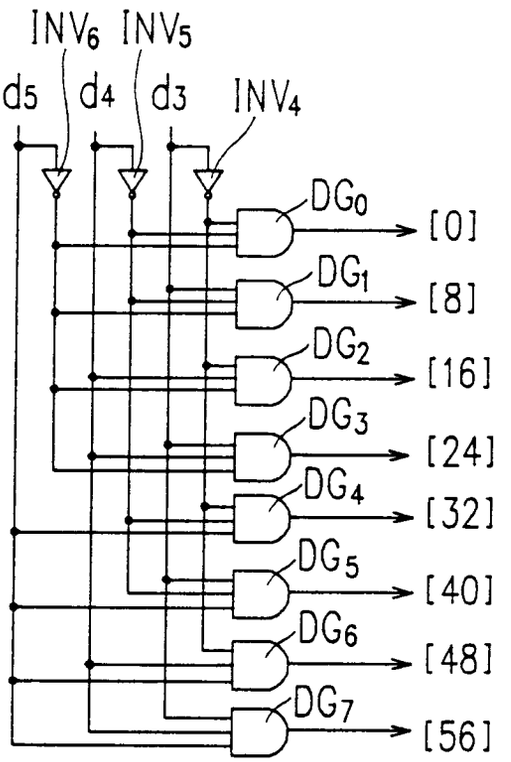
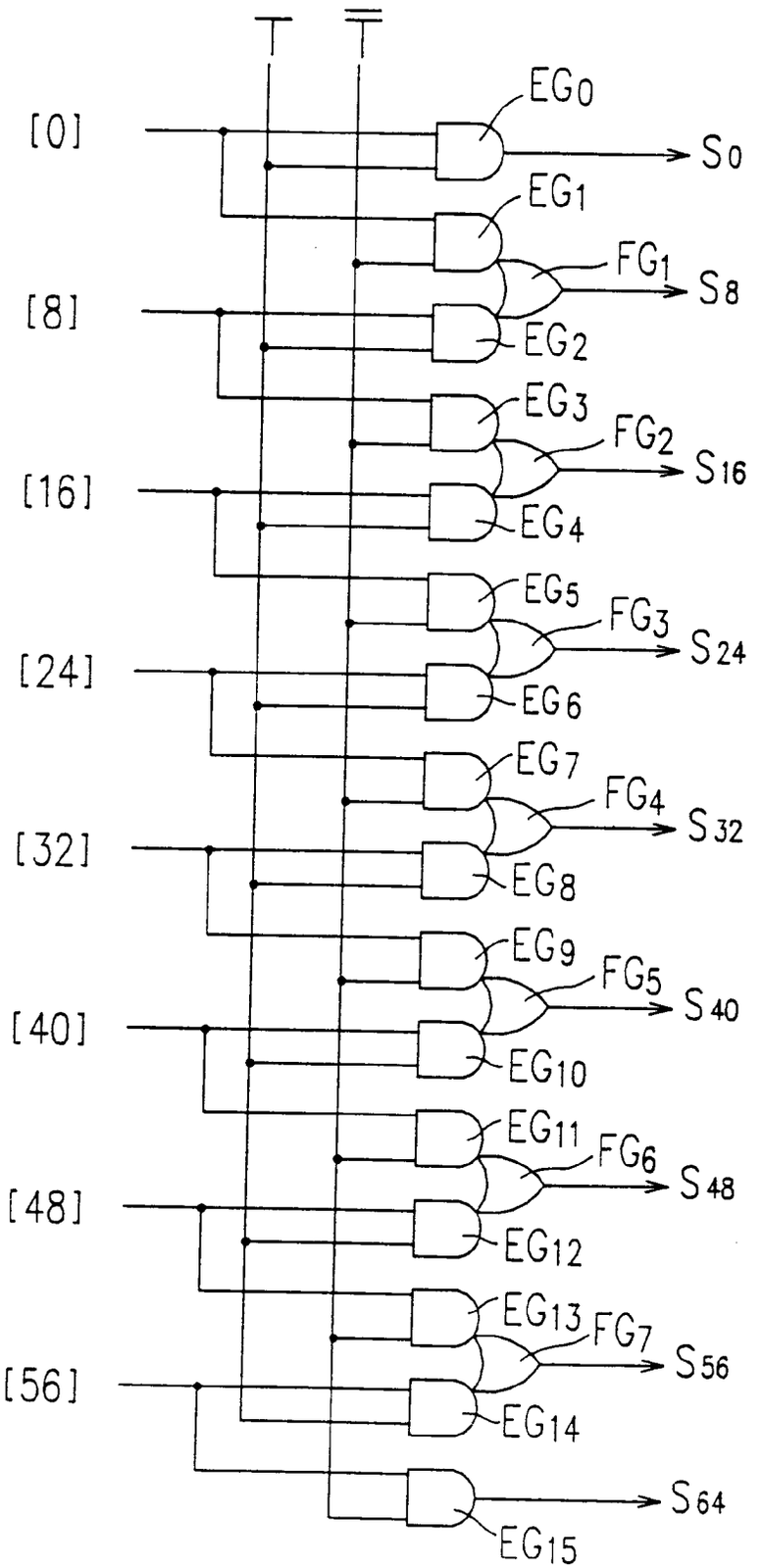

(0)
(1)
(2)
(3)
(4)
(5)
(6)
(7)
t1
t2
t3
t4
t5
t6
t7
BG1
BG2
BG3
BG4
BG5
BG6
BG7
CG
T
T
INV3
80

Fig.9


INV6
INV5
d5
d4
d3
INV4
DG0
DG1
DG2
DG3
DG4
DG5
DG6
DG7
[0]
[8]
[16]
[24]
[32]
[40]
[48]
[56]

90

Fig.10


[0]
[8]
[16]
[24]
[32]
[40]
[48]
[56]
EG0
EG1
FG1
EG2
EG3
FG2
EG4
EG5
FG3
EG6
EG7
FG4
EG8
EG9
FG5
EG10
EG11
FG6
EG12
EG13
FG7
EG14
EG15
S0
S8
S16
S24
S32
S40
S48
S56
S64

95

Fig.11

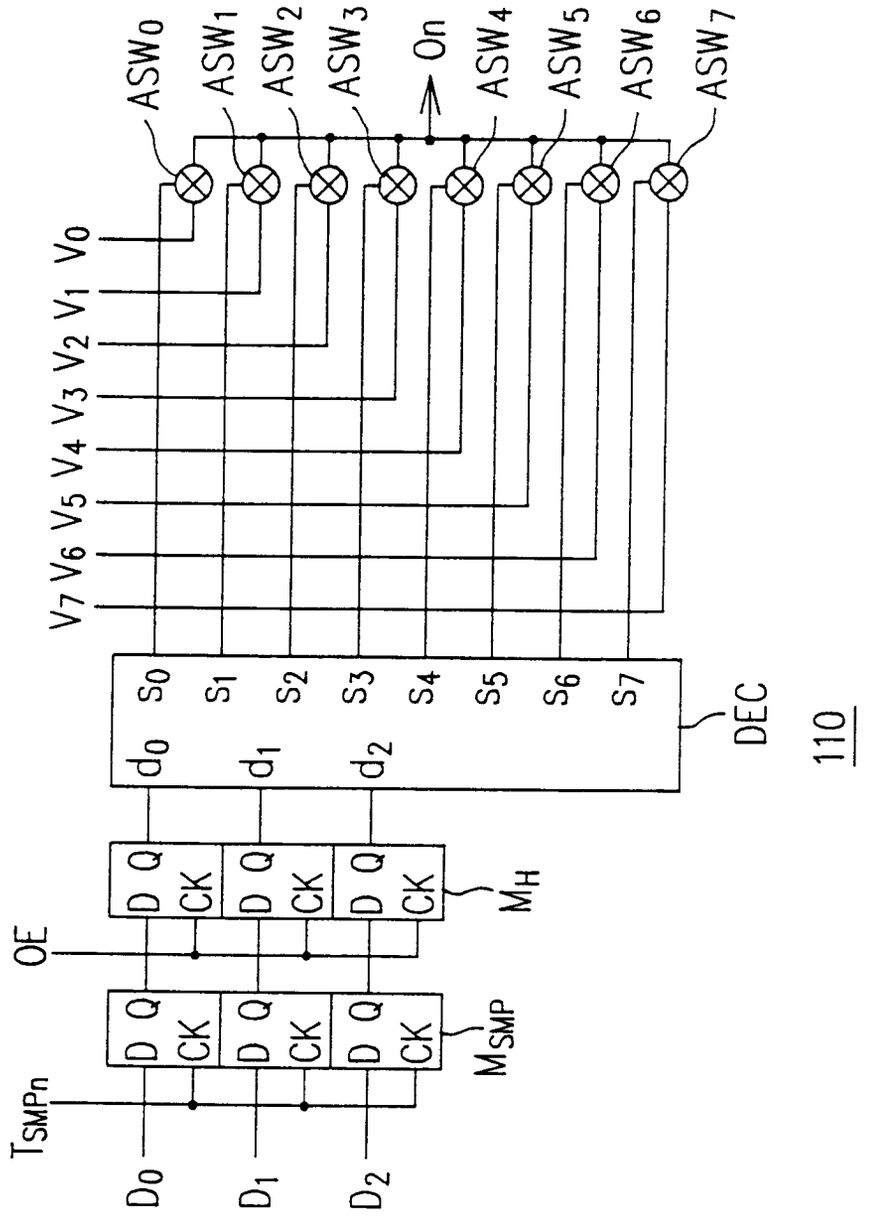


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Fig.12

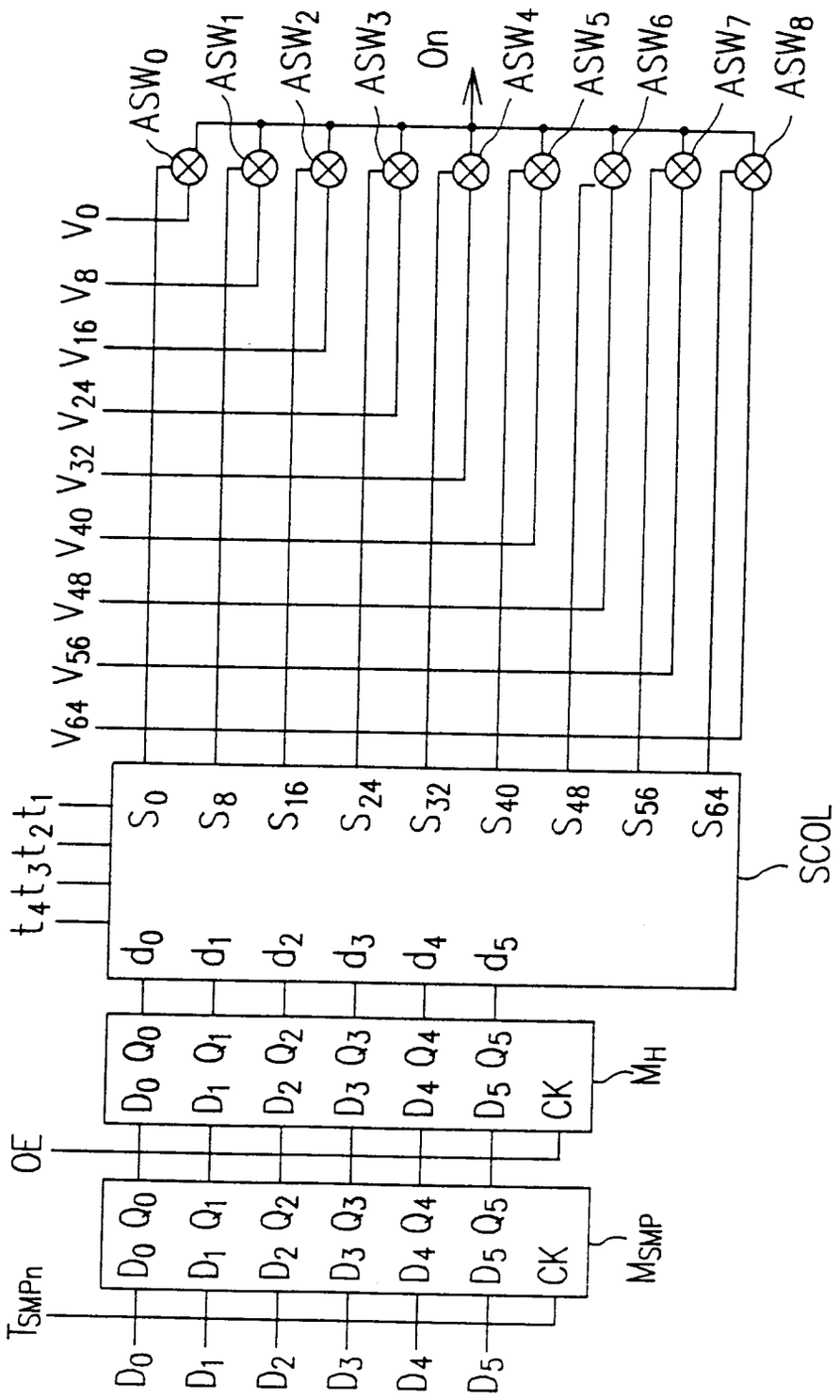

TSMPn
OE
D0
D1
D2
D3
D4
D5
MSMP
MH
t4 t3 t2 t1
d0 d1 d2 d3 d4 d5
S0 S8 S16 S24 S32 S40 S48 S56 S64
SCOL
V64 V56 V48 V40 V32 V24 V16 V8 V0
ASW0 ASW1 ASW2 ASW3 On ASW4 ASW5 ASW6 ASW7 ASW8
120

Fig.13

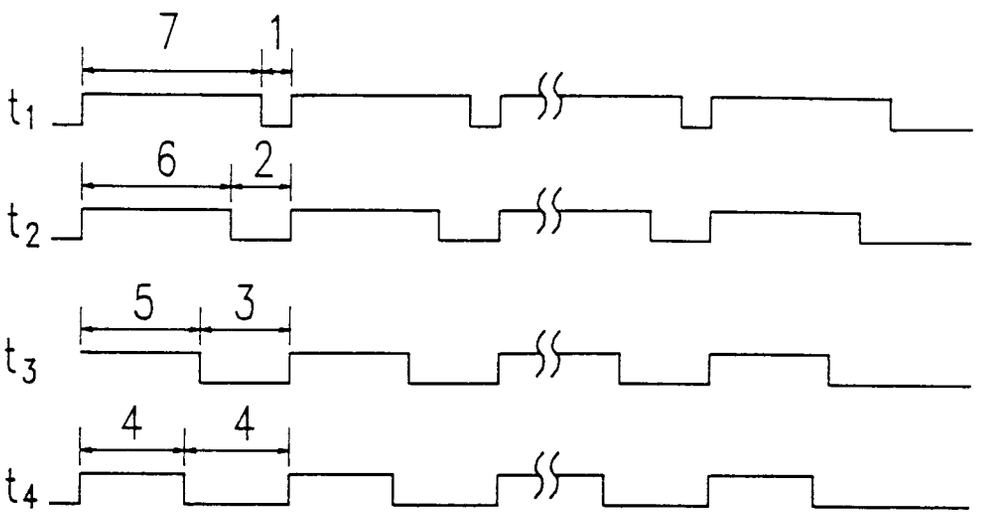


Fig.14

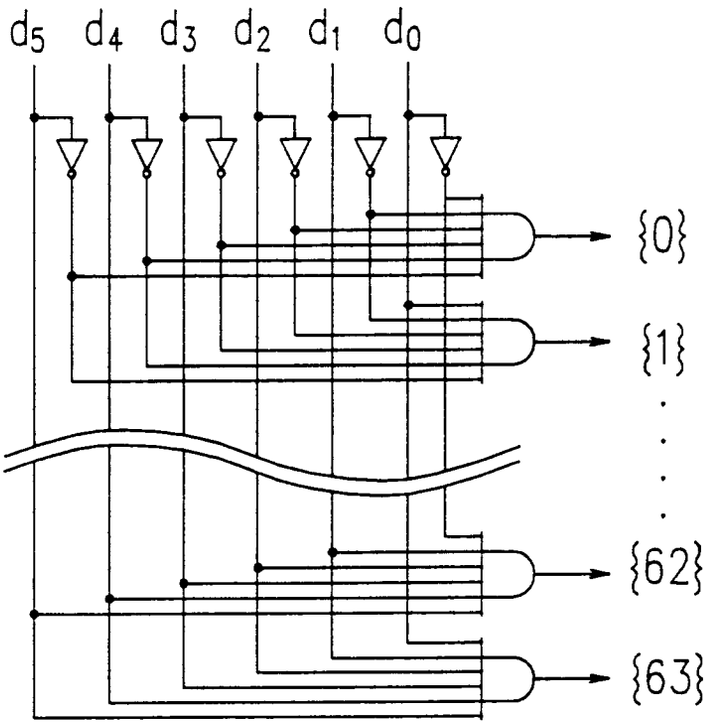
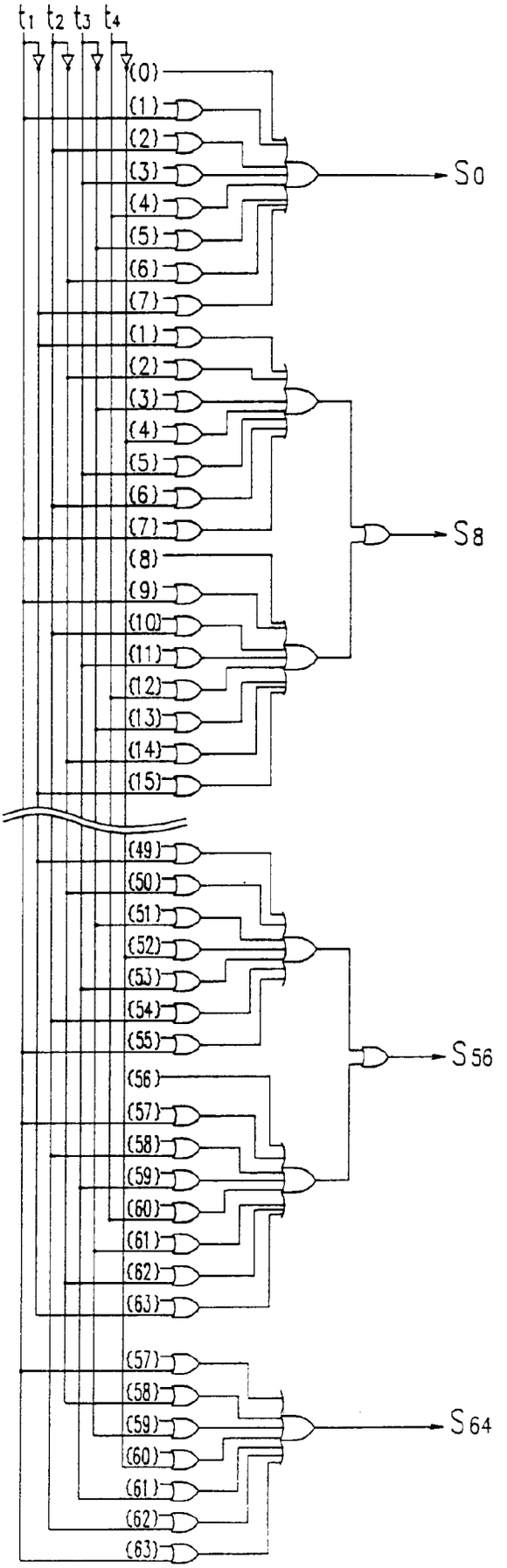


Fig.15


t1 t2 t3 t4
(0)
(1)
(2)
(3)
(4)
(5)
(6)
(7)
S0
(1)
(2)
(3)
(4)
(5)
(6)
(7)
(8)
(9)
(10)
(11)
(12)
(13)
(14)
(15)
S8
(49)
(50)
(51)
(52)
(53)
(54)
(55)
(56)
(57)
(58)
(59)
(60)
(61)
(62)
(63)
S56
(57)
(58)
(59)
(60)
(61)
(62)
(63)
S64