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Circuit de commande pour dispositif d'affichage

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**EP-A- 0 433 054**                      **EP-A- 0 515 191**

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## Description

**BACKGROUND OF THE INVENTION**

## 5 1. Field of the Invention:

[0001] The present invention relates to a driving circuit for a display apparatus. More particularly, the present invention relates to a driving circuit for an active matrix type liquid crystal display apparatus which displays an image with multiple gray scales in accordance with digital video signals.

## 10 2. Description of the Related Art:

[0002] An active matrix type liquid crystal display apparatus includes a display panel and a driving circuit for driving the display panel. The display panel includes a pair of glass substrates and a liquid crystal layer formed between the pair of glass substrates. On one of the pair of glass substrates, a plurality of gate lines and a plurality of data lines are formed. The driving circuit is disposed for every pixel in the display panel, and the driving circuit applies a driving voltage to the liquid crystal of the display panel. The driving circuit includes a gate driver for individually selecting one of a plurality of switching elements connected to the gate lines and the data lines, and a data driver for supplying a video signal corresponding to an image to pixel electrodes via the selected switching element.

20 [0003] Figure 11 shows a configuration of a part of a data driver in a prior art driving circuit. The circuit 110 shown in Figure 11 outputs a video signal to one of a plurality of data lines. Accordingly, the data driver requires circuits 110 the number of which is equal to the number of data lines provided in a display panel. For simplicity of explanation, it is herein assumed that video data consists of three bits ( $D_0, D_1, D_2$ ). On such an assumption, the video data may have eight values of 0 to 7, and a signal voltage supplied to each pixel is one of eight levels  $V_0-V_7$ .

25 [0004] The circuit 110 includes a sampling flip-flop  $M_{SMP}$ , a holding flip-flop  $M_H$ , a decoder DEC, and analog switches  $ASW_0-ASW_7$ . To each of the analog switches  $ASW_0-ASW_7$ , a corresponding one of external source voltages  $V_0-V_7$  of respective eight levels which are different from each other is supplied. In addition, to the analog switches  $ASW_0-ASW_7$ , control signals  $S_0-S_7$  are supplied from the decoder DEC, respectively. Each of the control signals  $S_0-S_7$  is used for switching the ON/OFF state of the respective analog switch.

30 [0005] Next, the operation of the circuit 110 is described. At the rising of a sampling pulse  $T_{SMPn}$  corresponding to the nth pixel, the sampling flip-flop  $M_{SMP}$  gets video data ( $D_0, D_1, D_2$ ), and holds the video data therein. When such video data sampling for one horizontal period is completed, an output pulse signal OE is applied to the holding flip-flop  $M_H$ . Upon receiving the output pulse signal OE, the holding flip-flop  $M_H$  gets the video data ( $D_0, D_1, D_2$ ) from the sampling flip-flop  $M_{SMP}$ , and transfers the video data to the decoder DEC.

35 [0006] The decoder DEC decodes the video data ( $D_0, D_1, D_2$ ), and produces a control signal for turning on one of the analog switches  $ASW_0-ASW_7$  in accordance with the respective values (0-7) of the video data ( $D_0, D_1, D_2$ ). As a result, one of the external source voltages  $V_0-V_7$  is output to a data line  $O_n$ . For example, in the case where the value of the video data held in the holding flip-flop  $M_H$  is 3, the decoder DEC outputs a control signal  $S_3$  which turns on the analog switch  $ASW_3$ . As a result, the analog switch  $ASW_3$  becomes into the ON-state, and  $V_3$  of the external source

40 [0007] Such a prior art data driver involves a problem in that, as the number of bits in video data increases, the circuit configuration becomes complicated and the size of the circuit is increased. This is because the prior art data driver requires gray-scale voltages the number of which is equal to the gray scales to be displayed. For example, in the case where the video data consists of 4 bits for displaying 16 gray-scale images, the number of required gray-scale voltages is:  $2^4 = 16$ . Similarly, in the case where the video data consists of 6 bits for displaying 64 gray-scale images, the number of required gray-scale voltages is:  $2^6 = 64$ . In the case of 8-bit video data for displaying 256 gray-scale images, the number of required gray-scale voltages is:  $2^8 = 256$ . As described above, the prior art data driver requires a large number of gray-scale voltages as the number of bits of video data increases. This causes the circuit configuration to be complicated and the circuit size to be increased. Moreover, interconnections between voltage source circuits and analog switches are also complicated.

50 [0008] For the above-mentioned reasons, the actual application of such a prior art data driver is limited to 3-bit video data or 4-bit video data.

[0009] In order to solve such prior art problems, there have been proposed methods and circuits for driving a display apparatus in Japanese Laid-Open Patent Publication Nos. 4-136983, 4-140787 corresponding to EP-A-0 478 386, and 6-27900 corresponding to EP-A-0 515 191.

55 [0010] Figure 12 shows a configuration for a part of a driving circuit disclosed in Japanese Laid-Open Patent Publication No. 6-27900. The circuit 120 shown in Figure 12 outputs a video signal to one of a plurality of data lines. Accordingly, the data driver requires circuits 120 the number of which is equal to the number of data lines provided in a

display panel. It is herein assumed that video data consists of 6 bits ( $D_0, D_1, D_2, D_3, D_4, D_5$ ). On such an assumption, the video data may have 64 values of 0-63, and a signal voltage applied to each pixel is one of nine gray-scale voltages  $V_0, V_8, V_{16}, V_{24}, V_{32}, V_{40}, V_{48}, V_{56}$ , and  $V_{64}$ , and a plurality of interpolated voltages which are produced from the gray-scale voltages  $V_0, V_8, V_{16}, V_{24}, V_{32}, V_{40}, V_{48}, V_{56}$ , and  $V_{64}$ .

5 [0011] The circuit 120 includes a sampling flip-flop  $M_{SMP}$ , a holding flip-flop  $M_H$ , a selection control circuit **SCOL**, and analog switches **ASW<sub>0</sub>-ASW<sub>8</sub>**. To each of the analog switches **ASW<sub>0</sub>-ASW<sub>8</sub>**, is applied a corresponding one of gray-scale voltages  $V_0, V_8, V_{16}, V_{24}, V_{32}, V_{40}, V_{48}, V_{56}$ , and  $V_{64}$  of respective levels which are different from each other. To the analog switches **ASW<sub>0</sub>-ASW<sub>8</sub>**, control signals  $S_0, S_8, S_{16}, S_{24}, S_{32}, S_{40}, S_{48}, S_{56}$ , and  $S_{64}$  are supplied from the selection control circuit **SCOL**, respectively. Each of the control signals are used to switch the ON/OFF state of the analog signal.

10 [0012] To the selection control circuit **SCOL**, clock signals  $t_1, t_2, t_3$ , and  $t_4$  are supplied. As is shown in Figure 13, the clock signals  $t_1, t_2, t_3$ , and  $t_4$  have duty ratios which are different from each other. The selection control circuit **SCOL** receives 6-bit video data  $d_5, d_4, d_3, d_2, d_1$ , and  $d_0$ , and outputs one of control signals  $S_0, S_8, S_{16}, S_{24}, S_{32}, S_{40}, S_{48}, S_{56}$ , and  $S_{64}$  in accordance with the value of the received video data. The relationship between the input and the output of the selection control circuit **SCOL** is determined by using a logical table.

15 [0013] Table 1 shows a logical table for the selection control circuit **SCOL**. The 1st to 6th columns of Table 1 indicate values of bits  $d_5, d_4, d_3, d_2, d_1$ , and  $d_0$  of the video data, respectively. The 7th to 15th columns of Table 1 indicate values of control signals  $S_0, S_8, S_{16}, S_{24}, S_{32}, S_{40}, S_{48}, S_{56}$ , and  $S_{64}$ , respectively. Each blank in the 7th to 15th columns in Table 1 means that the value of the control signal is 0. In addition, " $t_i$ " indicates that the value of the control signal is 1 when the value of the clock signal  $t_i$  is 1, and the value of the control signal is 0 when the value of the clock signal  $t_i$  is 0. Also, " $\bar{t}_i$ " indicates that the value of the control signal is 0 when the value of the clock signal  $t_i$  is 1, and the value of the control signal is 1 when the value of the clock signal  $t_i$  is 0. Herein,  $i = 1, 2, 3$ , and 4.

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Table 1

5	$d_5$	$d_4$	$d_3$	$d_2$	$d_1$	$d_0$	$S_0$	$S_8$	$S_{16}$	$S_{24}$	$S_{32}$	$S_{40}$	$S_{48}$	$S_{56}$	$S_{64}$
	0	0	0	0	0	0	1	0							
	0	0	0	0	0	1	$t_1$	$\overline{t_1}$							
10	0	0	0	0	1	0	$t_2$	$\overline{t_2}$							
	0	0	0	0	1	1	$t_3$	$\overline{t_3}$							
	0	0	0	1	0	0	$t_4$	$\overline{t_4}$							
15	0	0	0	1	0	1	$\overline{t_3}$	$t_3$							
	0	0	0	1	1	0	$\overline{t_2}$	$t_2$							
	0	0	0	1	1	1	$\overline{t_1}$	$t_1$							
	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0
20										$\overline{t_3}$	$t_3$				
	0	1	1	1	1	0				$\overline{t_2}$	$t_2$				
	0	1	1	1	1	1				$\overline{t_1}$	$t_1$				
25	1	0	0	0	0	0				1	$\overline{t_1}$				
	1	0	0	0	0	1				$t_1$	$\overline{t_2}$				
	1	0	0	0	1	0				$t_2$	$\overline{t_3}$				
30	1	0	0	0	1	1				$t_3$	$\overline{t_4}$				
	1	0	0	1	0	0				$t_4$	$\overline{t_3}$				
	1	0	0	1	0	1				$\overline{t_3}$	$t_3$				
35	1	0	0	1	1	0				$\overline{t_2}$	$t_2$				
	1	0	0	1	1	1				$\overline{t_1}$	$t_1$				
	1	0	1	0	0	0	0	0	0	0	1	0	0	0	0
40												$\overline{t_3}$	$t_3$		
	1	1	0	1	1	0						$\overline{t_2}$	$t_2$	0	
	1	1	0	1	1	1						$\overline{t_1}$	$t_1$	0	
45	1	1	1	0	0	0						1	$\overline{t_1}$		
	1	1	1	0	0	1						$t_1$	$\overline{t_2}$		
	1	1	1	0	1	0						$t_2$	$\overline{t_3}$		
	1	1	1	0	1	1						$t_3$	$\overline{t_4}$		
50	1	1	1	1	0	0						$t_4$	$\overline{t_3}$		
	1	1	1	1	0	1						$\overline{t_3}$	$t_3$		
	1	1	1	1	1	0						$\overline{t_2}$	$t_2$		
55	1	1	1	1	1	1						$\overline{t_1}$	$t_1$		

[0014] As is seen from Table 1, when the value of the video data is a multiple of 8, one of the gray-scale voltages

$V_0, \dots, V_{64}$  is output to the data line  $O_n$ . When the value of the video data is not a multiple of 8, an oscillating voltage which oscillates between a pair of gray-scale voltages  $V_0, \dots, V_{64}$  at a duty ratio of one of the clock signals  $t_1, t_2, t_3,$  and  $t_4$  is output to the data line  $O_n$ . The data driver **120** produces seven different oscillating voltages between respective adjacent gray-scale voltages, in accordance with the logical table of Table 1. Thus, it is possible to attain 64 gray-scale images by using only 9 levels of gray-scale voltages.

**[0015]** The following equations are logical equations which define the relationships among the video data  $d_5, d_4, d_3, d_2, d_1,$  and  $d_0,$  the clock signals  $t_1, t_2, t_3,$  and  $t_4,$  and the control signals  $S_0, S_8, S_{16}, S_{24}, S_{32}, S_{40}, S_{48}, S_{56},$  and  $S_{64}$  shown in Table 1.

$$S_0 = \{0\} + \{1\}t_1 + \{2\}t_2 + \{3\}t_3 + \{4\}t_4 + \{5\}t_3 + \{6\}t_2 + \{7\}t_1 \quad (1)$$

$$S_8 = \{1\}t_1 + \{2\}t_2 + \{3\}t_3 + \{4\}t_4 + \{5\}t_3 + \{6\}t_2 + \{7\}t_1 + \{8\} + \{9\}t_1 + \{10\}t_2 + \{11\}t_3 + \{12\}t_4 + \{13\}t_3 + \{14\}t_2 + \{15\}t_1 \quad (2)$$

$$S_{16} = \{9\}t_1 + \{10\}t_2 + \{11\}t_3 + \{12\}t_4 + \{13\}t_3 + \{14\}t_2 + \{15\}t_1 + \{16\} + \{17\}t_1 + \{18\}t_2 + \{19\}t_3 + \{20\}t_4 + \{21\}t_3 + \{22\}t_2 + \{23\}t_1 \quad (3)$$

**[0016]** Similarly, the control signals  $S_{24}, S_{32}, S_{40},$  and  $S_{48}$  are defined. The control signals  $S_{56}$  and  $S_{64}$  are defined as follows.

$$S_{56} = \{49\}t_1 + \{50\}t_2 + \{51\}t_3 + \{52\}t_4 + \{53\}t_3 + \{54\}t_2 + \{55\}t_5 + \{56\} + \{57\}t_1 + \{58\}t_2 + \{59\}t_3 + \{60\}t_4 + \{61\}t_3 + \{62\}t_2 + \{63\}t_1 \quad (4)$$

$$S_{64} = \{57\}t_1 + \{58\}t_2 + \{59\}t_3 + \{60\}t_4 + \{61\}t_3 + \{62\}t_2 + \{63\}t_1 \quad (5)$$

**[0017]** In the above equations,  $\{i\}$  indicates a value when the binary data ( $d_5, d_4, d_3, d_2, d_1, d_0$ ) is represented in the decimal notation. For example,  $\{1\} = (d_5, d_4, d_3, d_2, d_1, d_0) = (0, 0, 0, 0, 0, 1)$ . In addition, " $t_i$ " indicates a signal which is inverted from the signal  $t_i$ .

**[0018]** On the basis of the above logical equations, logical circuits shown in Figures **14** and **15** are obtained. The selection control circuit **SCOL** is constructed by the logical circuits shown in Figures **14** and **15**.

**[0019]** The logical circuit shown in Figure **14** produces 64 kinds of gray-scale selection data  $\{0\} - \{63\}$  in accordance with the value of 6-bit video data ( $d_5, d_4, d_3, d_2, d_1, d_0$ ). The logical circuit shown in Figure **15** produces control signals  $S_0, S_8, S_{16}, S_{24}, S_{32}, S_{40}, S_{48}, S_{56},$  and  $S_{64},$  based on the gray-scale selection data  $\{0\} - \{63\}$  and the clock signals  $t_1, t_2, t_3,$  and  $t_4.$  For example, a case where the video data ( $d_5, d_4, d_3, d_2, d_1, d_0$ ) = (0, 0, 0, 0, 0, 1) is input to the selection control circuit **SCOL** is explained. In such a case, the logical circuit shown in Figure **14** outputs the gray-scale selection data (1). The logical circuit shown in Figure **15** receives the gray-scale selection data (1) and alternately outputs the control signal  $S_0$  and the control signal  $S_8$  at a duty ratio of the clock signal  $t_1.$  As a result, the gray-scale voltage  $V_0$

and the gray-scale voltage  $V_g$  are alternately output via the analog switch  $ASW_0$  and the analog switch  $ASW_1$  at the duty ratio of the clock signal  $t_1$  to the data line  $O_n$ .

[0020] The actual data driver requires the selection control circuits **SCOL** the number of which is equal to the number of data lines. Thus, the circuit scale of the selection control circuit **SCOL** largely affects the chip size of the integrated circuit on which the data driver is installed. If the circuit scale of the selection control circuit **SCOL** becomes large, the cost for the integrated circuit is increased. Moreover, if the number of bits of video data increases in order to realize an image with a larger number of gray scales, the circuit scale of the data driver is further increased. This also increases the size and the production cost of the integrated circuit.

[0021] The present invention provides a driving circuit for driving a display apparatus, the display apparatus including pixels and data lines for applying voltages to said pixels and displaying, in use, an image with multiple grey scales in accordance with video data consisting of a plurality of bits, said driving circuit comprising:

oscillating voltage selecting means for selecting one of a plurality of oscillating signals oscillating between first and second predetermined levels and having respective duty ratios which are different from each other in accordance with video data consisting of bits selected from said plurality of bits, and for outputting said selected oscillating signal and an inverted oscillating signal which is obtained by inverting said selected oscillating signal;

grey-scale voltage selecting means for producing grey-scale voltage selecting signals which select a first grey-scale voltage and a second grey-scale voltage from a plurality of grey-scale voltages supplied by a grey-scale voltage supply means, in accordance with video data consisting of bits other than said selected bits of said plurality of bits; and

output means for outputting said first grey-scale voltage and said second grey-scale voltage selected by said grey-scale voltage selecting means to said data lines, in accordance with said oscillating signal and said inverted oscillating signal, the output means outputting the first grey scale voltage when the oscillating signal is at said first predetermined level and the second selected grey scale voltage when the inverted oscillating signal is at said first predetermined level.

[0022] In a preferred embodiment, the first grey-scale voltage and said second grey-scale voltage are adjacent ones of said plurality of grey-scale voltages.

[0023] In a preferred embodiment, the plurality of oscillating signals include oscillating signals having duty ratios of 8:0, 7:1, 6:2, 5:3, 4:4, 3:5, 2:6, and 1:7, respectively.

[0024] In a preferred embodiment, the output means comprises

(a) control signal output means for outputting a first control signal which oscillates at substantially the same duty ratio as that of said oscillating signal to one of said switching means which is supplied with said first grey-scale voltage selected by said grey-scale voltage selecting signals and for outputting a second control signal which oscillates at substantially the same duty ratio as that of said inverted oscillating signal to one of said switching means which is supplied with said second grey-scale voltage selected by said grey-scale voltage selecting signals; and

(b) a plurality of switching means, each of said plurality of switching means being supplied with a corresponding one of said plurality of control signals and a corresponding one of the plurality of grey-scale voltages, said grey-scale voltage supplied to said switching means being output to said data lines via said switching means in accordance with said control signal.

[0025] In a preferred embodiment, the switching means is an analogue switch.

[0026] According to the driving circuit of the invention, a pair of gray-scale voltages are selected (specified) among a plurality of gray-scale voltages, and one of a plurality of oscillating signals is specified. The driving circuit outputs a voltage signal which oscillates between the specified pair of gray-scale voltages at the oscillating frequency of the specified oscillating signal. Therefore, a plurality of interpolated gray scales can be realized between a plurality of applied gray-scale voltages.

[0027] According to the driving circuit of the invention, by using the gray-scale voltage specifying means and the oscillating signal specifying means, it is possible to always realize an image display with multiple gray scales in both cases where the driving circuit directly outputs one of the plurality of gray-scale voltages and where the driving circuit alternately outputs the specified pair of gray-scale voltages.

[0028] Accordingly, it is unnecessary to provide an additional driving circuit depending on the cases where the driving circuit directly outputs one of the plurality of gray-scale voltages and where the driving circuit alternately outputs the specified pair of gray-scale voltages. As a result, it is possible to simplify the configuration of the driving circuit, and the size of the driving circuit can be minimized.

[0029] Thus, the invention described herein makes possible the advantage of providing a driving circuit for a display

apparatus, which has a simplified and small construction, and which can display an image with multiple gray scales in accordance with multi-bit video data.

[0030] This and other advantages of the present invention will become apparent to those skilled in the art upon reading and understanding the following detailed description with reference to the accompanying figures.

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### **BRIEF DESCRIPTION OF THE DRAWINGS**

[0031] Figure 1 is a diagram showing a construction of a liquid crystal display apparatus.

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[0032] Figure 2 is a timing chart illustrating the relationship among input data, sampling pulses, and an output pulse in one horizontal period.

[0033] Figure 3 is a timing chart illustrating the relationship among input data, an output pulse, an output voltage, and a gate pulse in one vertical period.

[0034] Figure 4 is a timing chart illustrating the relationship among input data, an output pulse, an output voltage, a gate pulse, and a voltage applied to a pixel in one vertical period.

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[0035] Figure 5 shows waveforms of an output voltage oscillating in one output period.

[0036] Figure 6 is a diagram showing a part of a configuration for a data driver in a driving circuit in an example according to the invention.

[0037] Figure 7 is a diagram showing a part of a configuration of a selection control circuit **SCOL** in the driving circuit in the example according to the invention.

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[0038] Figure 8 is a diagram showing another part of the configuration of the selection control circuit **SCOL** in the driving circuit in the example according to the invention.

[0039] Figure 9 is a diagram showing another part of the configuration of the selection control circuit **SCOL** in the driving circuit in the example according to the invention.

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[0040] Figure 10 is a diagram showing another part of the configuration of the selection control circuit **SCOL** in the driving circuit in the example according to the invention.

[0041] Figure 11 is a diagram showing a part of a configuration for a data driver in a conventional driving circuit.

[0042] Figure 12 is a diagram showing a part of a configuration of a data driver in a driving circuit of a related art.

[0043] Figure 13 shows waveforms of signals  $t_1$ - $t_4$  supplied to a selection control circuit **SCOL**.

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[0044] Figure 14 is a diagram showing a part of a configuration of a selection control circuit **SCOL** in the conventional driving circuit.

[0045] Figure 15 is a diagram showing another part of the configuration of a selection control circuit **SCOL** in the conventional driving circuit.

### **DESCRIPTION OF THE PREFERRED EMBODIMENTS**

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[0046] Hereinafter, the present invention will be described by way of illustrative examples in accordance with the accompanying drawings. In the following description, a matrix type liquid crystal display apparatus is used as an example of a display apparatus. It is appreciated that the present invention is applicable to other types of display apparatus.

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[0047] Figure 1 shows a construction of a matrix type liquid crystal display apparatus. The liquid crystal display apparatus shown in Figure 1 includes a display section **100** for displaying a video image, and a driving circuit **101** for driving the display section **100**. The driving circuit **101** includes a data driver **102** which provides video signals to the display section **100** and a scanning driver **103** which provides scanning signals to the display section **100**. The data driver may be called "a source driver" or "a column driver". The scanning driver may be called "a gate driver" or "a row driver".

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[0048] The display section **100** includes an  $M \times N$  array of pixels **104** ( $M$  pixels in each column and  $N$  pixels in each row; where  $M$  and  $N$  are positive integers), and also includes switching elements **105** respectively connected to the pixels **104**.

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[0049] In Figure 1,  $N$  data lines **106** are used for connecting respective output terminals **S(i)** ( $i = 1, 2, \dots, N$ ) of the data driver **102** to the corresponding switching elements **105**. Similarly,  $M$  scanning lines **107** are used for connecting respective output terminals **G(j)** ( $j = 1, 2, \dots, M$ ) of the scanning driver **103** to the corresponding switching elements **105**. As the switching elements **105**, thin film transistors (TFTs) can be used. Alternatively, other types of switching elements may also be used. The data line may be called "a source line" or "a column line". The scanning line may be called "a gate line" or "a row line".

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[0050] The scanning driver **103** sequentially outputs a voltage which is kept at a high level during a specific time period from its output terminals **G(j)** to the corresponding scanning lines **107**. The specific time period is referred to as one horizontal period  $jH$  (where  $j$  is an integer of 1 to  $M$ ). The total length of time obtained by adding up all the horizontal periods  $jH$  (i.e.,  $1H + 2H + 3H + \dots + MH$ ), a blanking period and a vertical synchronizing period is referred to as one

vertical period.

[0051] When the level of the voltage which is output from the output terminal **G(j)** of the scanning driver **103** to the scanning line **107** is high, the switching element **105** connected to the output terminal **G(j)** is in the ON-state. When the switching element **105** is in the ON-state, the pixel **104** connected to the switching element **105** is charged in accordance with the voltage which is output from the output terminal **S(j)** of the data driver **102** to the corresponding data line **106**. The voltage of the thus charged pixel **104** remains unchanged for about one vertical period until it is charged again by the subsequent voltage to be supplied from the data driver **102**.

[0052] Figure **2** shows the relationship among digital video data DA, sampling pulses  $T_{\text{smp}i}$ , and an output pulse signal OE, during the *j*th horizontal period *jH* determined by a horizontal synchronizing signal  $H_{\text{syn}}$ . As can be seen from Figure **2**, while sampling pulses  $T_{\text{smp}1}$ ,  $T_{\text{smp}2}$ , ...,  $T_{\text{smp}i}$ , ..., and  $T_{\text{smp}N}$  are sequentially applied to the data driver **102**, digital video data  $DA_1$ ,  $DA_2$ , ...,  $DA_i$ , ..., and  $DA_N$  are fed into the data driver **102** accordingly. The *j*th output pulse  $OE_j$  determined by the output pulse signal OE is then applied to the data driver **102**. On receiving the *j*th output pulse  $OE_j$ , the data driver **102** outputs voltages from its output terminals **S(i)** to the corresponding data lines **106**.

[0053] Figure **3** shows the relationship among the horizontal synchronizing signal  $H_{\text{syn}}$ , the digital video data DA, the output pulse signal OE, and the timing of outputs of the data driver **102** and scanning driver **103**, during one vertical period determined by a vertical synchronizing signal  $V_{\text{syn}}$ . In Figure **3**, a SOURCE(*j*) indicates a level range of voltages output from the data driver **102**, with such timing as shown in Figure **2** and in accordance with the digital video data applied during the horizontal period *jH*. The SOURCE(*j*) is shown as a hatched rectangular area to indicate a level range of voltages output from all the *N* output terminals **S(1)** to **S(N)** of the data driver **102**. While the voltages indicated by the SOURCE(*j*) are applied to the data lines **106**, the voltage which is output from the *j*th output terminal **G(j)** of the scanning driver **103** to the *j*th scanning line **107** is changed to and kept at a high level, thereby turning on all the *N* switching elements **105** connected to the *j*th scanning line **107**. As a result, the *N* pixels **104** respectively connected to these *N* switching elements **105** are charged in accordance with the voltage applied to the corresponding data lines **106** from the data driver **102**.

[0054] The above-described process is repeated *M* times, i.e., for the 1st to *M*th scanning lines **107**, so that an image corresponding to one vertical period is displayed. In the case of non-interlace type display apparatus, the produced image serves as a complete display image on the display screen thereof.

[0055] In this specification, the time interval between the *j*th output pulse  $OE_j$  and the (*j*+1)th output pulse  $OE_{j+1}$  in the output pulse signal OE is defined as "one output period". This means that one output period is equal to a period represented by SOURCE(*j*) shown in Figure **3**. In cases where usual line sequential scanning is performed, it is preferable that one output period is made equal to one horizontal period. The reason for this is as follows. While the data driver **102** outputs voltages corresponding to digital video data for one horizontal (scanning) line, to the data lines **106**, it also performs sampling of digital video data for the next horizontal line. The maximum allowable length of time during which these voltages can be output from the data driver **102** is equal to one horizontal period. Furthermore, except for special cases, as the output period becomes longer, the pixels can be charged more accurately. In the driving circuit described herein, therefore, one output period is equal to one horizontal period. According to the present invention, however, one output period is not necessarily required to be equal to one horizontal period.

[0056] Figure **4** shows, in addition to the timings of the respective signals shown in Figures **2** and **3**, the levels of voltages which are applied to the pixels  $P(j, i)$  (*j* = 1, 2, ..., *M*) in accordance with the timings.

[0057] Figure **5** shows an exemplary waveform for a voltage signal output from the data driver **102** to the data lines **106** in one output period. In the case of the conventional data driver, the voltage level of the voltage signal output to the data lines **106** is constant during one output period. On the other hand, from the data driver **102** in this example according to the invention, the voltage signal output to the data lines **106** includes an oscillating component which oscillates during one output period. As is shown in Figure **5**, the voltage signal is a pulse-like signal, and a ratio of a high-level period to a low-level period, i.e., a duty ratio *n:m* is selected as described below.

[0058] Figure **6** shows a configuration of a part of the data driver **102** in the driving circuit **101**. The circuit **60** shown in Figure **6** outputs a video signal from an *n*th output terminal **S(n)** to one data line **106**. The data driver **102** includes circuits **60** the number of which is equal to the number of the data lines **106** provided in the display section **100**. Herein, it is assumed that the video data consists of 6 bits ( $D_0, D_1, D_2, D_3, D_4, D_5$ ). On such an assumption, the video data may have 64 kinds of values of 0 - 63, and a signal voltage applied to each pixel is one of nine gray-scale voltages  $V_0, V_8, V_{16}, V_{24}, V_{32}, V_{40}, V_{48}, V_{56},$  and  $V_{64}$ , and interpolated voltages which are produced from any pair of the gray-scale voltages chosen from  $V_0, V_8, V_{16}, V_{24}, V_{32}, V_{40}, V_{48}, V_{56},$  and  $V_{64}$ .

[0059] The circuit **60** includes a sampling flip-flop  $M_{\text{SMP}}$  which performs the sampling operation, a holding flip-flop  $M_{\text{H}}$  which performs the holding operation, a selection control circuit **SCOL**, and analog switches  $ASW_0$ - $ASW_8$ . To each of the analog switches  $ASW_0$ - $ASW_8$ , a corresponding one of nine gray-scale voltages  $V_0, V_8, V_{16}, V_{24}, V_{32}, V_{40}, V_{48}, V_{56},$  and  $V_{64}$  is supplied. The gray-scale voltages  $V_0$ - $V_{64}$  have respective levels which are different from each other. The selection control circuit **SCOL** is provided with seven oscillating signals  $t_1$ - $t_7$ . The oscillating signals  $t_1$ - $t_7$  have respective duty ratios which are different from each other.

[0060] As the sampling flip-flop  $M_{SMP}$  and the holding flip-flop  $M_H$ , for example, D-type flip-flops can be used. It is appreciated that such sampling and holding flip-flops can be realized by using other types of circuit elements.

[0061] Next, by referring to Figure 6, the operation of the circuit 60 is described. At the rising of a sampling pulse  $T_{SMPn}$  corresponding to the nth pixel, the sampling flip-flop  $M_{SMP}$  gets video data ( $D_0, D_1, D_2, D_3, D_4, D_5$ ), and holds the video data therein. When such video data sampling for one horizontal period is completed, an output pulse signal OE is applied to the holding flip-flop  $M_H$ . When the output pulse signal OE is applied, the video data held in the sampling flip-flop  $M_{SMP}$  is fed into the holding flip-flop  $M_H$  and output to the selection control circuit SCOL. The selection control circuit SCOL receives the video data, and produces a plurality of control signals in accordance with the value of the video data. The control signals are used for switching the ON/OFF states of the respective analog switches  $ASW_0$ - $ASW_8$ . The video data input to the selection control circuit SCOL is represented by  $d_0, d_1, d_2, d_3, d_4$ , and  $d_5$ , and the control signals output from the selection control circuit SCOL are represented by  $S_0, S_8, S_{16}, S_{24}, S_{32}, S_{40}, S_{48}, S_{56}$ , and  $S_{64}$ .

[0062] Table 2 is a logical table for the lower three bits  $d_2, d_1$ , and  $d_0$  of the 6-bit video data. The 1st to 3rd columns of Table 2 indicate the values of video data bits  $d_2, d_1$ , and  $d_0$ , respectively. The 4th to 11th columns of Table 2 indicate which oscillating signal is specified from the oscillating signals  $t_0$ - $t_7$ . In the 4th to 11th columns of Table 2, the oscillating signal which is indicated by a value of 1 is specified. For example, in the case of  $(d_2, d_1, d_0) = (0, 0, 0)$ , the oscillating signal  $t_0$  is specified. In this example, the oscillating signals  $t_0$ - $t_7$  are clock signals having duty ratios of 8:0, 7:1, 6:2, 5:3, 4:4, 3:5, 2:6, and 1:7, respectively. Herein, if an oscillating signal has a duty ratio of k:0 or 0:k (k is a natural number), the oscillating signal is defined as always being at a fixed level. The oscillating signals  $t_5, t_6$ , and  $t_7$  are the signals obtained by inverting the oscillating signals  $t_3, t_2$ , and  $t_1$ .

Table 2

$d_2$	$d_1$	$d_0$	$t_0$	$t_1$	$t_2$	$t_3$	$t_4$	$t_5$	$t_6$	$t_7$
0	0	0	1							
0	0	1		1						
0	1	0			1					
0	1	1				1				
1	0	0					1			
1	0	1						1		
1	1	0							1	
1	1	1								1

[0063] From the logical table of Table 2, the following logical equation is obtained.

$$T = (0)t_0 + (1)t_1 + (2)t_2 + (3)t_3 + (4)t_4 + (5)t_5 + (6)t_6 + (7)t_7 \tag{6}$$

[0064] In the above equation, (i) indicates a value of binary data ( $d_2, d_1, d_0$ ) which is represented in a decimal notation. That is,  $(0) = (d_2, d_1, d_0) = (0, 0, 0)$ ,  $(1) = (d_2, d_1, d_0) = (0, 0, 1)$ ,  $(2) = (d_2, d_1, d_0) = (0, 1, 0)$ ,  $(3) = (d_2, d_1, d_0) = (0, 1, 1)$ ,  $(4) = (d_2, d_1, d_0) = (1, 0, 0)$ ,  $(5) = (d_2, d_1, d_0) = (1, 0, 1)$ ,  $(6) = (d_2, d_1, d_0) = (1, 1, 0)$ , and  $(7) = (d_2, d_1, d_0) = (1, 1, 1)$ .

[0065] The oscillating signal  $t_0$  is continually at a level of "1", so that Equation (6) can alternatively be represented as the following equation.

$$T = (0) + (1)t_1 + (2)t_2 + (3)t_3 + (4)t_4 + (5)t_5 + (6)t_6 + (7)t_7 \tag{7}$$

[0066] Table 3 is a logical table representing the relationships among the upper three bits  $d_5, d_4$ , and  $d_3$  of the 6-bit video data, and the control signals  $S_0, S_8, S_{16}, S_{24}, S_{32}, S_{40}, S_{48}, S_{56}$ , and  $S_{64}$ . In Table 3, a variable T denotes a signal T which is defined by Equations (6) and (7). A variable  $\bar{T}$  denotes an inverted signal  $\bar{T}$  obtained by inverting the signal T.

Table 3

	d <sub>5</sub>	d <sub>4</sub>	d <sub>3</sub>	S <sub>0</sub>	S <sub>8</sub>	S <sub>16</sub>	S <sub>24</sub>	S <sub>32</sub>	S <sub>40</sub>	S <sub>48</sub>	S <sub>56</sub>	S <sub>64</sub>
5	0	0	0	T	$\bar{T}$							
	0	0	1		T	$\bar{T}$						
	0	1	0			T	$\bar{T}$					
	0	1	1				T	$\bar{T}$				
10	1	0	0					T	$\bar{T}$			
	1	0	1						T	$\bar{T}$		
	1	1	0							T	$\bar{T}$	
15	1	1	1								T	$\bar{T}$

[0067] From the logical table of Table 3, the following logical equations are obtained.

$$S_0 = [0]T \quad (8)$$

$$S_8 = [0]T + [8]T \quad (9)$$

$$S_{16} = [8]T + [16]T \quad (10)$$

$$S_{24} = [16]T + [24]T \quad (11)$$

$$S_{32} = [24]T + [32]T \quad (12)$$

$$S_{40} = [32]T + [40]T \quad (13)$$

$$S_{48} = [40]T + [48]T \quad (14)$$

$$S_{56} = [48]T + [56]T \quad (15)$$

$$S_{64} = [56]T \quad (16)$$

[0068] In the above equations, [i] indicates a value of binary data (d<sub>5</sub>, d<sub>4</sub>, d<sub>3</sub>), where i = (8 × j), and j is a value of binary data (d<sub>5</sub>, d<sub>4</sub>, d<sub>3</sub>) which is represented in a decimal notation. For example, [8] = (d<sub>5</sub>, d<sub>4</sub>, d<sub>3</sub>) = (0, 0, 1). In addition, "T" denotes an inverted signal of the signal T.

[0069] In accordance with the respective logical equations which are described above, logical circuits 70, 80, 90, and 95 shown in Figures 7 through 10 are obtained. The selection control circuit SCOL is constructed, for example, by the logical circuits 70, 80, 90, and 95 shown in Figures 7 through 10.

[0070] The logical circuit 70 shown in Figure 7 selectively outputs oscillating signal specifying signals (0)-(7) for specifying one of a plurality of oscillating signals t<sub>0</sub>-t<sub>7</sub>, in accordance with the lower 3 bits d<sub>2</sub>, d<sub>1</sub>, and d<sub>0</sub> of the video data. More specifically, the video data d<sub>2</sub>, d<sub>1</sub>, and d<sub>0</sub> and the inverted signals which are respectively obtained by inverting the video data d<sub>2</sub>, d<sub>1</sub>, and d<sub>0</sub> by inverter circuits INV<sub>0</sub> to INV<sub>2</sub> are input into AND circuits AG<sub>0</sub>-AG<sub>7</sub> in such combinations that constitute 0-7 in binary notation. The oscillating signal specifying signals (0)-(7) are thus obtained as the outputs of the AND circuits AG<sub>0</sub>-AG<sub>7</sub>.

[0071] The logical circuit **80** shown in Figure **8** specifies one of the plurality of oscillating signals  $t_0$ - $t_7$  in accordance with the oscillating signal specifying signals, and produces the specified oscillating signal  $T$  and the inverted oscillating signal  $\bar{T}$  which is obtained by inverting the specified oscillating signal  $T$  by an inverter circuit **INV<sub>3</sub>**. More specifically, the oscillating signal specifying signals (1)-(7) and the oscillating signals  $t_1$ - $t_7$  are input into AND circuits **BG<sub>1</sub>-BG<sub>7</sub>**, respectively, as is shown in Figure **8**. The oscillating signal specifying signal (0) and the outputs of the AND circuits **BG<sub>1</sub>-BG<sub>7</sub>** are supplied to an OR circuit **CG**. The oscillating signal  $T$  and the inverted oscillating signal  $\bar{T}$  are obtained as the output of the OR circuit **CG**.

[0072] The logical circuit **90** shown in Figure **9** selectively outputs gray-scale voltage specifying signals [0], [8], [16], [24], [32], [40], [48], and [56] for specifying a pair of gray-scale voltages from among a plurality of gray-scale voltages, in accordance with the upper three bits  $d_5$ ,  $d_4$ , and  $d_3$  of the video data. More specifically, the video data  $d_5$ ,  $d_4$ , and  $d_3$  and the inverted signals which are respectively obtained by inverting the video data  $d_5$ ,  $d_4$ , and  $d_3$  by inverter circuits **INV<sub>4</sub>-INV<sub>6</sub>** are input to AND circuits **DG<sub>0</sub>-DG<sub>7</sub>** in such combinations which constitute 0-7 in the binary notation. As the outputs of the AND circuits **DG<sub>0</sub>-DG<sub>7</sub>**, the gray-scale voltage specifying signals [0], [8], [16], [24], [32], [40], [48], and [56] are obtained.

[0073] The logical circuit **95** shown in Figure **10** selectively outputs the control signals  $S_0$ - $S_{64}$ , in accordance with the gray-scale voltage specifying signals [0], [8], [16], [24], [32], [40], [48], and [56], the oscillating signal  $T$ , and the inverted oscillating signal  $\bar{T}$ . More specifically, the gray-scale voltage specifying signals [0], [8], [16], [24], [32], [40], [48], and [56], and the oscillating signal  $T$  are input into AND circuits **EG<sub>0</sub>, EG<sub>2</sub>, EG<sub>4</sub>, EG<sub>6</sub>, EG<sub>8</sub>, EG<sub>10</sub>, EG<sub>12</sub>, and EG<sub>14</sub>**, respectively. The gray-scale voltage specifying signals [0], [8], [16], [24], [32], [40], [48], and [56] and the inverted oscillating signal  $\bar{T}$  are input into AND circuits **EG<sub>1</sub>, EG<sub>3</sub>, EG<sub>5</sub>, EG<sub>7</sub>, EG<sub>9</sub>, EG<sub>11</sub>, EG<sub>13</sub>, and EG<sub>15</sub>**, respectively. The outputs of the AND circuits **EG<sub>1</sub>** and **EG<sub>2</sub>** are coupled to the inputs of an OR circuit **FG<sub>1</sub>**, respectively. The outputs of the AND circuits **EG<sub>3</sub>** and **EG<sub>4</sub>** are coupled to the inputs of an OR circuit **FG<sub>2</sub>**, respectively. The outputs of the AND circuits **EG<sub>5</sub>** and **EG<sub>6</sub>** are coupled to an OR circuit **FG<sub>3</sub>**, respectively. The outputs of the AND circuits **EG<sub>7</sub>** and **EG<sub>8</sub>** are coupled to the inputs of an OR circuit **FG<sub>4</sub>**, respectively. The outputs of the AND circuits **EG<sub>9</sub>** and **EG<sub>10</sub>** are coupled to the inputs of an OR circuit **FG<sub>5</sub>**, respectively. The outputs of the AND circuits **EG<sub>11</sub>** and **EG<sub>12</sub>** are coupled to the inputs of an OR circuit **FG<sub>6</sub>**, respectively. The outputs of the AND circuits **EG<sub>13</sub>** and **EG<sub>14</sub>** are coupled to the inputs of an OR circuit **FG<sub>7</sub>**, respectively. As the outputs of the AND circuit **EG<sub>0</sub>**, the OR circuits **FG<sub>1</sub>-FG<sub>7</sub>**, and the AND circuit **EG<sub>15</sub>**, the control signals  $S_0$ ,  $S_8$ ,  $S_{16}$ ,  $S_{24}$ ,  $S_{32}$ ,  $S_{40}$ ,  $S_{48}$ ,  $S_{56}$ , and  $S_{64}$  are obtained.

[0074] The control signals  $S_0$ ,  $S_8$ ,  $S_{16}$ ,  $S_{24}$ ,  $S_{32}$ ,  $S_{40}$ ,  $S_{48}$ ,  $S_{56}$ , and  $S_{64}$  are supplied to the corresponding analog switches **ASW<sub>0</sub>-ASW<sub>8</sub>**. Each of the control signals  $S_0$ ,  $S_8$ ,  $S_{16}$ ,  $S_{24}$ ,  $S_{32}$ ,  $S_{40}$ ,  $S_{48}$ ,  $S_{56}$ , and  $S_{64}$  has either a high-level value or a low-level value. For example, if the control signal is at a high level, the corresponding analog switch is controlled to be in the ON-state. If the control signal is at a low level, the corresponding analog switch is controlled to be in the OFF-state. Alternatively, the relationship between the level of the control signal and the ON/OFF state of the analog signal can be set in a reverse manner.

[0075] As described above, in the case where video data consists of a plurality of bits, a waveform of an oscillating voltage is specified in accordance with video data consisting of at least one bit selected from the plurality of bits. Then, in accordance with video data consisting of bits other than the above selected bit(s), a pair of gray-scale voltages are specified from a plurality of gray-scale voltages. As a result, a voltage signal of an appropriate level can be output for every value of video data. The oscillating voltage is used for realizing a plurality of interpolated gray-scale voltages between the specified pair of gray-scale voltages which are specified from among the plurality of gray-scale voltages.

[0076] In the case where the value of the video data is a multiple of 8, only one of the plurality of gray-scale voltages may be output. In such a case, the duty ratio  $n:m$  of the oscillating signal or the control signal is interpreted to be  $k:0$  or  $0:k$  ( $k$  is a natural number).

[0077] Alternatively, regardless of whether the value of the video data is a multiple of 8 or not, the specified pair of gray-scale voltages among the plurality of gray-scale voltages may be alternately output.

[0078] As described above, the selection control circuit **SCOL** according to the invention constructed of the logical circuits **70**, **80**, **90**, and **95** shown in Figures **7** through **10** has a simplified construction as compared with the conventional selection control circuit **SCOL** shown in Figure **12** which is constructed of the logical circuits shown in Figures **14** and **15**. According to the invention, it is possible to display an image with multiple gray scales, such as 64 gray scales, by using a driving circuit having a more simplified construction. For example, in order to realize a display image with 64 gray scales, only 9 kinds of gray-scale voltages are required.

[0079] The actual data driver requires selection control circuits **SCOL** the number of which is equal to the number of data lines. Thus, the circuit scale of the selection control circuits **SCOL** largely affects the chip size of an integrated circuit (LSI) on which a data driver is installed. According to the invention, it is possible to significantly reduce the size of the integrated circuit including the selection control circuits **SCOL**. As a result, the production cost of the integrated circuit can be reduced. In cases where the number of bits of video data is increased in order to realize an image with a larger number of gray scales, such miniaturization of the circuit scale of the data driver is of great use. Accordingly, it is possible to make further progress in the size and cost reduction of the integrated circuit.

[0080] According to the invention, it is possible to obtain one or more interpolated voltages from voltages supplied from given voltage sources, whereby the number of voltage sources can be greatly decreased as compared with a conventional driving circuit which requires a large number of voltage sources. If the voltage sources are provided from the outside of the driving circuit, the number of input terminals of the driving circuit can be reduced. If the driving circuit is constructed as an LSI, the number of input terminals of the LSI can be reduced. According to the invention, it is possible to realize a driving LSI for displaying an image with multiple gray scales which could not be realized by the prior art example because of the increase in the number of terminals. In the present invention, the following effects can be attained: (1) the production cost of a display apparatus and a driving circuit are largely reduced; (2) a driving circuit for multiple gray scales which could not be practically produced due to the chip size or the LSI installation can be readily produced; and (3) the power consumption is decreased because a large number of voltage sources are not required.

[0081] Various other modifications will be apparent to and can be readily made by those skilled in the art without departing from the scope of this invention. Accordingly, it is not intended that the scope of the invention be limited to the description as set forth herein, but rather by the appended claims.

**Claims**

1. A driving circuit for driving a display apparatus, the display apparatus including pixels and data lines ( $S_{(1)} \dots S_{(n)}$ ) for applying voltages to said pixels and displaying, in use, an image with multiple grey scales in accordance with video data consisting of a plurality of bits, said driving circuit comprising:

oscillating voltage selecting means for selecting one of a plurality of oscillating signals ( $t_0 \dots t_7$ ) oscillating between first and second predetermined levels and having respective duty ratios which are different from each other in accordance with video data consisting of bits ( $d_2, d_1, d_0$ ) selected from said plurality of bits, and for outputting said selected oscillating signal (T) and an inverted oscillating signal ( $\bar{T}$ ) which is obtained by inverting said selected oscillating signal (T);

grey-scale voltage selecting means for producing grey-scale voltage selecting signals which select a first grey-scale voltage and a second grey-scale voltage from a plurality of grey-scale voltages ( $V_0, V_8, V_{16}, V_{24}, V_{32}, V_{40}, V_{48}, V_{56}, V_{64}$ ) supplied by a grey-scale voltage supply means, in accordance with video data consisting of bits ( $d_5, d_4, d_3$ ) other than said selected bits of said plurality of bits; and

output means for outputting said first grey-scale voltage and said second grey-scale voltage selected by said grey-scale voltage selecting means to said data lines, in accordance with said oscillating signal (T) and said inverted oscillating signal ( $\bar{T}$ ), the output means outputting the first grey scale voltage when the oscillating signal (T) is at said first predetermined level and the second selected grey scale voltage when the inverted oscillating signal ( $\bar{T}$ ) is at said first predetermined level.

2. A driving circuit according to claim 1, wherein said first grey-scale voltage and said second grey-scale voltage are adjacent ones of said plurality of grey-scale voltages.

3. A driving circuit according to claim 1 or 2, wherein said plurality of oscillating signals include oscillating signals having duty ratios of 8:0, 7:1, 6:2, 5:3, 4:4, 3:5, 2:6, and 1:7, respectively.

4. A driving circuit as claimed in claim 1, 2 or 3 wherein the output means comprises

(a) control signal output means for outputting a first control signal which oscillates at substantially the same duty ratio as that of said oscillating signal (T) to one of said switching means which is supplied with said first grey-scale voltage selected by said grey-scale voltage selecting signals and for outputting a second control signal which oscillates at substantially the same duty ratio as that of said inverted oscillating signal ( $\bar{T}$ ) to one of said switching means which is supplied with said second grey-scale voltage selected by said grey-scale voltage selecting signals; and

(b) a plurality of switching means, each of said plurality of switching means being supplied with a corresponding one of said plurality of control signals and a corresponding one of the plurality of grey-scale voltages, said grey-scale voltage supplied to said switching means being output to said data lines via said switching means in accordance with said control signal.

5. A driving circuit according to claim 4, wherein said switching means is an analogue switch.

**Patentansprüche**

1. Ansteuerschaltung zum Ansteuern einer Anzeigevorrichtung, die Pixel und Datenleitungen ( $S_{(1)} \dots S_{(n)}$ ) aufweist, um Spannungen an die Pixel anzulegen und um im Gebrauch ein Bild mit mehreren Graustufen entsprechend Videodaten anzuzeigen, die aus mehreren Bits bestehen, wobei die Ansteuerschaltung Folgendes aufweist:
  - eine Oszillierspannung-Auswähleinrichtung zum Auswählen eines von mehreren schwingenden Signalen ( $t_0 \dots t_7$ ), die zwischen einem ersten und einem zweiten vorbestimmten Pegel schwingen und jeweilige Tastverhältnisse aufweisen, die entsprechend aus Bits ( $d_2, d_1, d_0$ ), die aus den mehreren Bits ausgewählt sind, bestehenden Videodaten voneinander verschieden sind, und zum Ausgeben des ausgewählten schwingenden Signals (T) und eines invertierten schwingenden Signals ( $\bar{T}$ ), das durch Invertieren des ausgewählten schwingenden Signals (T) erhalten wird;
  - eine Graustufenspannung-Auswähleinrichtung zum Erzeugen von Graustufenspannung-Auswählsignalen, die aus einer Anzahl von durch eine Graustufenspannung-Liefereinrichtung gelieferten Graustufenspannungen ( $V_0, V_8, V_{16}, V_{24}, V_{32}, V_{40}, V_{48}, V_{56}, V_{64}$ ) eine erste Graustufenspannung und eine zweite Graustufenspannung entsprechend Videodaten auswählt, die aus anderen Bits ( $d_5, d_4, d_3$ ) als den ausgewählten Bits der mehreren Bits bestehen; und
  - eine Ausgabereinrichtung zum Ausgeben der durch die Graustufenspannung-Auswähleinrichtung ausgewählten ersten Graustufenspannung und zweiten Graustufenspannung an die Datenleitungen entsprechend dem schwingenden Signal (T) und dem invertierten schwingenden Signal ( $\bar{T}$ ), wobei die Ausgabereinrichtung die erste Graustufenspannung ausgibt, wenn sich das schwingende Signal (T) auf dem ersten vorbestimmten Pegel befindet, und sie die zweite ausgewählte Graustufenspannung ausgibt, wenn sich das invertierte schwingende Signal ( $\bar{T}$ ) auf dem ersten vorbestimmten Pegel befindet.
  
2. Ansteuerschaltung nach Anspruch 1, bei der die erste Graustufenspannung und die zweite Graustufenspannung unter der Anzahl von Graustufenspannungen benachbart sind.
  
3. Ansteuerschaltung nach Anspruch 1 oder 2, bei der die mehreren schwingenden Signale solche schwingenden Signale umfassen, die Tastverhältnisse 8:0, 7:2, 6:2, 5:3, 4:4, 3:5, 2:6 oder 1:7 aufweisen.
  
4. Ansteuerschaltung nach Anspruch 1, 2 oder 3, bei der die Ausgabereinrichtung Folgendes aufweist:
  - (a) eine Steuersignal-Ausgabereinrichtung zum Ausgeben eines ersten Steuersignals, das im Wesentlichen mit demselben Tastverhältnis wie das schwingende Signal (T) schwingt, an eine von Schalteinrichtungen, die mit der durch die Graustufenspannung-Auswählsignale ausgewählten ersten Graustufenspannung versorgt wird, und zum Ausgeben eines zweiten Steuersignals, das im Wesentlichen mit demselben Tastverhältnis wie das invertierte schwingende Signal ( $\bar{T}$ ) schwingt, an eine der Schalteinrichtungen, die mit der durch die Graustufenspannung-Auswählsignale ausgewählten zweiten Graustufenspannung versorgt wird; und
  - (b) eine Anzahl von Schalteinrichtungen, von denen jede mit einem entsprechenden der Anzahl von Steuersignalen und einer entsprechenden der Anzahl von Graustufenspannungen versorgt wird, wobei die an die Schalteinrichtung gelieferte Graustufenspannung über die Schalteinrichtung entsprechend dem Steuersignal an die Datenleitungen ausgegeben wird.
  
5. Ansteuerschaltung nach Anspruch 4, bei der die Schalteinrichtung ein Analogschalter ist.

**Revendications**

1. Circuit d'attaque pour attaquer un appareil d'affichage, l'appareil d'affichage comprenant des pixels et des lignes de données ( $S_{(1)} \dots S_{(n)}$ ) pour appliquer des tensions auxdits pixels et afficher, en service, une image à échelles de gris multiples conformément à des données vidéo se composant d'une multiplicité de bits, ledit circuit d'attaque comprenant:
  - des moyens de sélection de tension d'oscillation pour sélectionner un signal parmi une multiplicité de signaux oscillants ( $t_0 \dots t_7$ ) oscillant entre un premier et un second niveaux prédéterminés et présentant des rapports cycliques respectifs différents les uns des autres, conformément à des données vidéo se composant de bits ( $d_2, d_1, d_0$ ) sélectionnés parmi ladite multiplicité de bits, et pour délivrer en sortie ledit signal oscillant sélectionné (T) et un signal oscillant inversé ( $\bar{T}$ ) qui est obtenu en inversant ledit signal oscillant sélectionné (T);

des moyens de sélection de tension d'échelle de gris pour produire des signaux de sélection de tension d'échelle de gris qui sélectionnent une première tension d'échelle de gris et une seconde tension d'échelle de gris à partir d'une multiplicité de tensions d'échelle de gris ( $V_0, V_8, V_{16}, V_{24}, V_{32}, V_{40}, V_{48}, V_{56}, V_{64}$ ) fournies par des moyens d'alimentation en tension d'échelle de gris, conformément à des données vidéo se composant de bits ( $d_5, d_4, d_3$ ) autres que lesdits bits sélectionnés de ladite multiplicité de bits; et des moyens de sortie pour envoyer auxdites lignes de données ladite première tension d'échelle de gris et ladite seconde tension d'échelle de gris sélectionnées par lesdits moyens de sélection de tension d'échelle de gris, en fonction dudit signal oscillant (T) et dudit signal oscillant inversé ( $\bar{T}$ ), les moyens de sortie délivrant la première tension d'échelle de gris lorsque le signal oscillant (T) est audit premier niveau prédéterminé, et la seconde tension d'échelle de gris sélectionnée lorsque le signal oscillant inversé ( $\bar{T}$ ) est audit premier niveau prédéterminé.

2. Circuit d'attaque selon la revendication 1, dans lequel ladite première tension d'échelle de gris et ladite seconde tension d'échelle de gris sont des tensions adjacentes parmi ladite multiplicité de tensions d'échelle de gris.

3. Circuit d'attaque selon la revendication 1 ou la revendication 2, dans lequel ladite multiplicité de signaux oscillants comprend des signaux oscillants ayant, respectivement, des rapports cycliques égaux à 8:0, 7:1, 6:2, 5:3, 4:4, 3:5, 2:6 et 1:7.

4. Circuit d'attaque selon l'une des revendications 1, 2 et 3, dans lequel les moyens de sortie comprennent:

(a) des moyens de sortie de signal de commande pour envoyer un premier signal de commande, qui oscille suivant sensiblement le même rapport cyclique que celui dudit signal oscillant (T), à l'un desdits moyens de commutation qui reçoit ladite première tension d'échelle de gris sélectionnée par lesdits signaux de sélection de tension d'échelle de gris, et pour envoyer un second signal de commande, qui oscille suivant sensiblement le même rapport cyclique que celui dudit signal oscillant inversé ( $\bar{T}$ ), à l'un desdits moyens de commutation qui reçoit ladite seconde tension d'échelle de gris sélectionnée par lesdits signaux de sélection de tension d'échelle de gris; et

(b) une multiplicité de moyens de commutation, chaque moyen de ladite multiplicité de moyens de commutation recevant un signal correspondant parmi ladite multiplicité de signaux de commande et une tension correspondante parmi la multiplicité de tensions d'échelle de gris, ladite tension d'échelle de gris fournie auxdits moyens de commutation étant envoyée auxdites lignes de données par l'intermédiaire desdits moyens de commutation, conformément audit signal de commande.

5. Circuit d'attaque selon la revendication 4, dans lequel lesdits moyens de commutation sont des commutateurs analogiques.



Fig. 2

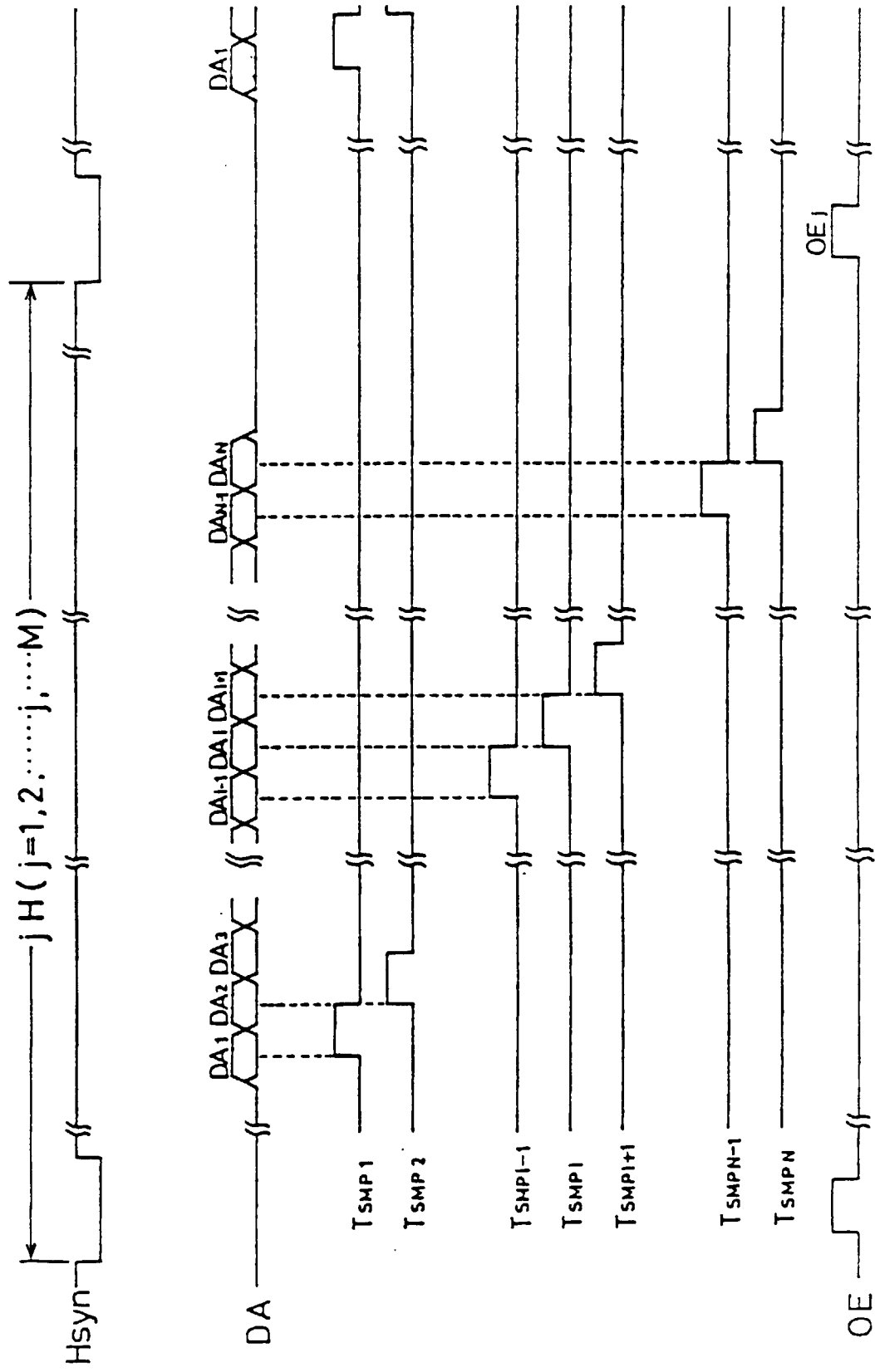


Fig. 3

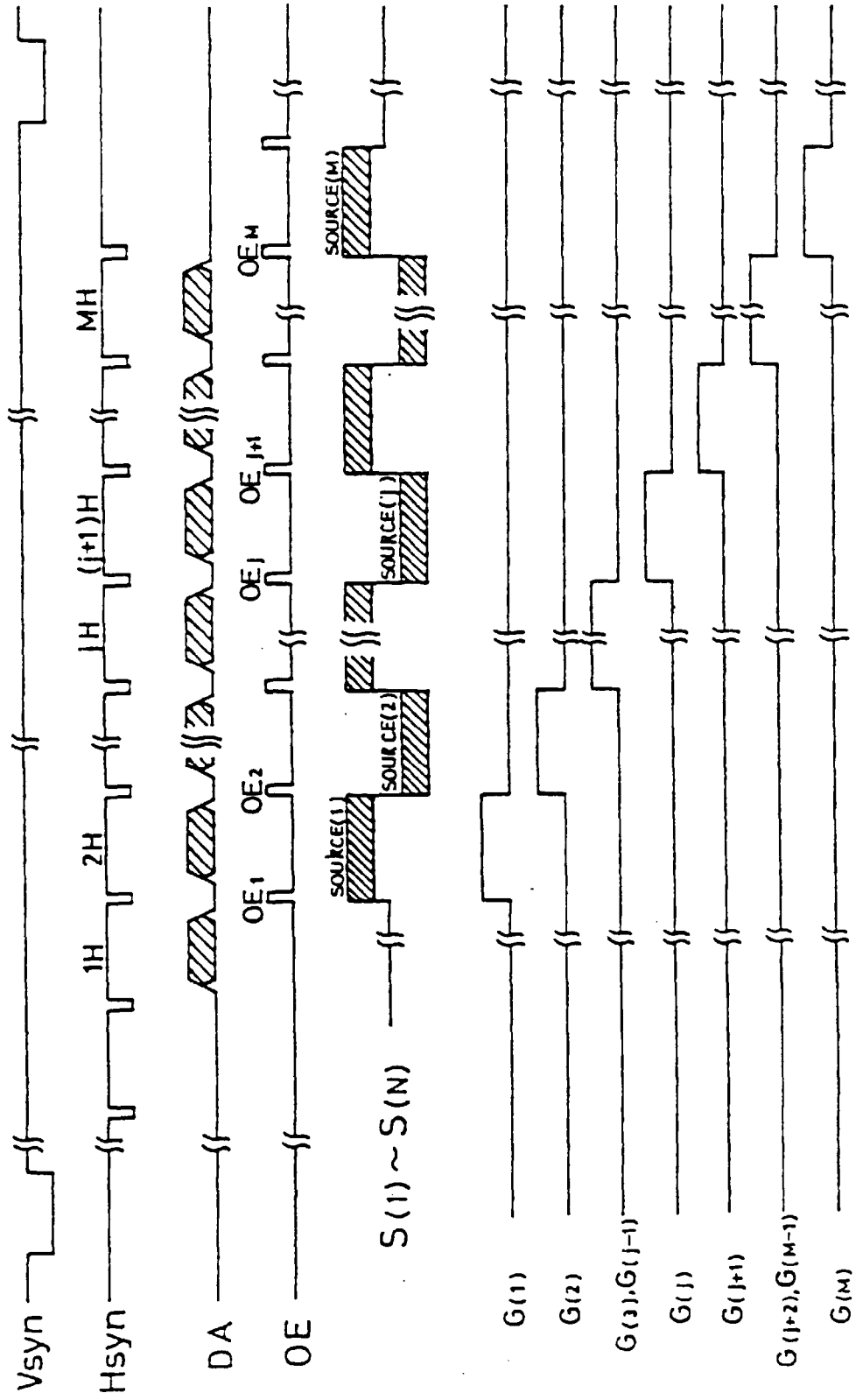


Fig. 4

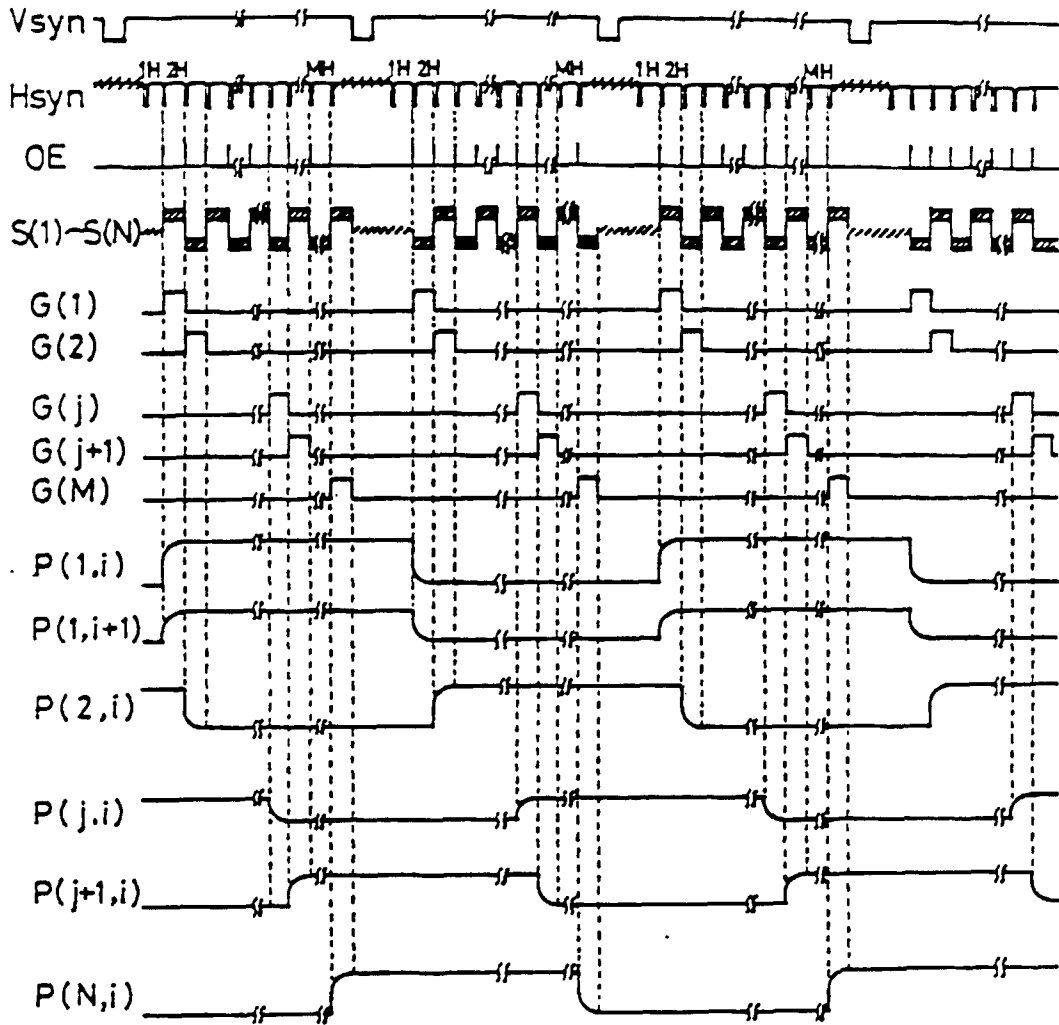


Fig.5

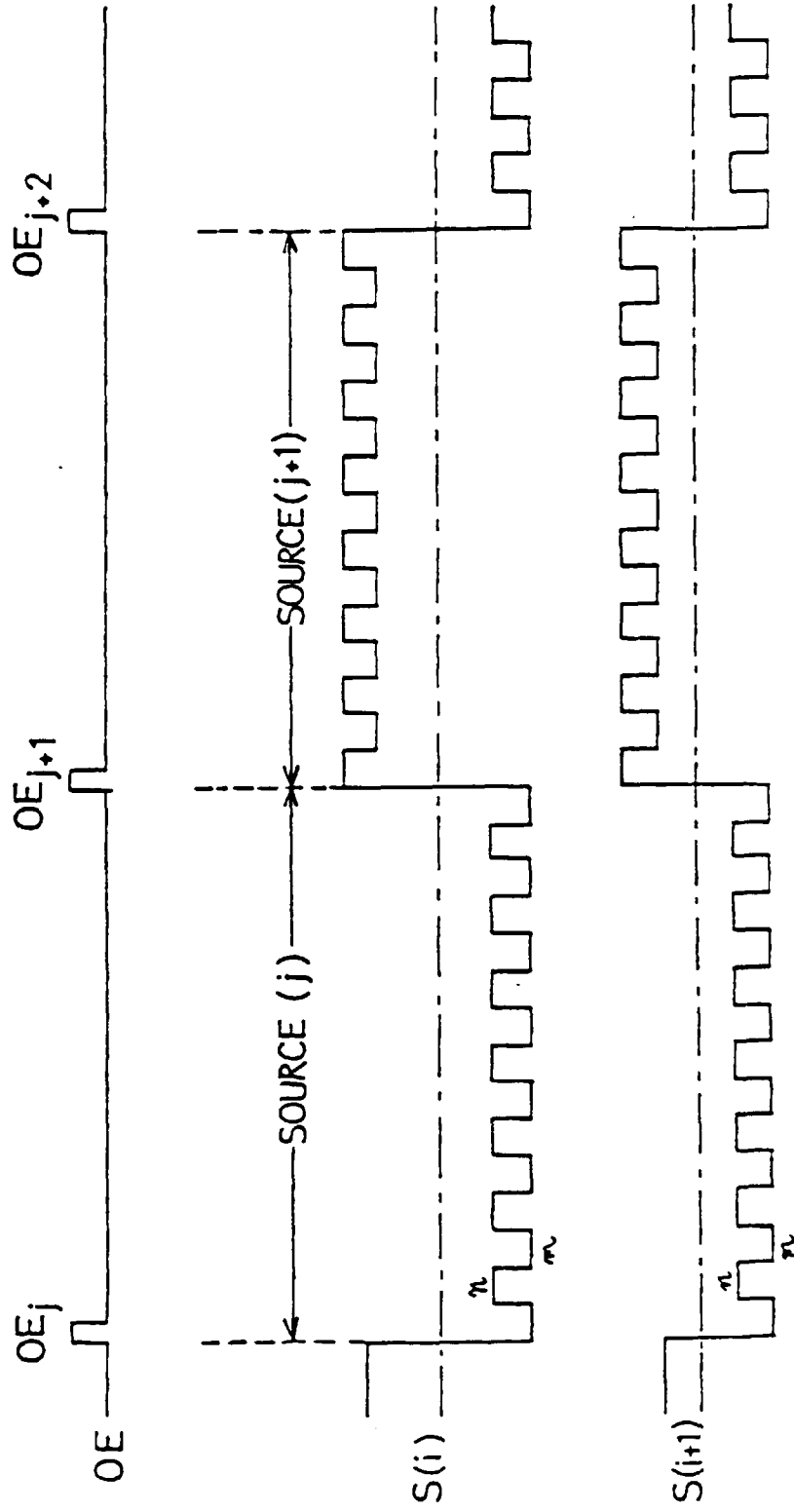


Fig.6

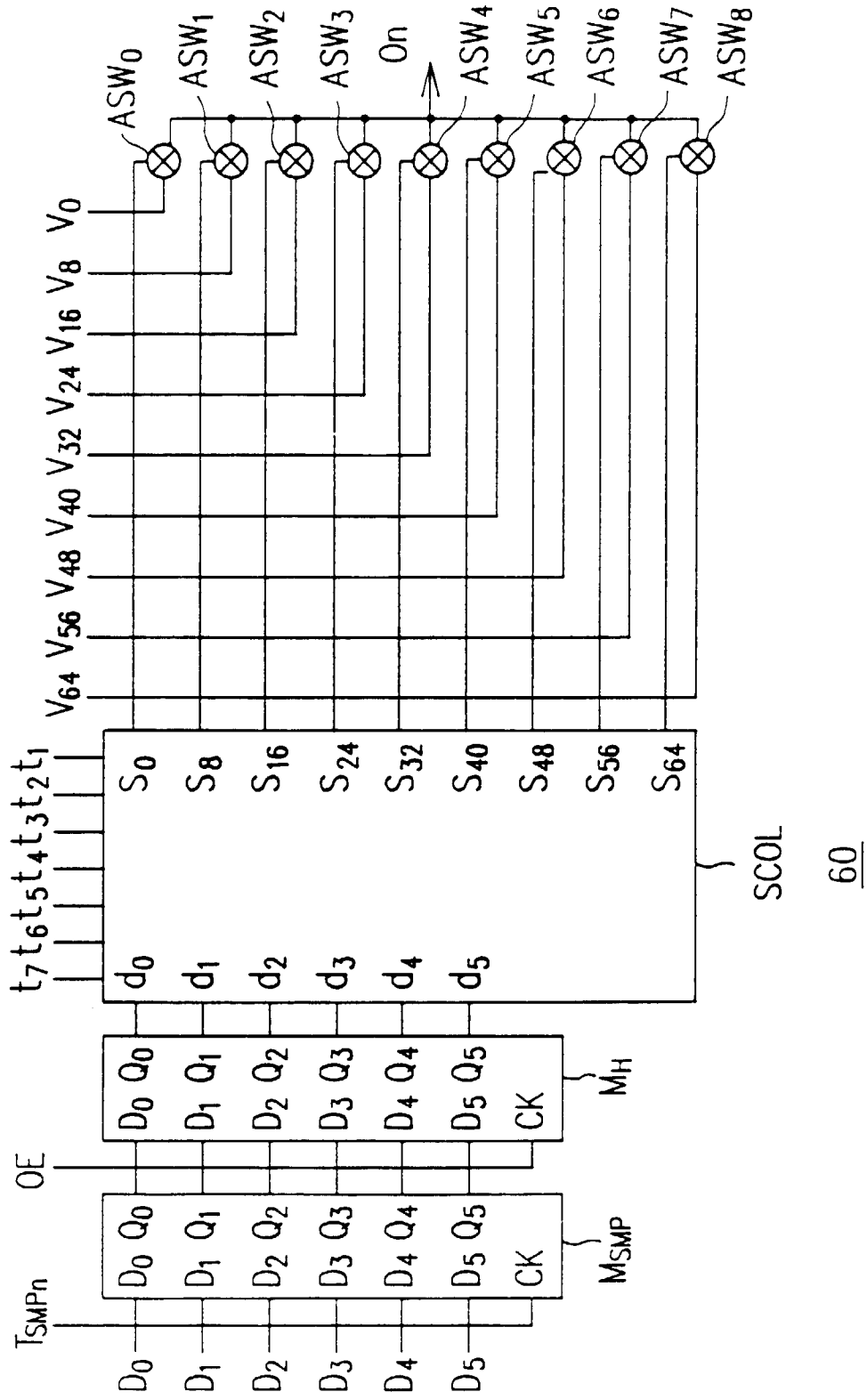


Fig.7

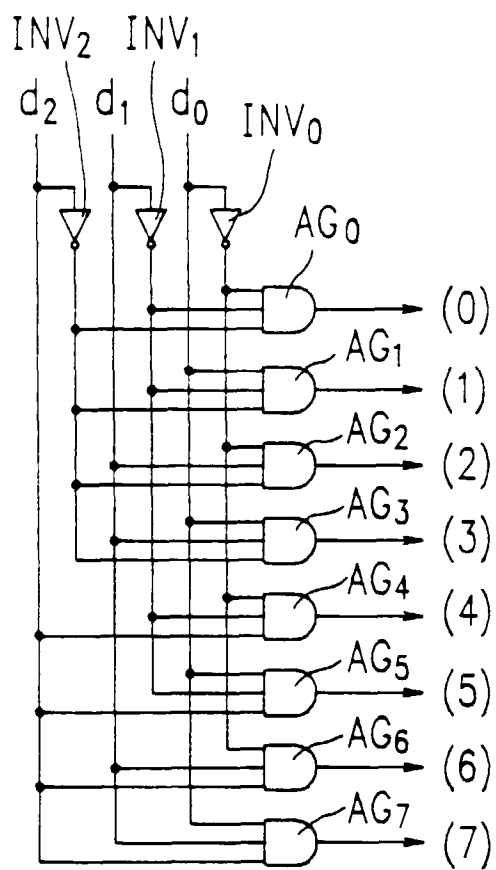
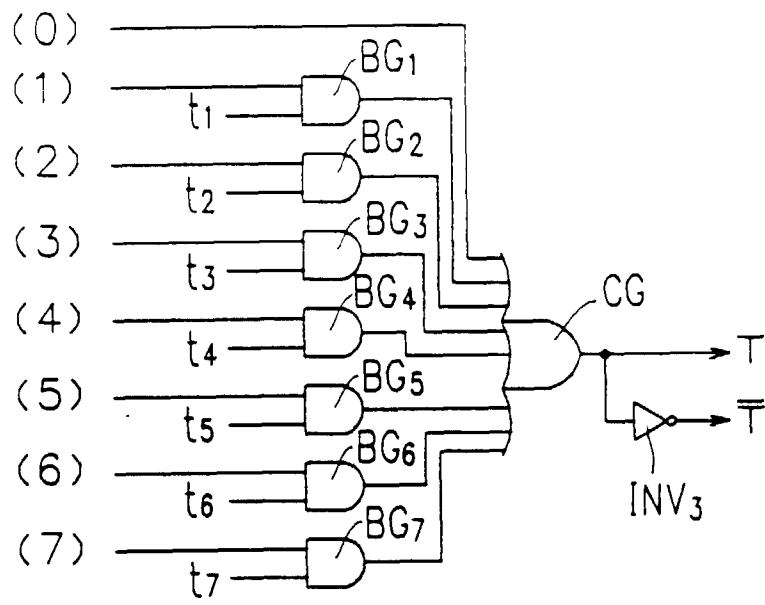
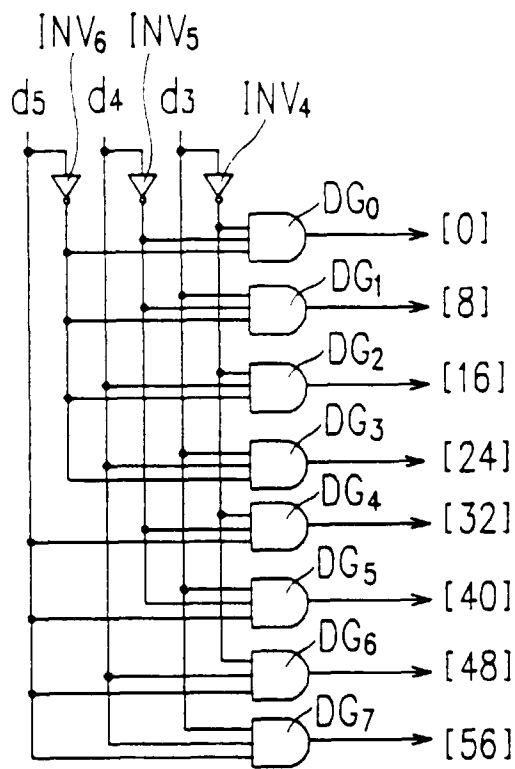


Fig.8



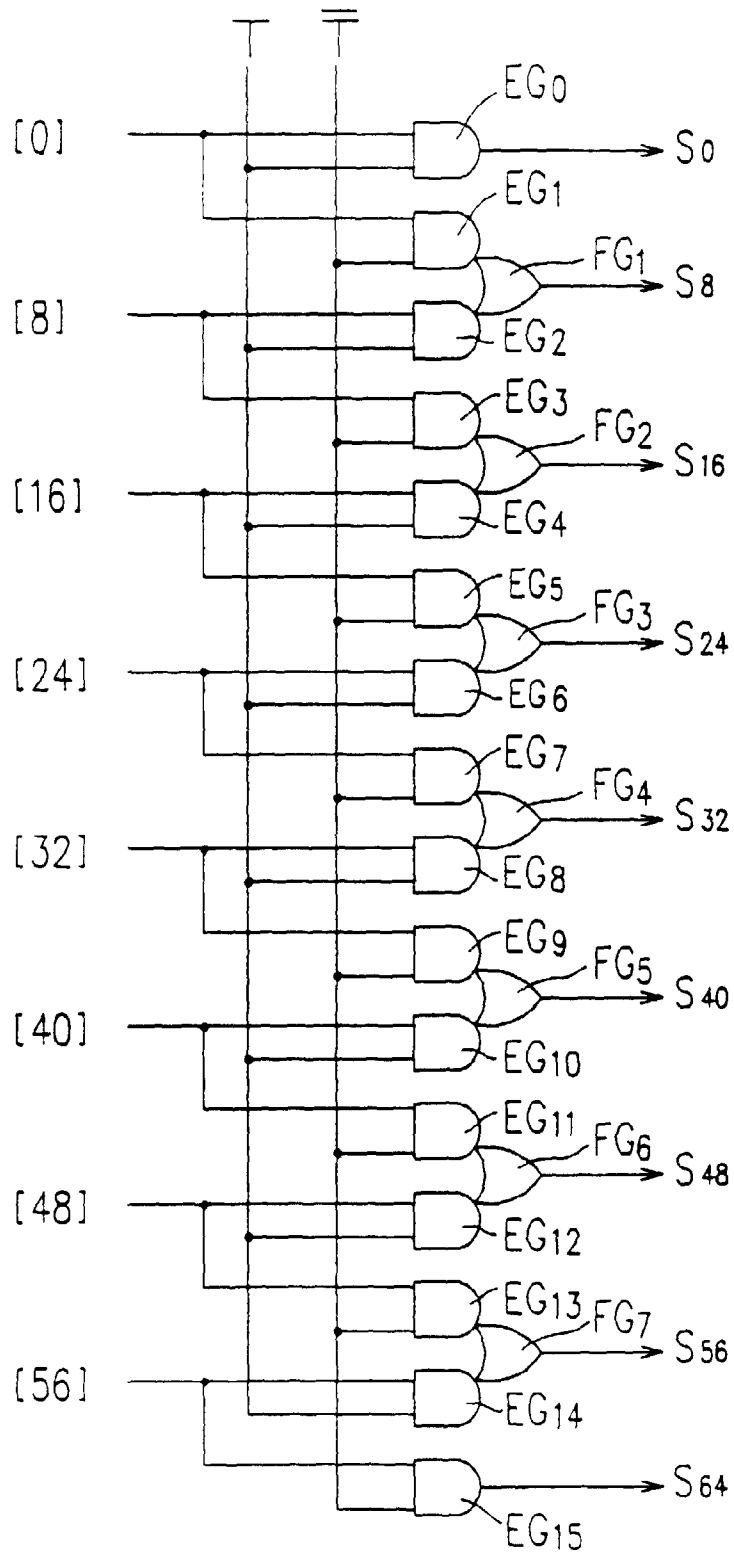
80

Fig.9



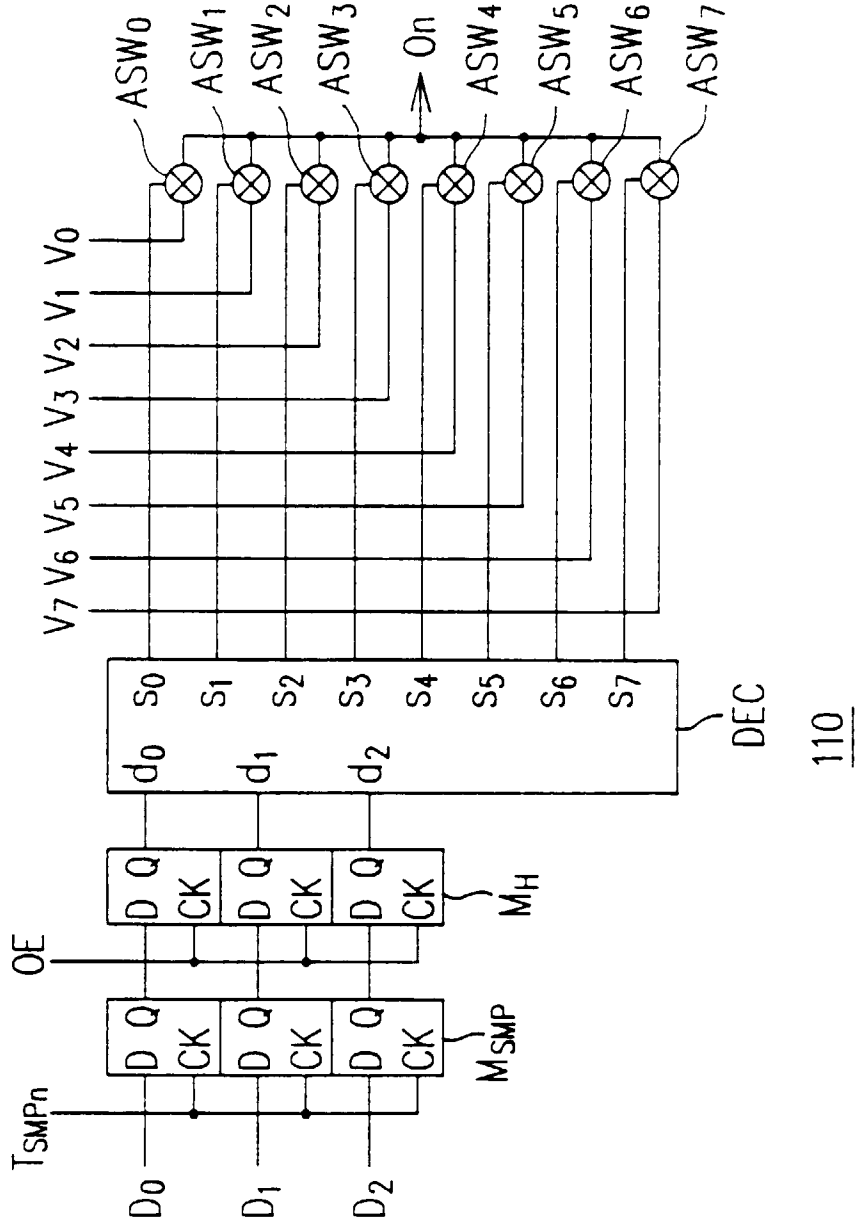
90

Fig.10



95

Fig.11



110

Prior Art

Fig.12

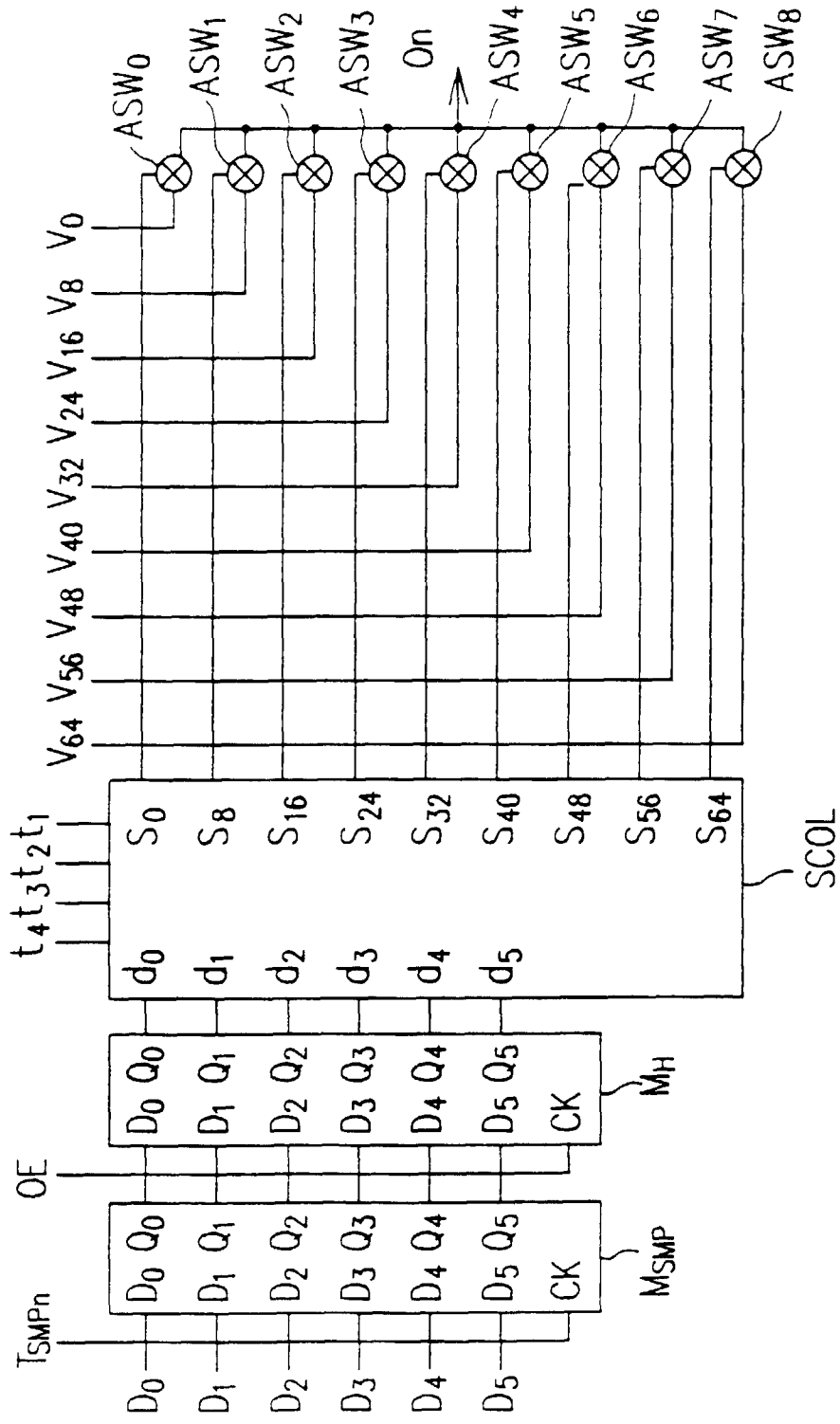


Fig.13

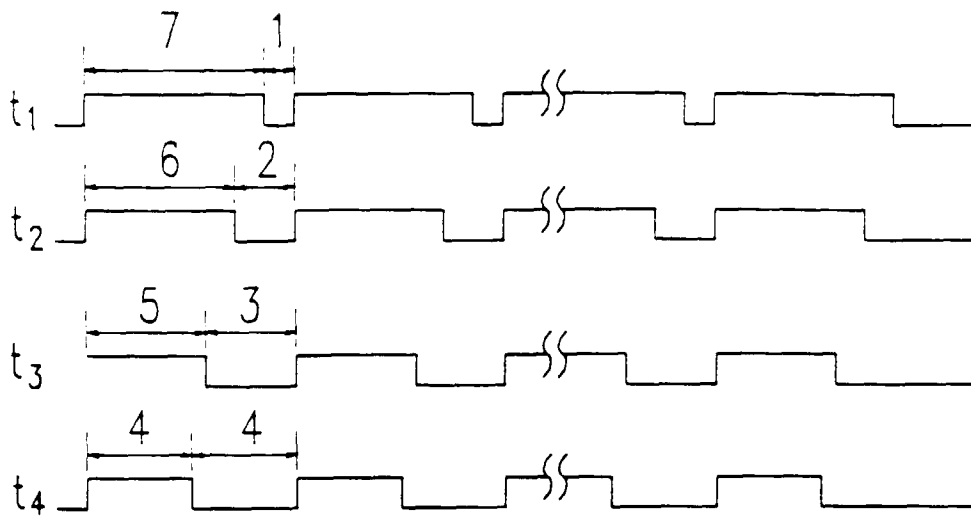


Fig.14

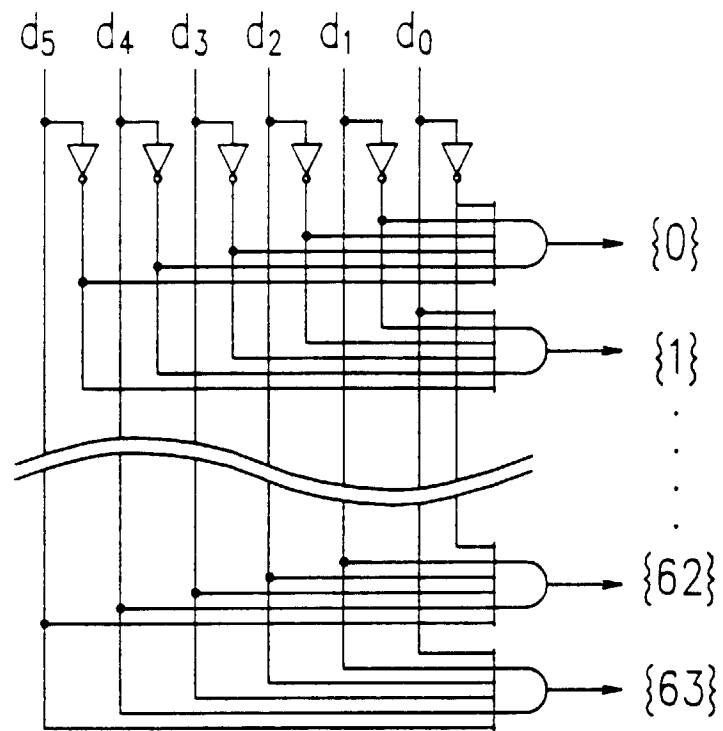


Fig.15

