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(71) Applicant : **CANON KABUSHIKI KAISHA**
30-2, 3-chome, Shimomaruko,
Ohta-ku
Tokyo (JP)

(72) Inventor : **Miyawaki, Mamoru, c/o Canon Kabushiki Kaisha**
30-2, 3-chome,
Shimomaruko,
Ohta-ku
Toyko (JP)
Inventor : **Ueno, Isamu, c/o Canon Kabushiki Kaisha**
30-2, 3-chome,
Shimomaruko,
Ohta-ku
Toyko (JP)

(74) Representative : **Beresford, Keith Denis Lewis et al**
BERESFORD & Co.
2-5 Warwick Court
High Holborn
London WC1R 5DJ (GB)

(54) Gain-controlled solid-state image pickup device.

(57) Photo-electric Conversion Apparatus A photo-electric conversion apparatus having a plurality of photo-electric conversion elements is provided with an amplifier which can externally control a gain thereof, at an output terminal of each of the photo-electric conversion elements.

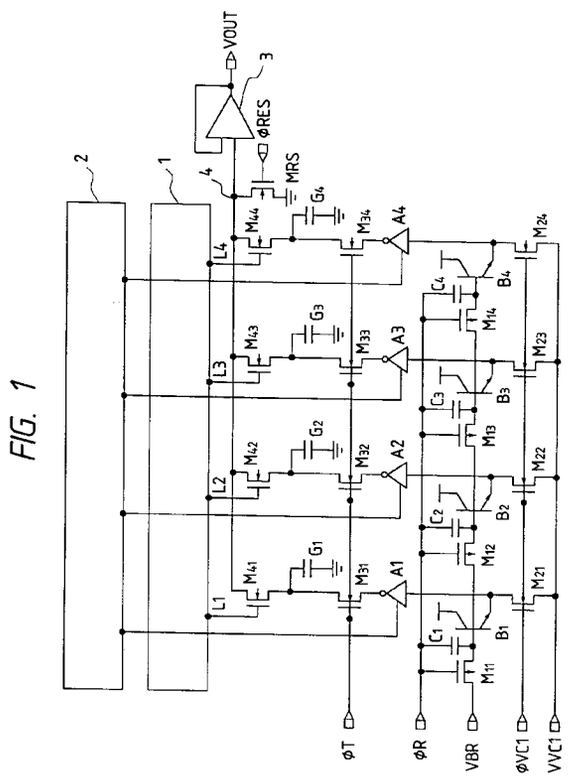


FIG. 1

EP 0 626 784 A1

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a photo-electric conversion apparatus e.g. used in an AE (Auto-Exposure) sensor or AF (Auto-Focus) sensor of a copying machine, a facsimile machine, a video camera recorder and a camera.

Related Background Art

As an electronics technology has highly developed recently, high image fineness and high image quality have rapidly been realized in a field of a solid state image pick-up device used as a photo-electric conversion apparatus. An output of the solid state image pick-up device is rarely used as it is but it is processed in several stages before it is formed into a TV signal.

Accordingly, when the number of pixels is increased to attain high fineness, a huge volume of operation and processing are required in the signal processing and the high image quality may be restricted by the signal processing.

SUMMARY OF THE INVENTION

In one aspect the present invention provides a solid state image pick-up device which produces signals multiplied by coefficients in order to built a signal processing function in the solid state image pick-up device.

An embodiment of the present invention provides a photo-electric conversion apparatus comprising a plurality of photo-electric conversion elements by providing an externally gain controllable amplifier at an output terminal of each photo-electric conversion element, so that signal processing for multiplying a desired coefficient to each signal is well attained.

Other aspects and advantages of the present invention will be apparent from the claims, and from the following description of non-limiting embodiments and the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 shows a circuit configuration of a photo-electric conversion apparatus in accordance with an embodiment 1 of the present invention,

Fig. 2 shows a timing chart for illustrating an operation of the embodiment 1 of the photo-electric conversion apparatus,

Fig. 3 shows a circuit diagram of an amplifier used in the present invention,

Fig. 4 shows a graph of a characteristic of the amplifier,

Fig. 5 shows a circuit configuration of a photo-electric conversion apparatus in accordance with an embodiment 2 of the present invention,

Fig. 6 shows a circuit configuration of a photo-electric conversion apparatus in accordance with an embodiment 3 of the present invention,

Fig. 7 shows a circuit configuration of a photo-electric conversion apparatus in accordance with an embodiment 4 of the present invention, and

Fig. 8 shows a circuit configuration of a photo-electric conversion apparatus in accordance with an embodiment 5 of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 1 shows a first embodiment of the present invention. In the present embodiment, bipolar photo-electric conversion elements are one-dimensionally arranged as photo-electric conversion elements, and base regions thereof are interconnected through PMOS transistors M_{11} - M_{14}.

Amplifiers A1 - A4 are independently connected to respective emitter output lines of the photo-electric elements.

An operation of the present embodiment is explained by referring to a timing chart of Fig. 2.

At a time t_1, a pulse of a low level is applied to ϕ_R so that the PMOS transistors M_{11} - M_{14} are turned on and the bases of the bipolar transistors B_1 - B_4 are connected in common and reset to V_{BR}. Thereafter, ϕ_R rises to a middle level so that the PMOS transistors M_{11} - M_{14} are turned off and the reset operation is terminated.

At a time t_2, a pulse ϕ_{VC1} rises and the NMOS transistors M_{21} - M_{24} are turned on so that emitter terminals of all bipolar transistors B_1 - B_4 are reset to a voltage V_{VC}, and at a time t_3, a pulse ϕ_R rises to a high level so that the base potentials of the bipolar transistors B_1 - B_4 are brought up through capacitors C_1 - C_4 and the base-emitter junctions is forwardly biased. Thus, the bipolar transistors simultaneously operate in an emitter follower mode and hole on the bases are recombined and the base potentials are settled around $V_{VC} + V_{BE}$ (Transient reset operation). When the transient reset operation is terminated, at a time t_4, the pulse ϕ_R falls to the middle level so that the base potentials of the respective bipolar transistors fall through the capacitors C_1 - C_4 and the base-emitter junction is reversely biased. From this state, an accumulation operation of the photo-carriers starts.

After a predetermined accumulation time has elapsed, at the time t_5, the pulses ϕ_T and ϕ_R rise to the high level so that the NMOS transistors M_{31} - M_{34} are turned on and the base potentials of the bipolar transistors B_1 - B_4 are brought up to forwardly bias the base-emitter junction. Thus, the photo-carriers accumulated on the bases are outputted from the emitter

terminals. By applying predetermined voltages from a power supply 2 to the control terminals of the amplifiers A_1 - A_4, the respective amplifiers may have desired gains.

The outputs of the amplifiers A_1 - A_4 are read to C_{T1} - C_{T4}, respectively, and at a time t_6, the pulse ϕ_T falls to the low level so that the NMOS transistors M_{31} - M_{34} are turned off and the voltages on the respective capacitors C_{T1} - C_{T4} are maintained. At the time t_6, the pulses ϕ_T and ϕ_R rise to the high level simultaneously. However, it is preferable that the pulse ϕ_T raises to the high level earlier than the pulse ϕ_R.

Thereafter, at a time t_7, a high level pulse is applied to ϕ_{RES} so that the NMOS transistor M_{RS} is turned on, and after the output line 4 is reset, the scan circuit 1 is operated to transfer the signals to the output terminal V_{OUT} through the output buffer 3 starting from the signal on C_{T1}.

A preferred embodiment of the amplifiers A1 - A4 and a DC characteristic thereof are shown in Figs. 3 and 4.

Fig. 3 shows an inverting amplifier using an NPN transistor and a gain thereof is controlled by a gate voltage of an NMOS transistor connected to an emitter terminal.

Calculation of a DC characteristic of the inverting amplifier is shown in Fig. 4.

In Fig. 4, an abscissa represents an input voltage V_{IN} and an ordinate represents an output voltage V_{OUT}, and a graph is shown with the gain control voltage V_C being used as a parameter. As seen from Fig. 4, the larger the V_C is, the larger is the gain. Thus, it is suitable for the present invention because of its smaller circuit scale. Needless to say, other type of amplifier may be used.

Fig. 5 shows a second embodiment of the present invention. The present embodiment is an improvement over the first embodiment in that the power supply 2 is omitted and the gain control voltages of the amplifiers A1 - A4 are serially applied from a terminal V-GAIN.

In an operation, the scan circuit 1 is operated during the accumulation period and the pulse ϕ_{WR} rises to the high level, the NMOS transistor M51 is turned on so that the gain control voltage of the amplifier A1 is written from the terminal V-GAIN. Thereafter, the pulse L1 is rendered to the low level and M51 is turned off to hold the written voltage. This operation is sequentially carried out for the amplifiers A1 - A4, and thereafter the pulse ϕ_R rendered to the high level so that the respective photo-electric conversion elements carry out the read operation and the voltages multiplied by the factors of the respective gains are read at C_{T1} - C_{T4}.

Other operations may be carried out in the same manner as those of Fig. 1.

Accordingly, the space is significantly saved compared to case where the power supply is provided for each amplifier.

In the above explanation of the operation, the control voltages of the amplifiers A1 - A4 are written during the accumulation period although they may be written in other period, for example during the sequential transfer of the charges of C_{T1} - C_{T4}. In this case, the gain control voltages written in the amplifiers A1 - A4 are used in the next photo-electric conversion operation.

Fig. 6 shows a third embodiment of the present invention. In the present embodiment, the second embodiment is developed to a two-dimensional photo-electric conversion apparatus. A vertical scan circuit 5 is provided to conduct serial resetting and signal reading of the photo-electric conversion elements row by row. The basic operation is identical to that of the second embodiment.

Fig. 7 shows a fourth embodiment of the present invention. In the first to third embodiments, the photo-electric conversion apparatus use the amplifier elements by the bipolar transistors having the base-collector junctions used as the photo-diodes. In the present embodiment, MOS's are used. The like elements to those of the previous embodiments are designated by the like numerals and the explanation thereof is omitted. In a sense amplifier 11, a photo-diode is connected to a gate of an MOS, and in a variable gain amplifier 10, a resistor of an MOS amplifier is a variable resistor which comprises a double structure of MOS gate switch a lower gate 12 being floating and one of upper gates 13 being connected to a power supply, and a voltage pulse is applied to the other upper gate 14.

The potential of the floating gate changes with an amplitude of the voltage pulse so that the MOS's of the amplifier 10 function as variable resistors. In the present embodiment, the photo signal generated by the photo-diode is converted by the factor of gain of the amplifier determined by the variable resistor, and the modulated signal is sequentially read by a shift register via a read capacitor.

While Fig. 7 shows the one-dimensional sensor, it should be understood that the present invention is not limited to the one-dimensional sensor but it may be applied to a two-dimensional sensor.

A fifth embodiment of the present invention is shown in Fig. 8. S_{ij} (ij = 1 - 4) comprises a base isolation PMOS 12, a base potential control capacitor 13 and a bipolar transistor 15.

Cells S_{11} and S_{21} output to a vertical line 16, and cells S_{12} and S_{22} output to a vertical line 17. Line selection is conducted by pulses ϕ_{PR1} and ϕ_{PR2}.

First, a high pulse is applied to ϕ_{PR1} so that the cells S_{11} and S_{12} are selected, and the respective outputs are simultaneously read to the gates of the amplifiers a_{ij} (i,j = 1,2).

The gains of the amplifiers are adjusted by the vertically arranged power supplies through wires 18,

19, 20 and 21, and the pulse ϕ_{PT1} is rendered to the high level to read the photo output of the S_{11} multiplied by the gain of the amplifier a_{11} to the capacitor 22, the photo output of the S_{12} multiplied by the gain of the amplifier a_{12} to the capacitor 23, the photo output of the S_{11} multiplied by the gain of the amplifier a_{21} to the capacitor 24, and the photo output of the S_{21} multiplied by the gain of the amplifier a_{22} to the capacitor 25.

The pulse ϕ_{PR1} is then rendered to the down level and the pulse ϕ_{PR2} is rendered to the high level so that the cells S_{21} and S_{22} are selected and they are read to the gates of the amplifiers a_{ij} (ij = 1 - 2').

The pulse ϕ_{PT2} is rendered to the high level to read the photo output of the cell S_{11} multiplied by the gain of the amplifier a_{11} to the capacitor 26, the photo output of the cell S_{12} multiplied by the gain of the amplifier a_{12} to the capacitor 27, the photo output of the cell S_{21} multiplied by the gain of the amplifier a_{21} to the capacitor 28, and the photo output of the cell S_{22} multiplied by the gain of the amplifier a_{22} to the capacitor 29.

The signals read to the capacitors 22, 23, 26 and 27 are summed through the capacitors 30, 31, 32 and 33 and outputted from the amplifier 38, and the signals read to the capacitors 24, 25, 28 and 29 are summed through the capacitors 34, 35, 36 and 37 and outputted from the amplifier 39.

The outputs of the amplifiers 38 and 39 are differentiated by a differential amplifier 40. Accordingly, the gains may include positive gains and negative gains so that Fourier transform output of the image can be read at a high speed.

Using the above, and other analogous embodiments, the following technological advantages (1)-(4) can be attained since the sensor can output therefrom a signal on which various image processings, for example, convolution, edge output, Laplace transform, Fourier transform and wavelet transform, have been performed.

(1) A photo-electric conversion apparatus can be form on one chip, so that the cost of production can be reduced.

(2) High-speed processing can be attained since processing can be done in a parallel operation on image data itself rather than on the serial output of the sensor.

(3) A plurality of processings can be attained by one chip.

(4) Image recognization and image discrimination can be attained functionally.

Other types of photosensor element may be used, such as non-bipolar phototransistors, and the bipolar type phototransistor may be used without the base control capacitors C1, C2, C3, C4 (in which case accumulation and read-out from the phototransistor may be simultaneous).

Claims

1. A photo-electric conversion apparatus comprising:
   a) a plurality of photo-electric conversion elements;
   b) a plurality of read channels for separately reading outputs of said photo-electric conversion elements;
   c) a plurality of gain controllable amplifiers provided one for each channel, and
   d) control means for controlling gains of said amplifiers.

2. A photo-electric conversion apparatus according to Claim 1 further comprising storage means for storing output signals of the photo-electric conversion elements through the amplifiers.

3. A photo-electric conversion apparatus according to Claim 2 wherein said storage means includes capacitors.

4. A photo-electric conversion apparatus according to Claim 2 further comprising read means for serially reading the signals of said storage means.

5. A photo-electric conversion apparatus according to Claim 4 wherein said read means is controlled by said control means.

6. A photo-electric conversion apparatus according to Claim 1, wherein each of said gain controllable amplifiers includes a transistor having a plurality of floating gate electrodes.

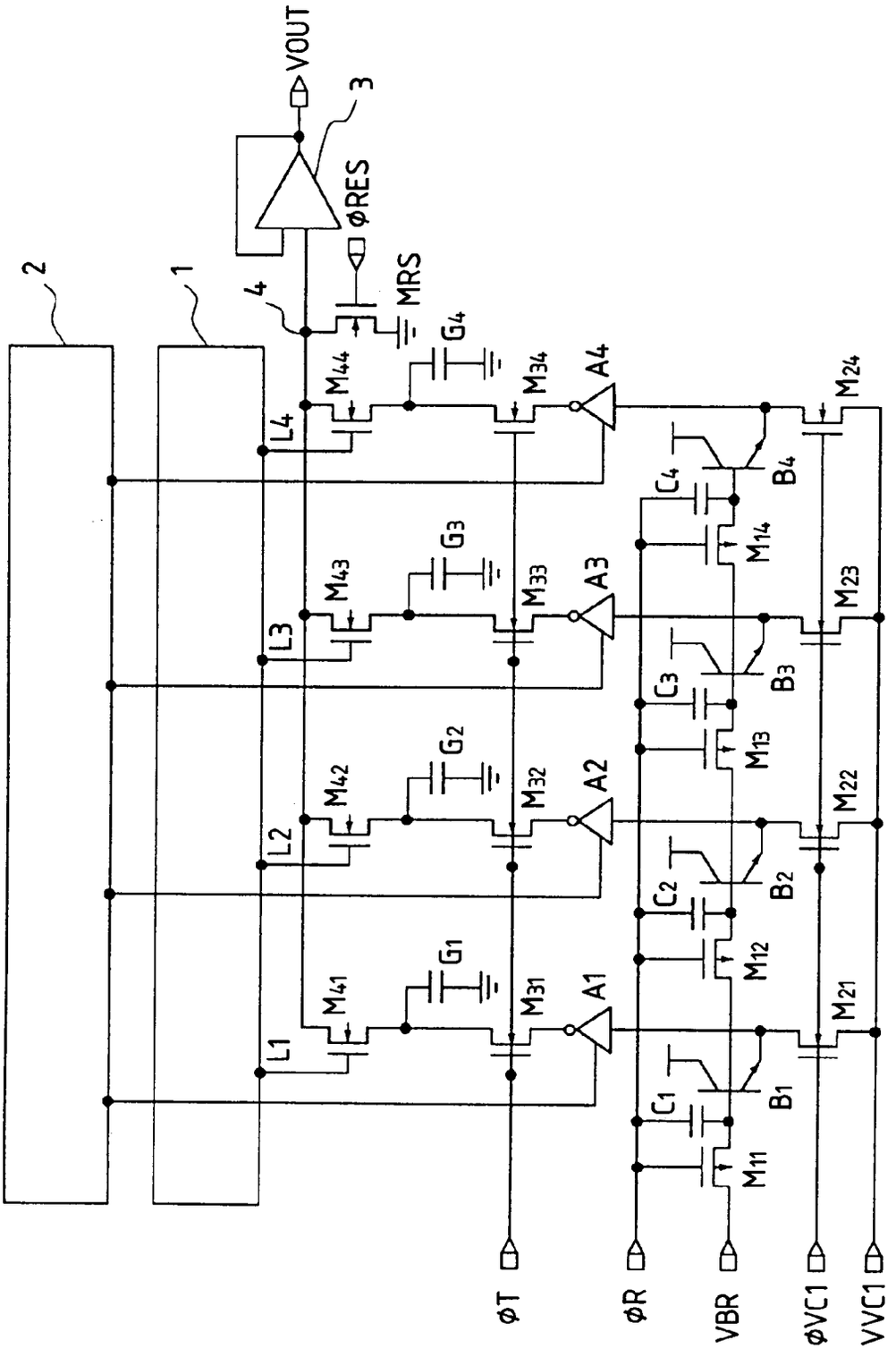
7. A photo-electric conversion apparatus according to Claim 1, further comprising operating means for operating a plurality of output signals gain-controlled by said gain controllable amplifier.

8. Photoelectric conversion apparatus comprising an array of photoelectric conversion sensors (B, 11, s) and amplifying means (A, 10) for amplifying the signals read from the photoelectric conversion sensors,
   characterised by gain control means (2, M51-M54) for adjusting the gain applied to a signal by the amplifying means in dependence upon which of the photoelectric conversion sensors it was read from.

9. Apparatus according to claim 8 in which the amplifying means comprises an array of amplifiers (A, 10) each for amplifying the signal read from a respective said photoelectric conversion sensor, and a plurality of photoelectric conversion sensors share a common said amplifier.

10. Apparatus according to claim 8 or claim 9 comprising signal storage means (G) for storing the photoelectric conversion signals.

FIG. 1


VOUT
3
ØRES
MRS
4
2
1
G4
M44
M34
A4
L4
M24
C4
B4
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M43
M33
A3
L3
M23
C3
B3
M13
G2
M42
M32
A2
L2
M22
C2
B2
M12
G1
M41
M31
A1
L1
M21
C1
B1
M11
ØT
ØR
VBR
ØVC1
VVC1

FIG. 2

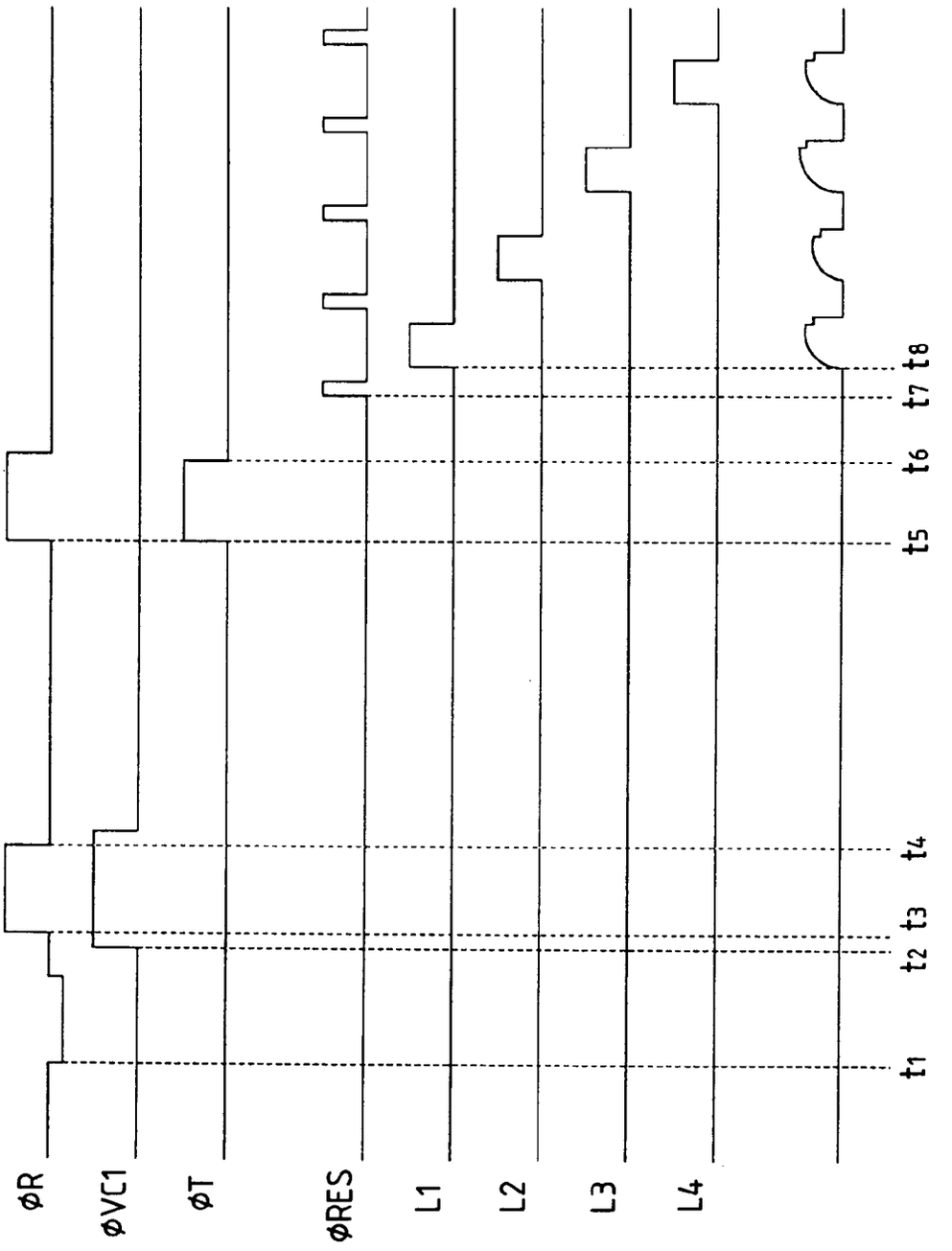


FIG. 3

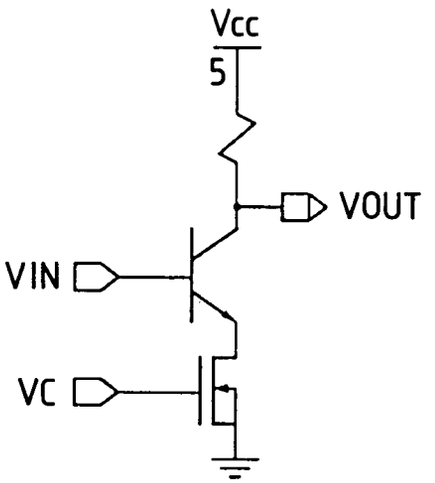

Vcc
5
VOUT
VIN
VC

FIG. 4

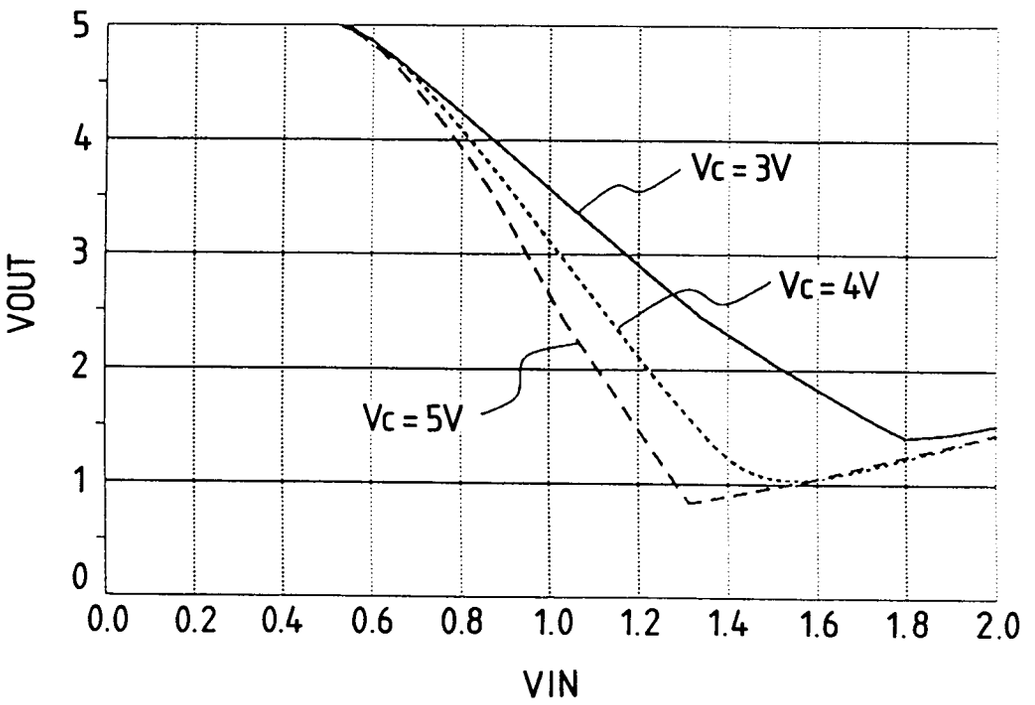

5
4
3
2
1
0
VOUT
Vc = 3V
Vc = 4V
Vc = 5V
0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
2.0
VIN

FIG. 5

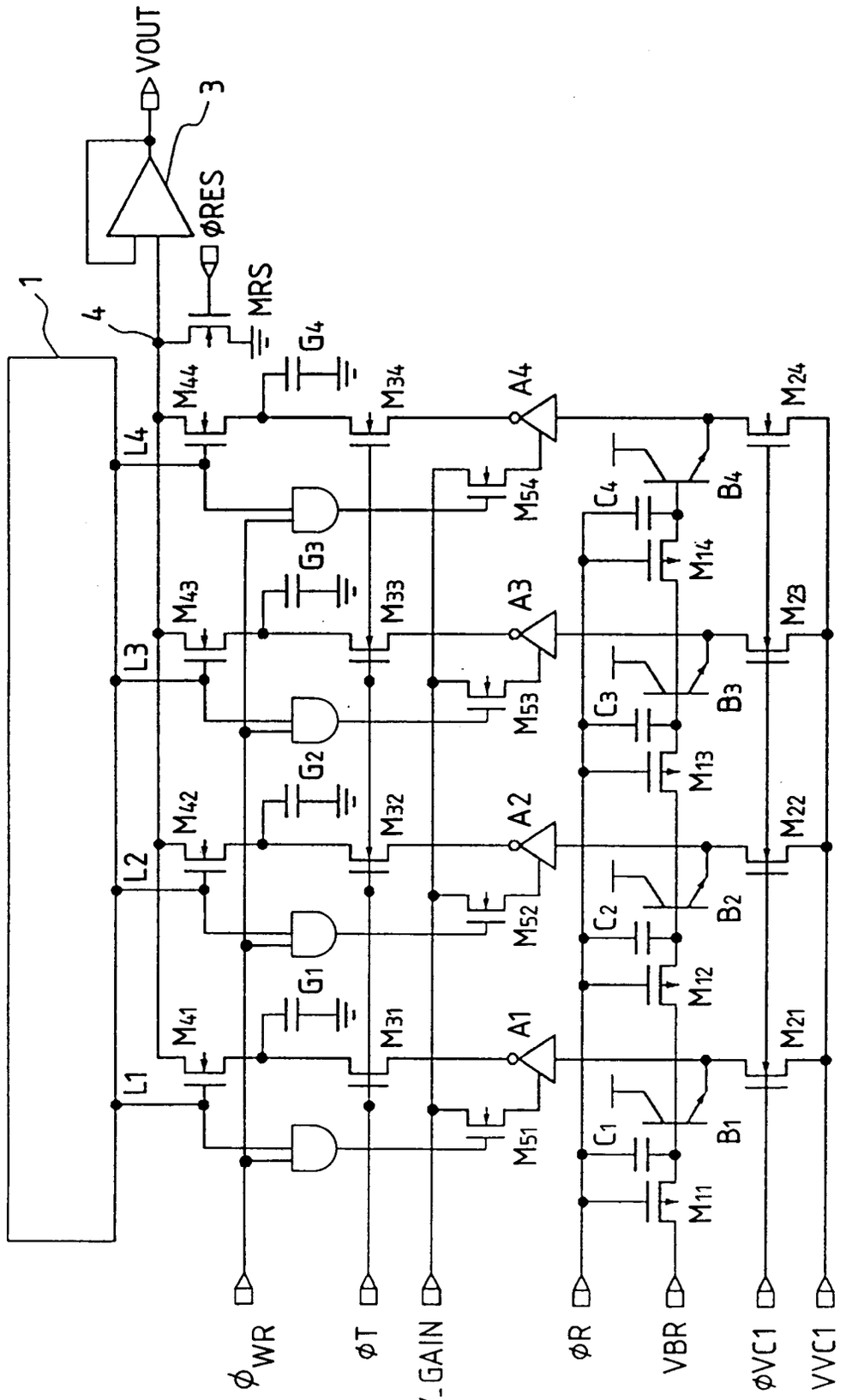
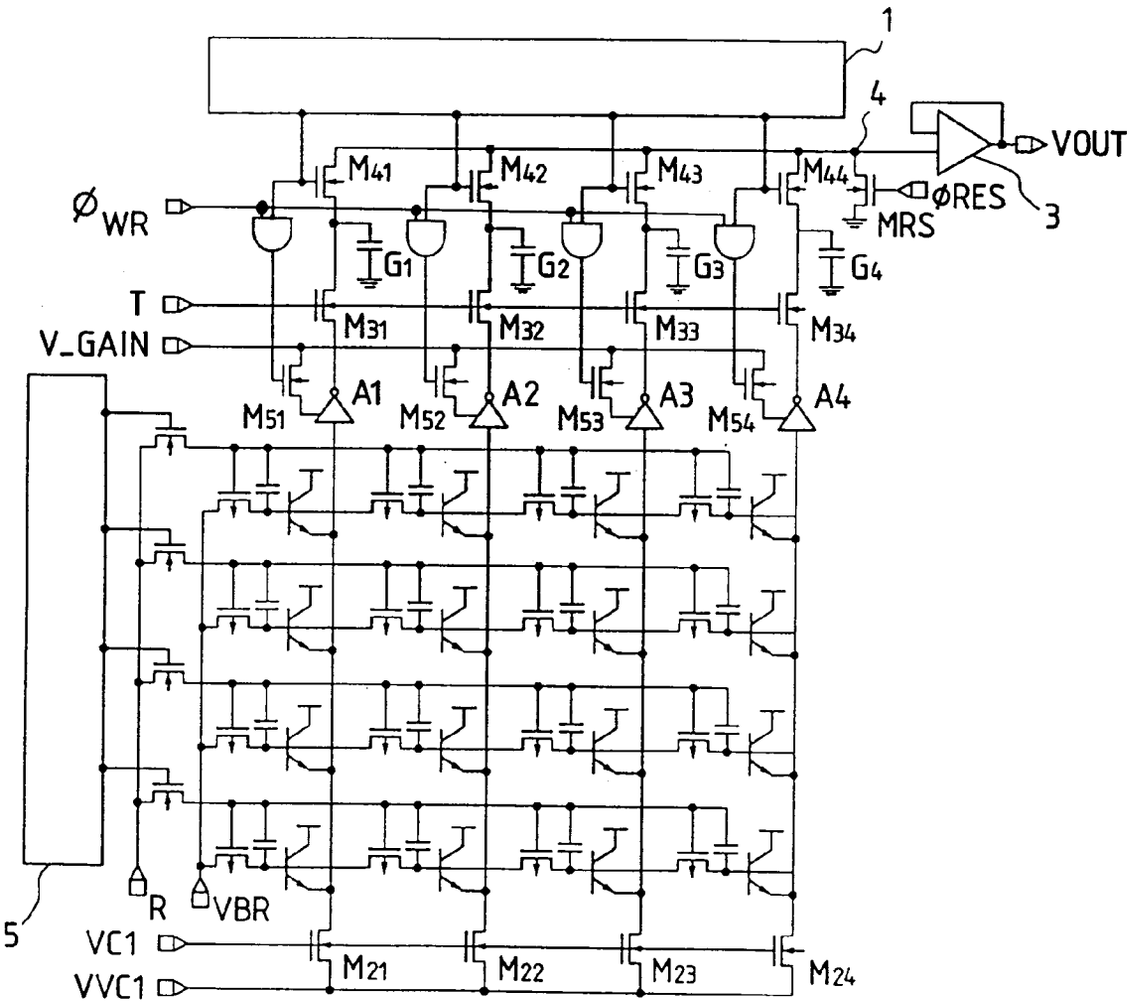

VOUT
3
ØRES
MRS
1
4
G4
M44
M34
A4
L4
M54
C4
B4
M14
M24
G3
M43
M33
A3
L3
M53
C3
B3
M13
M23
G2
M42
M32
A2
L2
M52
C2
B2
M12
M22
G1
M41
M31
A1
L1
M51
C1
B1
M11
M21
ØWR
ØT
V_GAIN
ØR
VBR
ØVC1
VVC1

FIG. 6


1
4
VOUT
3
ØRES
MRS
M41
M42
M43
M44
ØWR
G1
G2
G3
G4
T
V_GAIN
M31
M32
M33
M34
A1
A2
A3
A4
M51
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M54
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R
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VC1
VVC1
M21
M22
M23
M24

FIG. 7

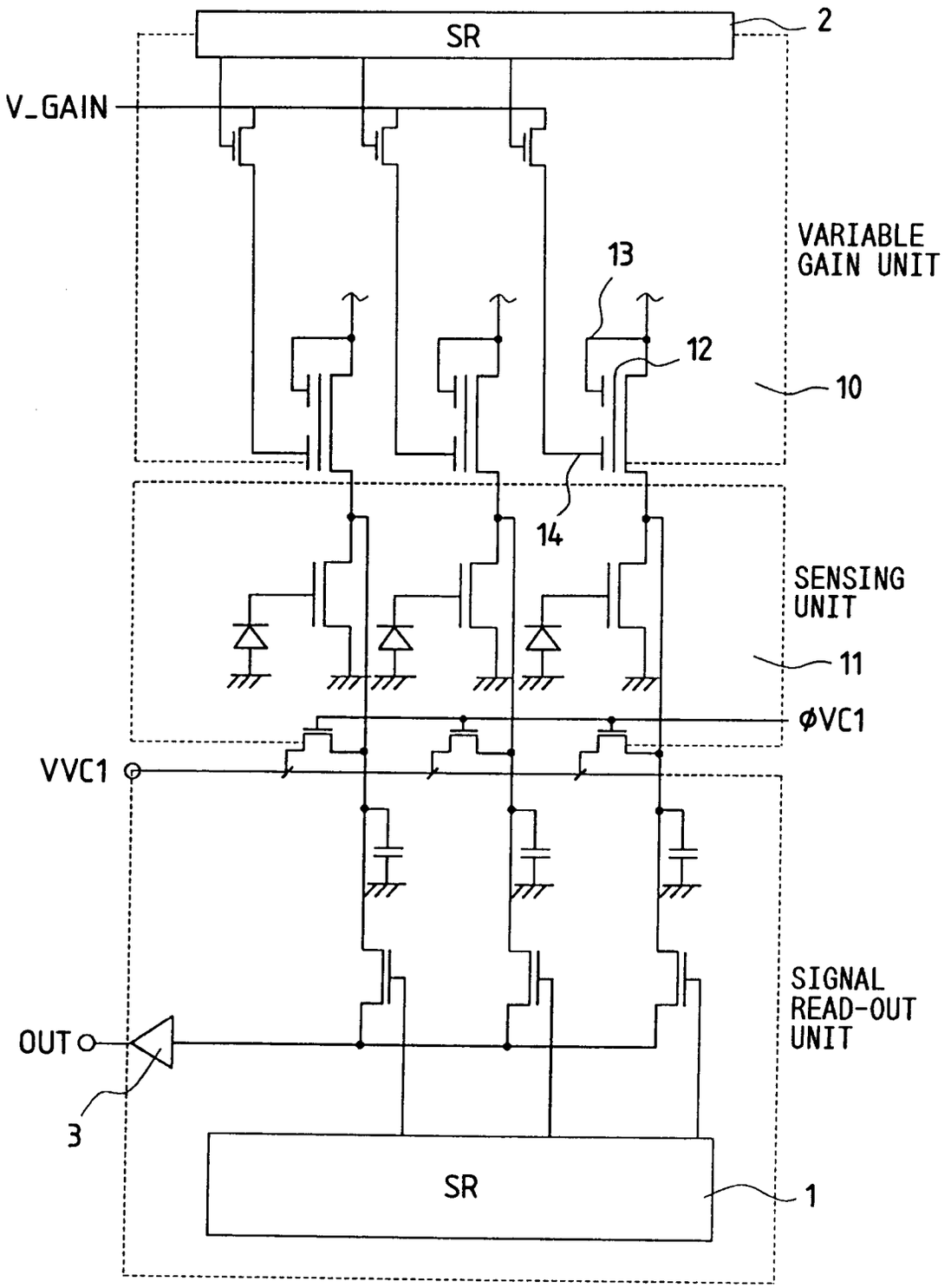
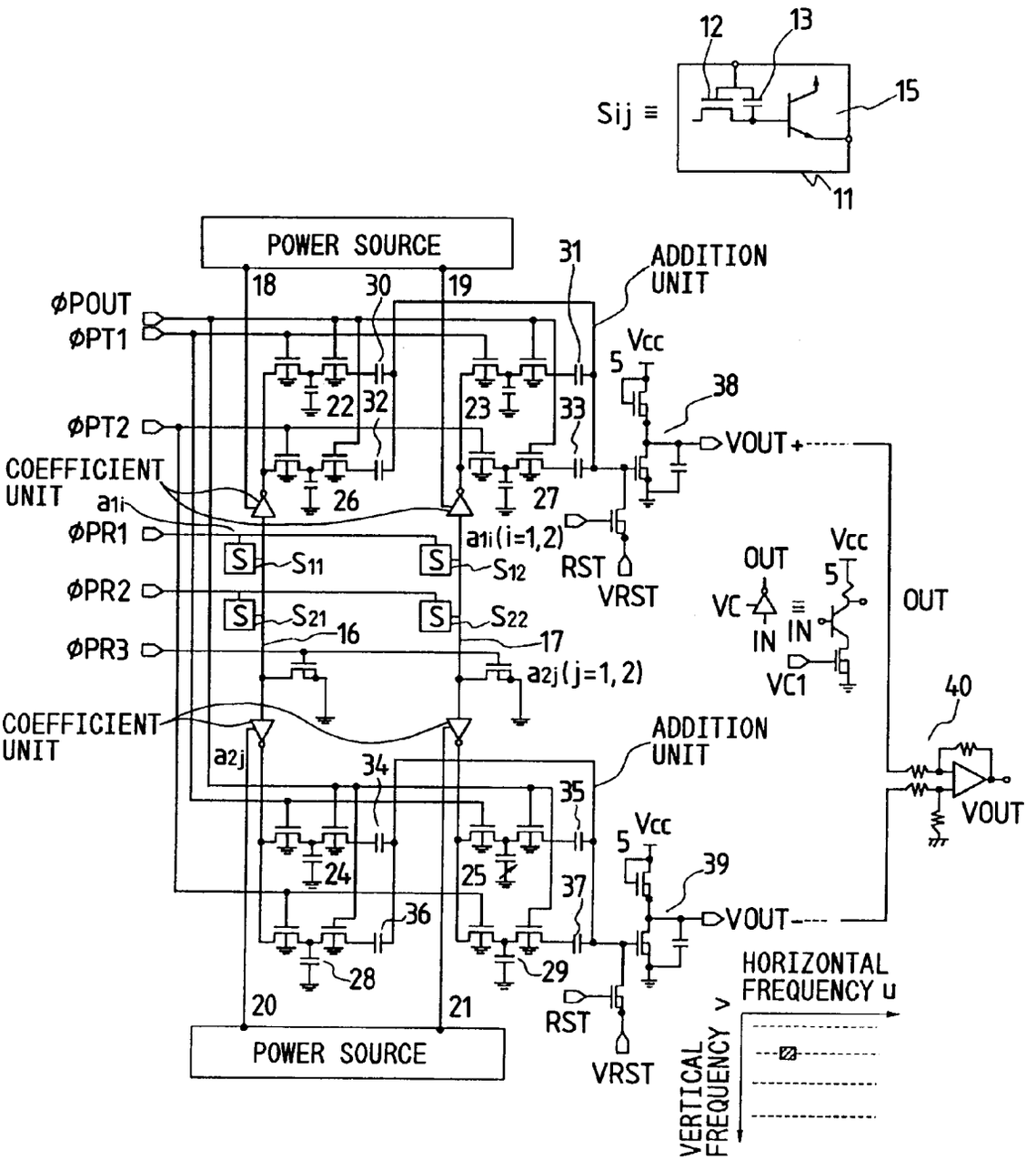

SR
2
V_GAIN
VARIABLE
GAIN UNIT
13
12
10
14
SENSING
UNIT
11
φVC1
VVC1
SIGNAL
READ-OUT
UNIT
OUT
3
SR
1

FIG. 8


Sij ≡
12
13
15
11
POWER SOURCE
ADDITION UNIT
ØPOUT
ØPT1
ØPT2
ØPR1
ØPR2
ØPR3
COEFFICIENT UNIT
a1i
a1i(i=1,2)
a2j
a2j(j=1,2)
Vcc
VOUT+
VOUT-
RST
VRST
OUT
VC
IN
VC1
S11
S12
S21
S22
HORIZONTAL FREQUENCY u
VERTICAL FREQUENCY v

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 94 30 3792

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
X	WO-A-91 04633 (VLSI VISION LIMITED) * page 9, line 1 - line 19 * * page 11, line 12 - line 15 * * page 14, line 16 - line 21; figure 1 * * page 15, line 9 - line 14 *	1-4,7	H04N3/15
X	GB-A-2 185 654 (DAINIPPON SCREEN) * page 3, line 80 - line 105; figure 10 *	1,7	
A		6	
X	EP-A-0 473 966 (SONY CORPORATION) * column 7, line 6 - line 26; figure 3 *	1	
A	US-A-5 146 339 (SHINOHARA ET AL.) * column 5, line 4 - line 38; figure 3 *	1	

TECHNICAL FIELDS SEARCHED (Int.Cl.5)

H04N

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	9 September 1994	Bequet, T

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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