(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number : **0 631 284 A1**

(12) EUROPEAN PATENT APPLICATION

(21) Application number : **93830279.1**

(22) Date of filing : **28.06.93**

(51) Int. Cl.[5] : **G11C 5/14**

(43) Date of publication of application :
28.12.94 Bulletin 94/52

(84) Designated Contracting States :
DE FR GB IT

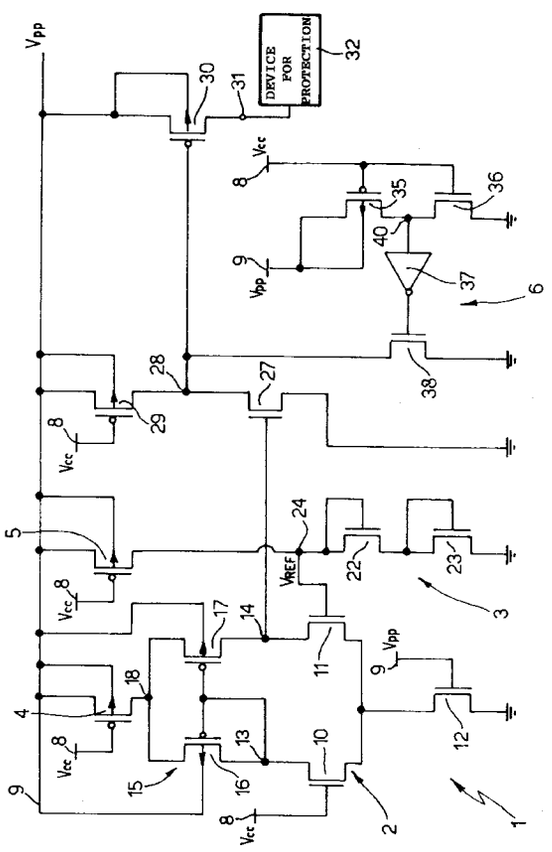
(71) Applicant : **SGS-THOMSON MICROELECTRONICS s.r.l.**
Via C. Olivetti, 2
I-20041 Agrate Brianza (Milano) (IT)

(72) Inventor : **Pezzini, Saverio**
Via Istria 5
I-20059 Vimercate (IT)

(74) Representative : **Jorio, Paolo et al**
Studio Torta,
Via Viotti, 9
I-10121 Torino (IT)

(54) Protection circuit for devices comprising nonvolatile memories.

(57) A protection circuit (1) comprising a first and second supply line (8, 9) at a first and second supply voltage (V_{CC}, V_{PP}) respectively ; a reference voltage source (3) ; a comparator (2) connected to the first supply line (8) and the source ; and a switch (30) controlled by the comparator via a control terminal and located between the second supply line (9) and the output (31) of the circuit (1). To reduce static consumption of the comparator (2) under normal operating conditions, the circuit (1) comprises enabling control elements (4-6, 29) connected to the two supply lines (8, 9) and to the comparator (2) for disabling the comparator and turning on the switch (30) when the two supply voltages differ by a value below a predetermined threshold, but are greater than a reference value.



EP 0 631 284 A1

The present invention relates to a protection circuit for devices comprising nonvolatile memories.

In devices comprising nonvolatile memories, such as EPROMs, EEPROMs and flash-EEPROMs, the content of the memory must be protected in the event supply V_{CC} is inadvertently cut off in the presence of programming voltage V_{PP}, or in the event voltage V_{PP} is applied before supply voltage V_{CC} when the device is turned on.

For this purpose, protection circuits are provided comprising comparators, which compare supply voltage V_{CC} with a reference voltage and, if the supply voltage is lower than the reference voltage, disable supply of voltage V_{PP} to prevent damaging the memory or altering the stored data.

A drawback of known circuits of the aforementioned type is the high static consumption, not always desirable, of the comparators employed.

It is an object of the present invention to provide a protection circuit designed to overcome the above drawback.

According to the present invention, there is provided a protection circuit for devices comprising nonvolatile memories, as claimed in Claim 1.

A preferred, non-limiting embodiment of the present invention will be described by way of example with reference to the accompanying drawing, which shows a simplified electric diagram of the circuit according to the present invention.

The circuit according to the present invention, indicated as a whole by 1 in the accompanying drawing, receives two reference voltages V_{CC} (defining the supply voltage) and V_{PP} (defining the programming voltage of the memory, not shown) supplied respectively over lines 8 and 9. The circuit substantially comprises a comparator 2, a reference voltage V_{REF} source 3 (both supplied with voltage V_{PP} via respective P channel MOS transistors 4, 5), and an inverter 6 supplied with voltage V_{PP} and controlled by supply voltage V_{CC}.

More specifically, comparator 2 comprises a pair of N channel MOS transistors 10, 11 having the control terminals connected respectively to V_{CC} supply line 8 and voltage source 3; the source terminals connected to each other and to a constant current source 12 (in this case, a MOS transistor); and the drain terminals connected (at nodes 13, 14) to the inputs of a current mirror 15 formed by two P channel MOS transistors 16, 17. Transistor 16 connected to transistor 10 of comparator 2 is diode-connected, with its control terminal shortcircuited with its drain terminal connected to node 13. The source terminals of transistors 16, 17 not connected to nodes 13, 14 are mutually connected at node 18, which is connected via transistor 4 to line 9 supplying voltage V_{PP} Transistor 4 presents the control terminal connected to line 8 (V_{CC}), the drain terminal connected to node 18, and the source terminal and substrate connected to line 9. The drawing also shows the connection between the substrate of transistors 16, 17 and line 9 (V_{PP}).

In the embodiment shown, voltage source 3 is formed by the series connection of two diode-connected N channel MOS transistors 22 and 23 connected between node 24, to which the control terminal of transistor 11 is connected, and ground (also defined as reference potential line). Node 24 is also connected to line 9 via transistor 5, which presents the control terminal connected to voltage V_{CC}, the drain terminal connected to node 24, and the source terminal and substrate connected to line 9.

The output node 14 of comparator 2 is connected to the control terminal of an N channel MOS output transistor 27 having the source terminal grounded and the drain terminal connected, via node 28, to the drain terminal of a P channel MOS transistor 29, which presents the control terminal connected to V_{CC} line 8, and the source terminal and substrate connected to V_{PP} line 9. Transistors 27 and 29 combine to form an inverter.

Node 28 is connected to the output of inverter 6 and to the control terminal of a P channel MOS transistor 30 operating as a switch. More specifically, transistor 30 presents the source terminal and substrate connected to line 9, and the drain terminal (defining output 31 of circuit 1) connected to the device 32 for protection (including a memory not shown).

Inverter 6 comprises a pair of opposite-channel transistors 35, 36 series connected to each other; an inverter 37; and an N channel MOS transistor 38 operating as a switch. More specifically, transistor 35 is of P channel type, with the source terminal and substrate connected to line 9; the drain terminal connected to the drain terminal of transistor 36 at node 40; and the control terminal connected to the control terminal of transistor 36 and to V_{CC} line 8. Transistor 36, which is of N channel type, also presents a grounded source terminal. Inverter 37 is located between node 40 and the control terminal of transistor 38, which presents a grounded source terminal, and the drain terminal connected to node 28.

Operation of the above circuit will now be described with reference to three possible states of supply lines 8 and 9. In the following description, the threshold voltage of the PMOS transistors (the voltage between the source terminal and control terminal, over and above which the transistor is turned on) is indicated by V_{TH}.

$V_{CC} < V_{REF}$ and $V_{CC} < V_{PP} - V_{TH}$ (i.e. $V_{PP} - V_{CC} > V_{TH}$)

This situation is typically encountered when, for any reason, the supply voltage (but not the programming voltage) is cut off, or, when the device is turned on, the programming voltage increases more rapidly than the supply voltage, in which case, supply of the programming voltage must be prevented.

In the above situation, transistor 35 is on; transis-

tor 36 is off; node 40 is high; the output of inverter 37 is low, so that transistor 38 is off; transistors 4, 5 and 29 are on and supply comparator 2 and voltage source 3; and, since the control terminal of transistor 10 is at a lower potential (V_{CC}) than node 24 (V_{PP}), output 14 of comparator 2 is low, transistor 27 is off, node 28 presents roughly the same potential as line 9 (V_{PP}), and transistor 30 is off, thus disabling supply of V_{PP}.

$V_{CC} > V_{REF}$ and $V_{CC} > V_{PP} - V_{TH}$ (i.e. $V_{PP} - V_{CC} < V_{TH}$)

This is the normal operating situation encountered far more frequently than the others (e.g. when reading the memory of device 32) and in which static consumption of comparator 2 is undesirable.

In the above situation, transistor 35 is off; transistor 36 is on; node 40 is low; the output of inverter 37 is high; transistor 38 is on, thus grounding node 28; transistor 30 is on, thus enabling supply of V_{PP}; and transistors 4, 5 and 29 are off, so that comparator 2 is also off and absorbs no current. The state of transistor 27 is unknown.

$V_{REF} < V_{CC} < V_{PP} - V_{TH}$ (i.e. $V_{PP} - V_{CC} > V_{TH}$)

This is a special condition used, for example, when programming the memory, and wherein the supply voltage is higher than the reference voltage, but the programming voltage is much higher than the supply voltage.

In the above condition, transistor 35 is on; node 40 is high; the output of inverter 37 is low, so that transistor 38 is off; transistors 4, 5 and 29 are on and supply voltage source 3 and comparator 2, the output 14 of which is high; transistor 27 is on and maintains a low voltage at node 28; and transistor 30 is on, thus enabling supply of programming voltage V_{PP} to output 31 of the circuit and to device 32.

As this is a special operating condition lasting only a small portion of the overall operating time of the memory, consumption by comparator 2 is acceptable.

When both V_{CC} and V_{PP} are low, transistor 30 is probably off. As a low V_{PP} value, however, in no way endangers device 32, the state of circuit 1 is of little importance.

The advantages of the circuit according to the present invention will be clear from the foregoing description. Firstly, it provides for detecting situations endangering the device and due to the supply voltage being cut off in the presence of programming voltage, or due to the programming voltage rising more rapidly as compared with the supply voltage when the device is turned on. Secondly, under normal operating conditions, static consumption of the comparator is zero, thus eliminating any consumption and associated dissipation problems. In any case, the circuit according to the present invention provides for correct supply of the programming voltage as determined by the operating conditions.

Finally, the solution described is straightforward in design, provides for troublefree implementation and integration, and presents a high degree of reliability in any situation.

To those skilled in the art it will be clear that changes may be made to the circuit described and illustrated herein without, however, departing from the scope of the present invention. In particular, implementation of the components may differ as compared with that described, e.g. instead of being MOS types, the transistors may consist of bipolar devices.

Claims

1) A protection circuit (1) for devices (32) comprising nonvolatile memories, the circuit (1) comprising at least a first (8) and a second (9) supply line at a first (V_{CC}) and second (V_{PP}) supply voltage respectively; reference voltage source means (3); comparing means (2) connected to said first supply line (8) and to said source means; and switch means (30) controlled by said comparing means via a control terminal and located between said second supply line (9) and the output (31) of said circuit (1); characterized by the fact that it comprises enabling control means (4-6, 29) connected to said first and second supply lines (8, 9) and to said comparing means (2) for disabling said comparing means and turning on said switch means (30) when said first and second supply voltages differ by a value below a predetermined threshold.

2) A circuit as claimed in Claim 1, characterized by the fact that said enabling control means (4-6, 29) comprise a first controlled switch (4) located between said second supply line (9) and said comparing means (2) and having the control terminal connected to said first supply line (8).

3) A circuit as claimed in Claim 1 or 2, characterized by the fact that said source means (3) are connected to said second supply line (9) via a second controlled switch (5) located between said second supply line and said source means and having the control terminal connected to said first supply line (8).

4) A circuit as claimed in one of the foregoing Claims from 1 to 3, characterized by the fact that said comparing means (2) comprise a differential circuit (10, 11) having an output terminal (14) connected to the control terminal of an output transistor (27) connected between said second supply line (9), via a third controlled switch (29), and a reference potential line.

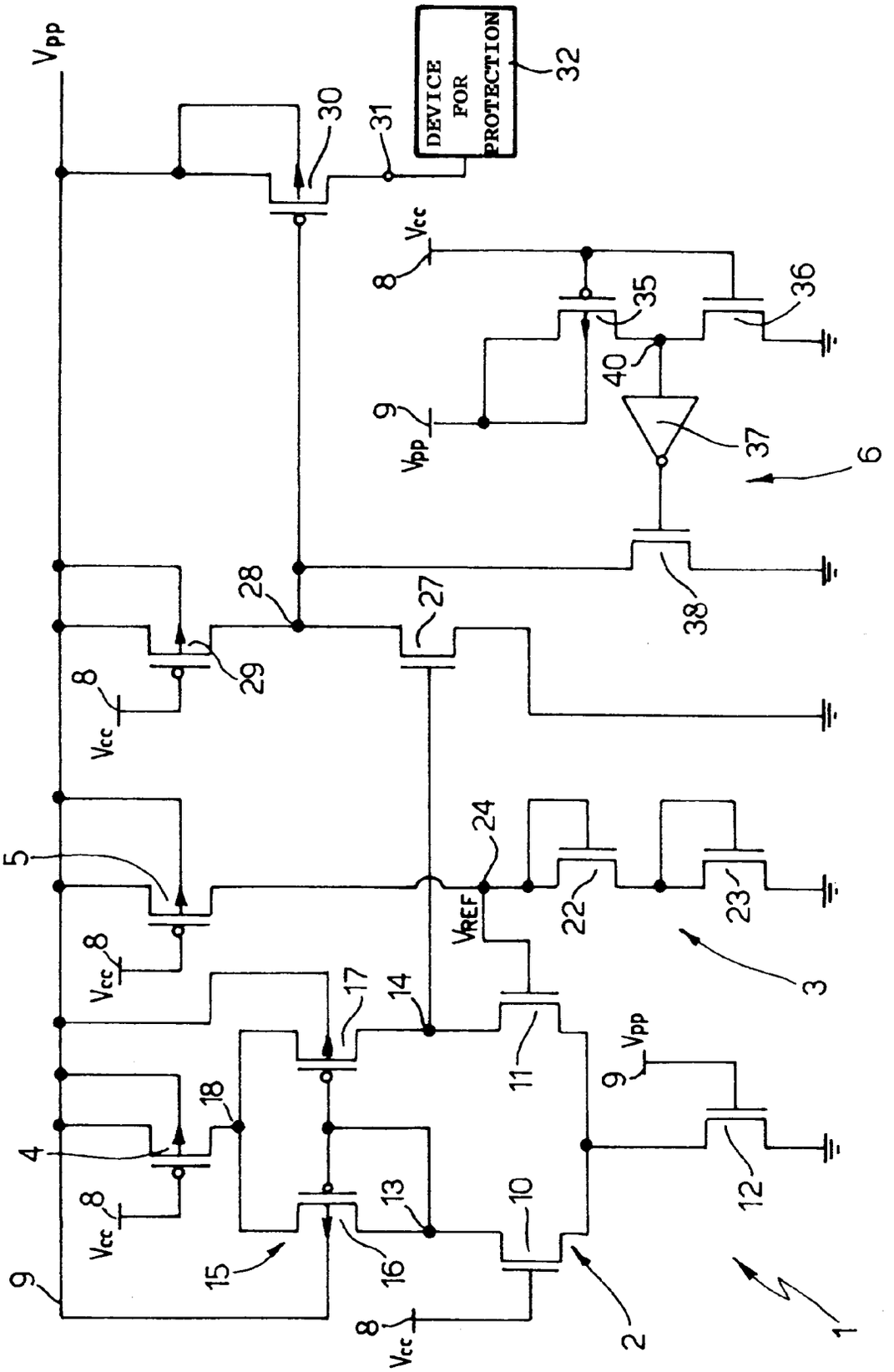
5) A circuit as claimed in Claims 2 to 4, characterized by the fact that each of said first, second and third controlled switches (4, 5, 29) comprises a P channel MOS transistor; and said output transistor (27) comprises an N channel MOS transistor.

6) A circuit as claimed in one of the foregoing Claims from 1 to 5, characterized by the fact that said enabling control means (4-6, 29) comprise a differential inverter stage (6) having a first and second input

connected respectively to said first and said second supply line (8, 9), and an output (28) connected to said control terminal of said switch means (30).

7) A circuit as claimed in Claim 6, characterized by the fact that said inverter stage (6) comprises a first and second transistor (35, 36) having respective first terminals connected to the same node (40), respective second terminals connected respectively to said second supply line (9) and to a reference potential line, and respective control terminals connected to each other and to said first supply line (8); an inverter element (37) having an input connected to said node (40), and an output; and a third transistor (38) having a first terminal connected to said control terminal of said switch means (30), and a control terminal connected to said output of said inverter element (37).

8) A circuit as claimed in Claim 7, characterized by the fact that said first transistor (35) is a P channel MOS transistor; and said second and third transistors (36, 38) are N channel MOS transistors.


Vpp
DEVICE FOR PROTECTION
32
30
31
Vcc
8
35
36
40
9
Vpp
37
6
38
28
27
29
5
24
VREF
22
23
3
17
14
11
18
4
13
10
12
15
16
2
1

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 93 83 0279

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	EP-A-0 454 170 (NEC) * column 6, line 14 - column 10, line 46; figure 3 *	1,2,4	G11C5/14
A	EP-A-0 053 273 (ITT) * page 4, line 33 - page 5, line 25; figure 1 *	1	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

G11C

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	25 November 1993	Cardus, A

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)