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## (54) Liquid crystal display apparatus.

(57) A multi-gradation thin-film liquid crystal display (TFT/LCD) includes a data line driver which does not cause an increase in the chip area, (i.e., which is constituted of a smaller number of circuit elements). Power supplies having respective reference potentials $V_a$ and $V_b$ corresponding to at least two different gradations, and switches $SW_a$ and $SW_b$ for selectively supplying the respective potentials to a data line, are provided in a driver IC for driving the data lines of a TFT/LCD panel. If an output potential corresponding to an arbitrary gradation between the two predetermined gradations is denoted by $V_c$, the output potential $V_c$ is supplied to the data line by being turned on and off the switches $SW_a$ and $SW_b$ alternately at a predetermined cycle in a ratio in which the potential $V_c$ proportionally divides the potentials $V_a$ and $V_b$. Therefore, the output potential corresponding to an arbitrary gradation between the two predetermined gradations can be obtained simply by properly changing the ratio of turning the two switches on and off.

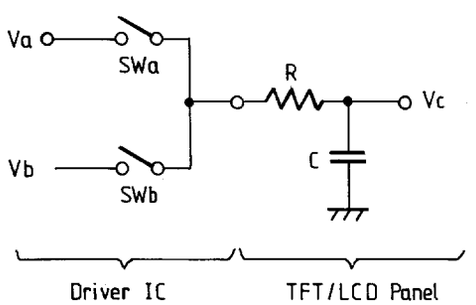


FIG. 2

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The present invention relates to a liquid crystal display apparatus including a driver for driving data lines of the liquid crystal display panel.

Drivers for multi-gradation thin-film transistor liquid crystal displays (TFT/LCD) are generally classified into analog type and digital type. In the analog type driver, an analog data signal representing gradations of respective pixels is sampled and held using switches and capacitors, buffered in operational amplifiers (voltage followers) and then output to data lines of a display panel.

In theory, the analog type driver can produce continuous (i.e., infinite) gradations. In practice, however, there are various problems such as low accuracy of output voltages, low operation speed and large power consumption, and thus the analog type driver is rarely used for computer displays.

On the other hand, in the digital type driver, a plurality of power supplies having different potentials are connected to each data line through their respective switches and a voltage signal is supplied to each data line by selectively turning on one of the switches in accordance with the input data. Since no linear circuit is used, the digital type driver consumes little power. Furthermore, since the power supply voltages are output as they are, output voltages are highly accurate and the operation speed can easily be increased. However, to increase display gradations, it is necessary to increase the number of power supply terminals to provide potentials corresponding to the respective necessary gradations and the number of switches corresponding to the respective power supply terminals.

Japanese patent application PEPA No. 61-58008 published on December 9, 1986 discloses a voltage generation circuit for producing a plurality of differing voltage outputs from a pair of power supplies in the above type of driver. In this circuit, a plurality of intermediate voltages between the voltages of the pair of power supplies are generated by dividing the interval between the two power supply voltages using a plurality of resistors based on the operation of selection switches. By connecting capacitors at positions where the voltage difference across the terminals of the division resistor is constant, the problem of the output waveform distortion is solved without increasing the power consumption.

However, in the above conventional circuit, a number of resistors and switches need to be provided on a chip. Therefore, to increase the number of display gradations, the chip area unavoidably increases. In practice, it is difficult to perform multi-gradation display of more than about 16 gradations using a driver formed on a small chip.

Accordingly, an object of the present invention is to provide a liquid crystal display apparatus which can perform multi-gradation display without increasing the chip area of the driver, i.e., with a smaller number of circuit elements.

Accordingly, the present invention provides a liquid crystal display apparatus comprising a liquid crystal display panel having a plurality of display cells arranged in a matrix and a plurality of data lines connected to the display cells, means for receiving input data comprising a plurality of bits per pixel, said plurality of bits representing gradations of a pixel to be displayed on the panel, and a drive means for driving the data lines by potential signals corresponding to the respective gradations represented by the input data, the drive means comprising: at least two switches connected to a power supply for selectively supplying reference potentials corresponding to at least two different graduation values to the data line; and decoding means responsive to the input data to control said two switches so that the switches are alternately turned on and off at a predetermined cycle so as to supply a potential to said data line, obtained from said reference potential, corresponding to a gradation represented by the input data.

Thus in accordance with the present invention, switches are connected to respective power supplies having reference potentials corresponding to at least two different gradations to allow the reference potentials to be selectively supplied to a data line of the liquid crystal display panel through the switches. A decoder is provided which decodes input data and controls the switches so that the switches are alternately turned on and off at a predetermined cycle at a ratio in which the reference potentials are proportionally divided by a potential corresponding to a gradation represented by the input data.

In a preferred embodiment comprising a thin-film transistor liquid crystal display, multiple graduations can be obtained by means of a driver which needs only two switches to produce the output voltage having an arbitrary level between two potentials. A small chip area is thus achieved.

A preferred embodiment of the invention will now be described, by way of example only, with reference to the accompanying drawings in which:

Figure 1 is a block diagram of a multi-gradation TFT/LCD;

Figure 2 is a schematic circuit diagram showing a relationship between a driver and a data line;

Figure 3 is a timing chart showing on/off cycles of two switches;

Figure 4 is a graph showing how an output voltage changes; and

Figure 5 is a block diagram of a driver according to an embodiment.

Figure 1 is a block diagram schematically showing a multi-gradation thin-film transistor liquid crystal display (TFT/LCD) according to the present invention. In general, this type of display consists of a shift register 1 for converting, to parallel data, serial input data (which represents display gradations of respective

pixels) of a line to be displayed that is received from a data source such as the CPU of a computer, a latch circuit 2 for latching the parallel-converted input data, a driver 5 for driving data lines 4 of a thin-film transistor liquid crystal display 3 by output potentials having magnitudes corresponding to the respective input data of the latch circuit 2, and a scanning circuit (gate driver) 7 for sequentially supplying scanning signals to gate lines 6 of the display panel 3. Each display cell on the gate line 6 being driven by the scanning circuit 7 exhibits gradations corresponding to the output potential of the associated data line.

The input data represents gradations of the respective pixels of one line. For example, in the case of a 64-gradation display, the input data consists of 6 bits per pixel. Therefore, the driver 5 should be able to generate potentials of 64 different magnitudes to properly represent the 6-bit gradation data.

Figure 2 is a schematic circuit diagram which shows a driver circuit embodying the principle of the invention. Switches connected to two respective power sources supplying the terminals of a driver IC having different potentials are turned on and off at a predetermined cycle at a time ratio in which the two potentials are proportionally divided by a potential corresponding to a gradation represented by the input data, so that the output potential necessary to produce the gradation represented by the input data is supplied to the cell.

To describe the above principle more specifically, the potentials of the two power supply terminals are denoted by $V_a$ and $V_b$, the switches connected to the respective terminals are denoted by $SW_a$ and $SW_b$, a load resistance and a capacitance of the data line of the display panel are denoted by R and C, and the output potential given to the cell is denoted by $V_c$. Furthermore, the time necessary to charge up the resistor and the capacitor of the data line is denoted by T, and on-periods of the respective switches $SW_a$ and $SW_b$ in a predetermined cycle t are denoted by $t_a$ and $t_b$, where t « T. When the switches $SW_a$ and $SW_b$ are repeatedly turned on and off at a time ratio as shown in Figure 3, the output potential $V_c$ changes as shown in Figure 4 because of the existence of an RC circuit consisting of the load resistor and the capacitor of the data line, and settles after a lapse of time period T. In this case, the output potential $V_c$ takes a value obtained by proportionally dividing the potentials $V_a$ and $V_b$ in the time ratio $t_a/t_b$. That is,

$$V_c = \frac{t_a V_a + t_b V_b}{t_a + t_b}.$$

It is apparent from Eq. 1 that if either $t_a$ or $t_b$ is made 0 in the on/off operation of the switches $SW_a$ and $SW_b$, the output potential $V_c$ becomes equal to $V_b$ or $V_a$.

It is desirable that T and t not be longer than about 30 μsec. and 3 μsec., respectively. For this reason, where $V_a$ and $V_b$ are 5 V and 4 V, respectively and the time ratio $t_a/t_b$ is an integer-to-integer ratio from 6:0 to 0:6, the output voltage $V_c$ takes values listed in the following table, as derived from Eq. 1.

| $t_a/t_b$ | $V_c$ |
|---|---|
| 6:0 | 5.0 |
| 5:1 | 4.8 |
| 4:2 | 4.7 |
| 3:3 | 4.5 |
| 2:4 | 4.3 |
| 1:5 | 4.2 |
| 0:6 | 4.0 |

In the above manner, generation of an output voltage $V_c$ with an arbitrary level can be obtained between the two power supply potentials by properly changing the time ratio $t_a/t_b$.

Figure 5 schematically shows an embodiment of an invention for driving one data line in the driver 5 (see Figure 1). The driver 5 has this type of circuit in the number of data lines 4. The driver 5 includes a plurality of switches $SW_1$-$SW_{17}$ that are connected to respective power supply terminals having a plurality of potentials $V_1$-$V_{17}$ (e.g., 1 to 17 V), and is constructed so as to selectively supply the potentials of the respective terminals to the data line 4.

Of the 6-bit gradation data supplied from the latch circuit 2 (see Figure 1), the upper 4-bit data is input to a first decoder 11 and the lower 2-bit data is input to a second decoder 12.

Using an incorporated conversion table 13, the first decoder 11 converts the upper 4-bit data to a signal for selecting one switch $SW_i$ and the following switch $SW_{i+1}$ from the switches $SW_1$-$SW_{17}$.

Using an incorporated conversion table 14, the second decoder 12 converts the lower 2-bit data into a signal indicating the ratio (time ratio) between the on-periods $t_a$ and $t_b$ of the respective selected switches $SW_i$ and $SW_{i+1}$. Under the control of a controller (not shown), the switches $SW_i$ and $SW_{i+1}$ are turned on and off at a predetermined cycle (e.g., 3 μsec.) at the time ratio indicated by the output signal of the decoder 12. After this operation is repeated for the predetermined period (e.g., 30 μsec.) necessary to charge up the data line, the output potential to be applied to the cell settles, as described above, to the potential corresponding to the 6-bit gradation data.

As described above, since the on/off time ratio of the two switches is set in accordance with the gradation data, the output potential takes a value corresponding to the gradation data.

## Claims

1. A liquid crystal display apparatus comprising a liquid crystal display panel (3) having a plurality of display cells arranged in a matrix and a plurality of data lines (4) connected to the display cells, means (1, 2) for receiving input data comprising a plurality of bits per pixel, said plurality of bits representing gradations of a pixel to be displayed on the panel, and a drive means (5) for driving the data lines by potential signals corresponding to the respective gradations represented by the input data, the drive means comprising:

   at least two switches (SWa, SWb) connected to a power supply for selectively supplying reference potentials corresponding to at least two different graduation values to the data line; and

   decoding means (11, 12, 13, 14) responsive to the input data to control said two switches so that the switches are alternately turned on and off at a predetermined cycle so as to supply a potential to said data line, obtained from said reference potential, corresponding to a gradation represented by the input data.

2. Apparatus as claimed in claim 1, wherein said power supply comprises at least n+1 terminals for supplying n reference potentials having equal potential differences.

3. Apparatus as claimed in claim 2, comprising n+1 switches connected to the n+1 terminals.

4. Apparatus as claimed in any preceding claim, wherein said decoding means comprises a first table to be referenced for selecting switches connected to terminals having two consecutive reference potentials of said n+1 terminals in accordance with first selected bits of the plurality of bits, and a second table to be referenced for determining a ratio between on and off periods of the two selected switches in accordance with the second selected bits of said plurality of bits.

5. Apparatus as claimed in any preceding claim, wherein the predetermined cycle has a period no greater than 10 percent of the time necessary to charge up the data line.

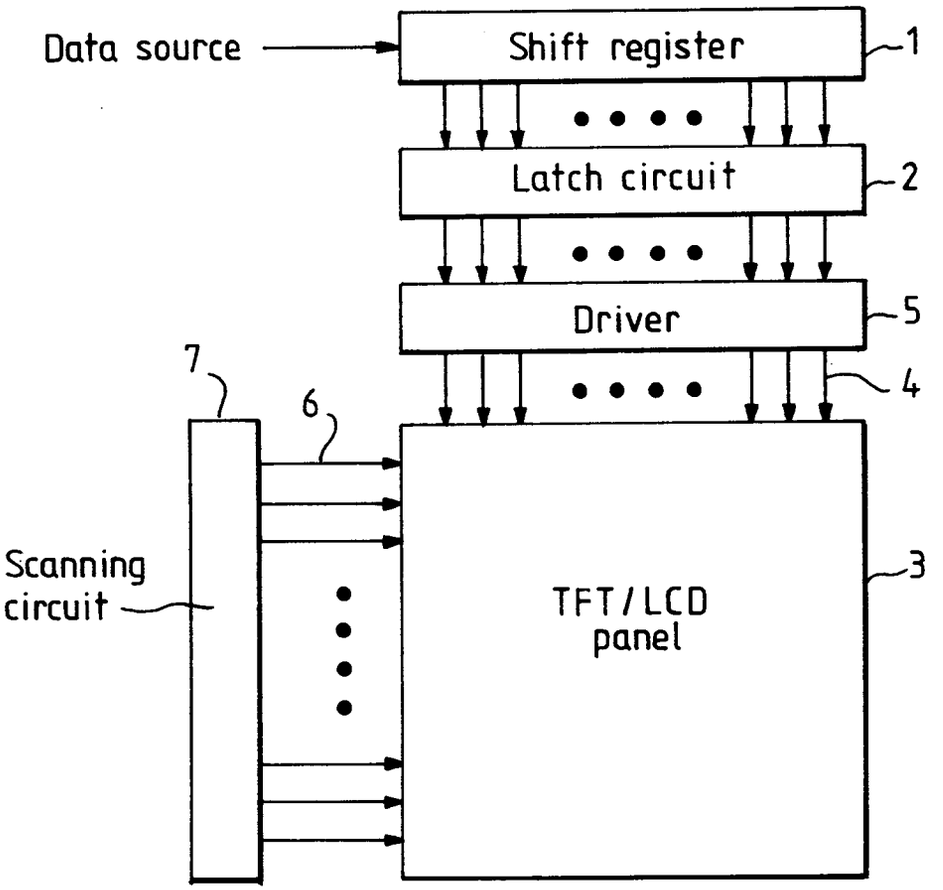
Data source
Shift register
1
Latch circuit
2
Driver
5
4
7
6
Scanning circuit
TFT/LCD panel
3

FIG. 1

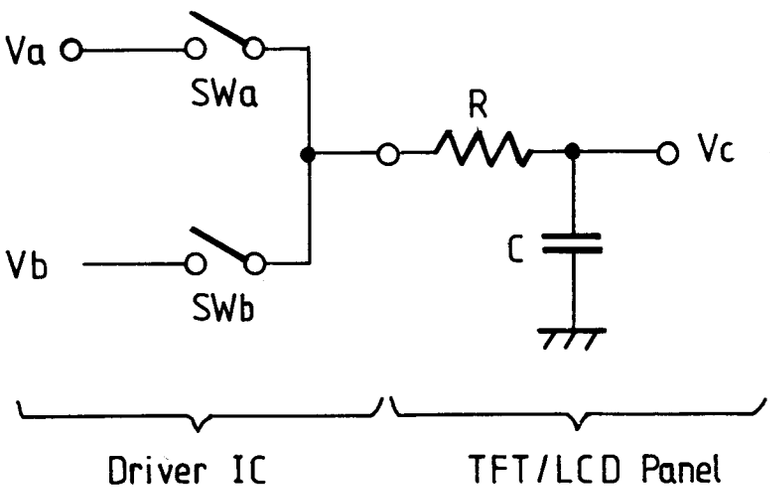
Va
SWa
R
Vc
Vb
C
SWb
Driver IC
TFT/LCD Panel

FIG. 2

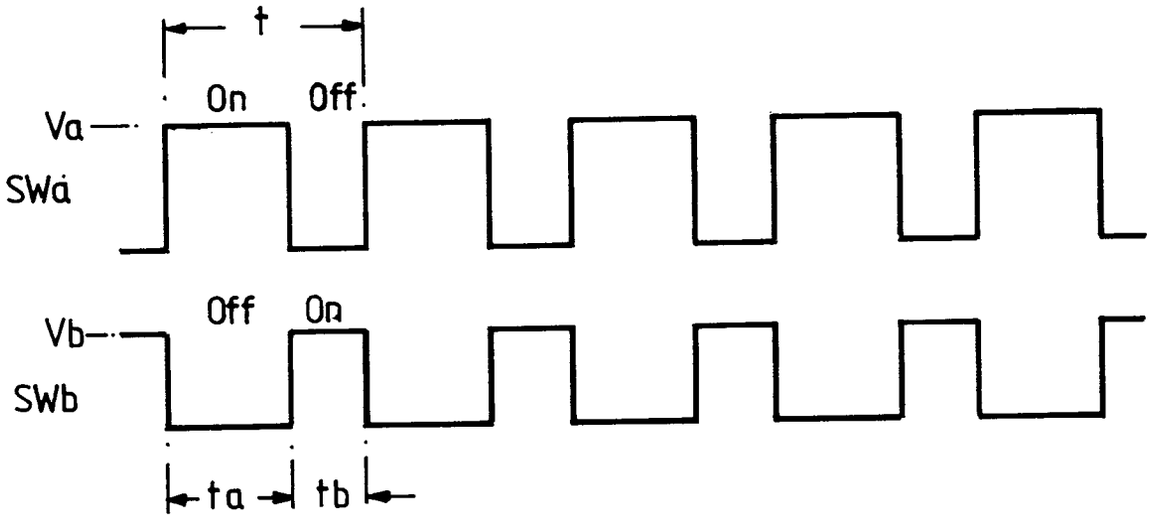


FIG. 3

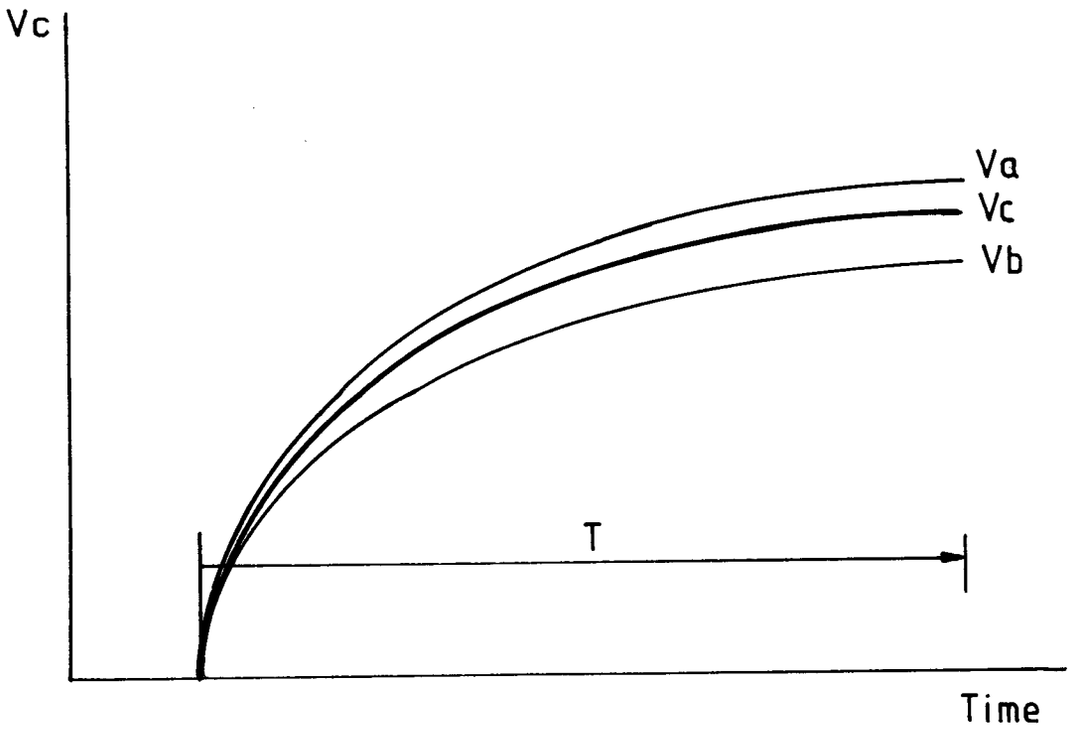


FIG. 4

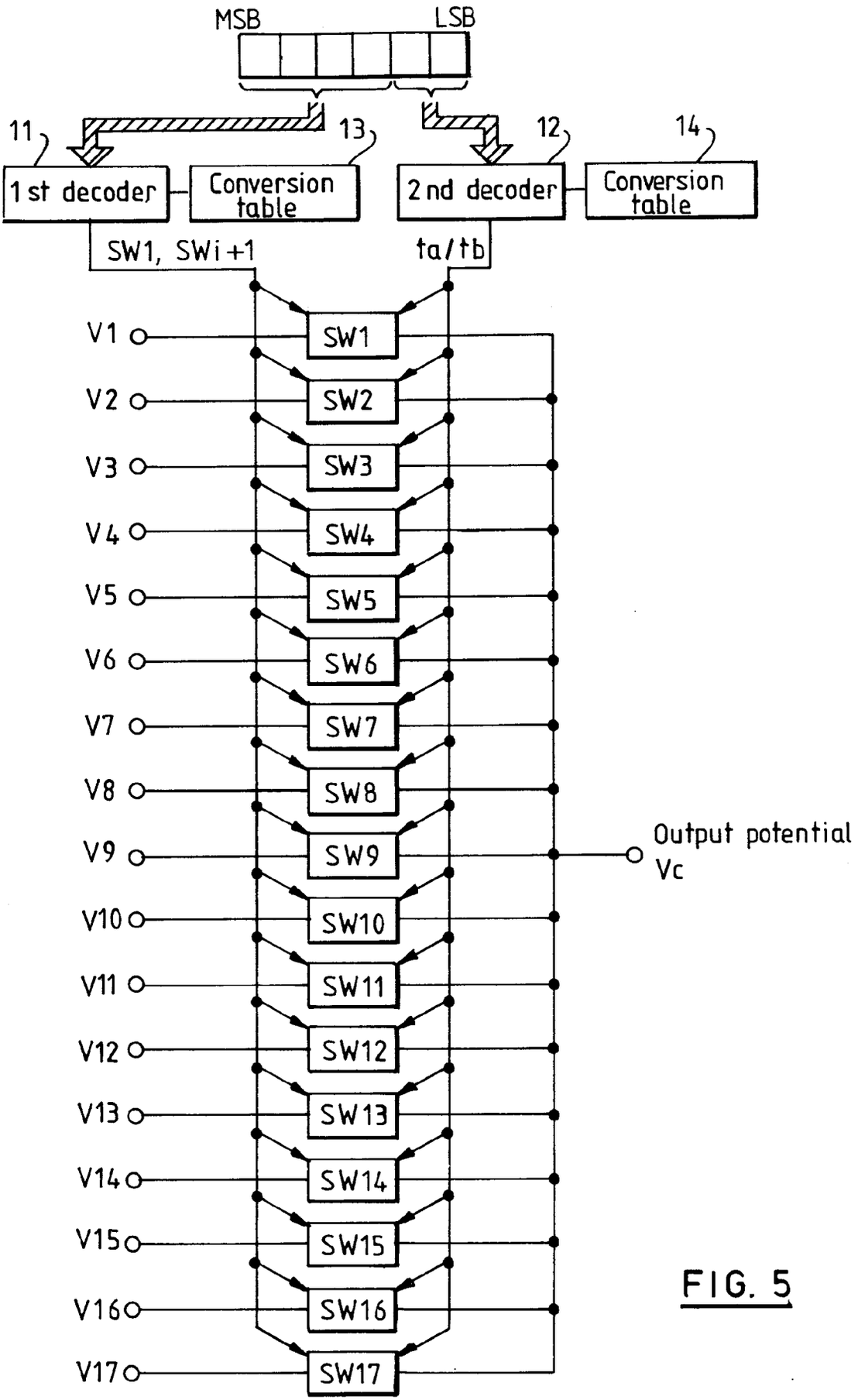
MSB
LSB
11
13
12
14
1 st decoder
Conversion table
2 nd decoder
Conversion table
SW1, SWi+1
ta/tb
V1
V2
V3
V4
V5
V6
V7
V8
V9
V10
V11
V12
V13
V14
V15
V16
V17
SW1
SW2
SW3
SW4
SW5
SW6
SW7
SW8
SW9
SW10
SW11
SW12
SW13
SW14
SW15
SW16
SW17
Output potential
Vc

FIG. 5

European Patent Office

# EUROPEAN SEARCH REPORT

Application Number
EP 94 30 4204

## DOCUMENTS CONSIDERED TO BE RELEVANT

| Category | Citation of document with indication, where appropriate, of relevant passages | Relevant to claim | CLASSIFICATION OF THE APPLICATION (Int.Cl.5) |
|---|---|---|---|
| Y | US-A-4 742 329 (Y. YAMADA ET AL.)<br>* abstract; figures 1,4 *<br>* column 2, line 36 - line 64 *<br>* column 4, line 45 - column 5, line 28 * | 1-3 | H03M1/82<br>G09G3/36 |
| Y | EP-A-0 488 516 (IBM)<br>* abstract; claim 1; figure 1 *<br>* column 1, line 44 - column 2, line 16 *<br>* column 3, line 41 - column 4, line 6 * | 1-3 | |
| A | EP-A-0 075 441 (FUJITSU)<br>* page 21, line 22 - page 22, line 16; figure 12 * | 1-5 | |
| A | PATENT ABSTRACTS OF JAPAN<br>vol. 17, no. 451 (P-1595) 18 August 1993<br>& JP-A-05 100 635 (NEC) 23 April 1993<br>* abstract * | 1-5 | |
| | | | TECHNICAL FIELDS SEARCHED (Int.Cl.5)<br>H03M<br>G09G |

The present search report has been drawn up for all claims

| Place of search | Date of completion of the search | Examiner |
|---|---|---|
| BERLIN | 1 September 1994 | Saam, C |

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
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EPO FORM 1503 03.82 (P04C01)