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(54) Improvements in or relating to synchronization circuits.

(57) A method of synchronizing a data signal of a controller chip 12 to a reference clock signal of a color palette chip 12 in a video driving system 10 includes the steps of altering the reference clock signal frequency, adjusting the phase of an output clock signal from the palette chip 12 wherein the output clock signal coupled with delay from controller chip 12 produces a feedback clock signal that is synchronized with the altered reference clock signal, and latching the data signal with the feedback clock signal thereby synchronizing the data signal to the reference clock signal.

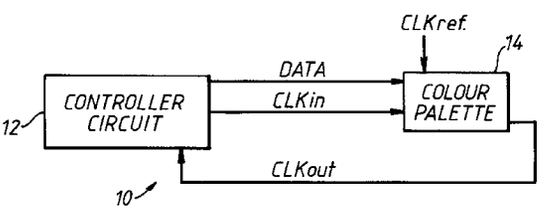

Fig. 1 (PRIOR ART)

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Field of the Invention

This invention relates to electronic circuits and more particularly relates to synchronization circuits in video palette applications.

Background of the Invention

As video systems continue to increase in operational frequency individual integrated circuit chips suffer synchronization problems. FIG.1 is a prior art block diagram illustrating the problem. In FIG.1 a video circuit 10 has a controller chip 12 connected to a video color palette chip 14. Controller chip 12 sends data to color palette 14 at a first frequency and color palette 14 manipulates the data at a second frequency which is greater than the first frequency. Typical examples would be a first frequency of 50 Mhz and a second frequency of 200 Mhz. Due to the high internal operating frequency of color palette 14, it is very difficult to obtain synchronization between color palette 14 and controller chip 12. Since the period of video palette 14 is 5nS and since the delay of the clock through controller chip 12 may be 10-20nS (CLKout - CLKin) it is obvious that synchronization between the two circuits can be a problem.

FIG.2 is a prior art solution to obtain synchronization between data of controller chip 12 and a reference clock signal CLKref of color palette 14. In FIG.2, signals, varying in delay from one another, each incrementally latch data into flip flops 16a-16d such that data is synchronized with CLKref of color palette 14. This solution is limited by the fact that one must assume what delay will be needed to appropriately synchronize data to CLKref. Furthermore, the delay through controller chip 12 is a strong function of temperature, supply voltage, and process variation, therefore the delay may constantly vary. A second disadvantage is that multiple flip flops 16a-16d are needed for each data bit. Therefore, if 64 data bits are incoming, 256 flip flops are needed; if 128 data bits are incoming, 512 flip flops are needed. Obviously, the large number of flip flops take a great deal of area in color palette 14 and dissipate power undesirably.

It is therefore an object of this invention to provide a method of providing synchronization between a controller chip and a video palette having variable delays in clock signals while simultaneously decreasing circuit area and power dissipation. Other objects and advantages of the invention will become apparent to those of ordinary skill in the art having reference to the following specification together with the drawings herein.

Summary of the Invention

A method of synchronizing a data signal of a controller chip 12 to a reference clock signal of a color palette chip 12 in a video driving system 10 includes the steps of altering the reference clock signal frequency, adjusting the phase of an output clock signal from the palette chip 12 wherein the output clock signal coupled with delay from controller chip 12 produces a feedback clock signal that is synchronized with the altered reference clock signal, and latching the data signal with the feedback clock signal thereby synchronizing the data signal to the reference clock signal.

According to the invention, various aspects are defined by claims 1 to 10.

Brief Description of the Drawings

FIG.1 is a prior art block diagram illustrating a video circuit 10.

FIG.2 is a prior art schematic diagram illustrating a synchronization methodology.

FIG.3 is a schematic diagram illustrating the preferred embodiment of the invention, a synchronization circuit 30 within video palette 14 for a video circuit 10 that is independent of process, temperature, or supply voltage variations.

Detailed Description of the Preferred Embodiment

FIG.3 is a schematic diagram illustrating the preferred embodiment of the invention, a synchronization circuit 30 within color palette 14 that provides synchronization between a reference clock (CLKref) and a feedback clock (CLKin) that is independent of process, temperature, or supply voltage variation and occupies less area and dissipates less power than prior art synchronization solutions. Synchronized feedback clock CLKin is then used to latch data (DATAin) from controller chip 12 thereby synchronizing data to CLKref. Synchronization circuit 30 includes a divide circuit 32 that receives a reference clock signal CLKref. Divide circuit 32 is connected to a phase locked loop circuit (PLL) 34. PLL 34 receives feedback clock signal CLKin from controller chip 12 (not shown) and a signal from divide circuit 32 and outputs a clock signal CLKout. Feedback clock signal CLKin is also connected to a D-type flip flop 36. Flip flop 36 takes an external data signal (DATAin) from controller chip 12 as its data input and feedback clock signal CLKin as its clock input and outputs a data signal (DATAout).

FIG.3 operates in the following manner. Synchronization circuit 30 takes reference clock signal CLKref that is operating at 200 Mhz, in this particular embodiment, and divides it down to 50 Mhz through divide circuit 32. It should be understood that other operating frequencies may also be used and that the operating frequency of CLKref is not limited to the frequency of this example. Divide circuit 32 may be a standard counter as is well known by those skilled in the art and may divide down, in alternative embodi-

ments, reference clock CLKref by any value such as, for example, divide by eight or divide by sixteen. Divide circuit 32 outputs a 50 Mhz signal (which may be called altered CLKref) to PLL 34. PLL 34 takes the output of divide circuit 32 and feedback clock signal CLKin, which is also operating at 50 Mhz and synchronizes CLKin to the output of divide circuit 32. PLL 34 obtains synchronization between altered CLKref and CLKin by adjusting the frequency of output clock signal CLKout thereby adjusting the phase of CLKin. Synchronization via adjustment of frequency in phase locked loops is well known by those skilled in the art of circuit design. CLKout then feeds back to controller chip 12 (as shown in FIG.1) where further delay due to various standard operations of controller chip 12 is added. The output clock of controller chip 12 is feedback clock signal CLKin which is then (due to added or removed delay from CLKout via PLL 34) synchronized with altered CLKref. Therefore, the input of PLL 34, which is CLKin, is synchronized with reference clock CLKref. CLKin also serves as a clock input for flip flop 36 which latches data on the rising edge of CLKin. Therefore, data is synchronized with reference clock signal CLKref. More accurately, data is synchronized with the output signal of divide circuit 32 which is altered CLKref. However, if the altered clock reference signal (altered CLKref) is delayed less than a half cycle of CLKref then synchronization between data and CLKref is considered close enough to be considered "effectively" synchronized.

The synchronization of data signal from controller chip 12 to CLKref of color palette 14 in FIG.1 is crucial because, as performance increases, color palette 14 will continue to operate internally at ever increasing frequencies. Because controller chip 12 and color palette 14 operate at different frequencies and have differing internal timing delays, the clock signals that dictate the timing of various operations within the delays between controller chip 12 and color palette 14 will differ. Further, since the delays are functions of temperature, supply voltage, and process variations it is obvious that the delays between controller chip 12 and color palette 14 will consistently vary. Synchronization circuit 30, within color palette 14, advantageously provides synchronization of data to CLKref that is independent of temperature and supply voltage variations as well as differences in process conditions. Still further, synchronization circuit 30 replaces a plurality of flip flops (as shown in FIG.2) with a single phase locked loop circuit 34 thus significantly reducing the area and power dissipation of color palette 14.

Although the invention has been described with reference to the preferred embodiment herein, this description is not to be construed in a limiting sense. Various modifications of the disclosed embodiment as well as other embodiments of the invention, will become apparent to persons skilled in the art upon reference to the description of the invention. It is therefore contemplated that the appended claims will cover any such modifications or embodiments as fall within the true scope of the invention.

Claims

1. A method of synchronizing a data signal of a controller chip to a reference clock signal of a color palette chip in a video driving system, comprising the steps of:
   altering the reference clock signal frequency such that the altered frequency of the reference clock signal is the same frequency as a feedback clock signal of the controller chip;
   adjusting the phase of an output clock signal, wherein the feedback clock signal and the altered reference clock signal are synchronized; and
   latching the data signal with the feedback clock signal wherein the data is thereby synchronized to the reference clock signal.

2. The method of claim 1, further comprising forming said feedback clock signal by coupling the output clock signal with a delay from the controller chip.

3. The method of claim 1 or claim 2, wherein adjusting the phase of the output clock signal comprises the steps of:
   comparing the phase of the feedback clock signal with the phase of the altered reference clock signal; and
   adjusting the frequency of the output clock signal until the phases of the feedback clock signal and the altered reference clock signal are synchronized.

4. A circuit for synchronizing a data signal of a controller chip to a reference clock signal of a colour palette chip in a video driving system comprising:
   means for altering the reference clock signal frequency such that the altered frequency of the reference clock signal is the same frequency as a feedback clock signal of the controller chip;
   phase adjusting means for adjusting the phase of an output clock signal; and
   latching means for latching the data signal with the feedback clock signal such that the data is thereby synchronised to the reference clock, wherein the feedback clock and the altered reference clock signal are synchronized.

5. The circuit of claim 4, further comprising:
   a divide circuit having the reference clock signal as an input and the altered reference clock signal as an output, wherein the frequency of the altered

reference clock signal is a fraction of the frequency of the reference clock signal;
and wherein the phase adjusting means comprise a phase adjust circuit connected to the divide circuit having the altered reference clock signal as a first input and the feedback clock signal as a second input, wherein the frequency of the altered reference clock signal and the feedback clock signal are equal, wherein the feedback clock signal is a delayed function of the output clock signal, wherein the delay between the output clock signal and the feedback clock signal varies with respect to temperature, supply voltage and process variation, wherein the phase adjust circuit adds or removes delay from the output clock signal in response to the phase relationship between the altered clock signal and the feedback clock signal such that the addition or removal of delay from the output clock signal synchronizes the feedback clock signal to the altered reference clock signal;
and the latch means comprises a data storage element having an enable input connected to the feedback clock signal, the data input connected to the data signal and the output wherein the feedback clock signal latches the data signal onto the output of the data storage element thereby synchronizing the data signal to the reference clock signal.

6. The circuit of claim 5, wherein the divide circuit comprises a counter.

7. The circuit of claim 6, wherein the counter comprises a programmable counter.

8. The circuit of any of claims 5 to 7, wherein the phase adjust circuit comprises a phase locked loop.

9. The circuit of any of claims 5 to 8, wherein the data storage element comprises a latch.

10. The circuit of any of claims 5 to 9, wherein the data storage element comprises a flip flop.

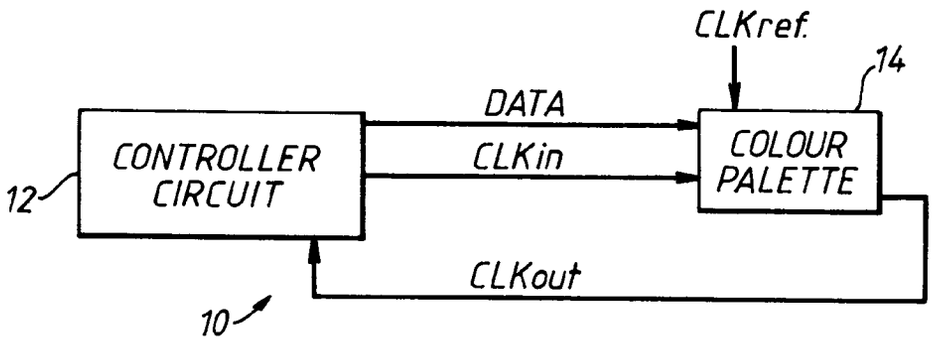

Fig. 1 (PRIOR ART)

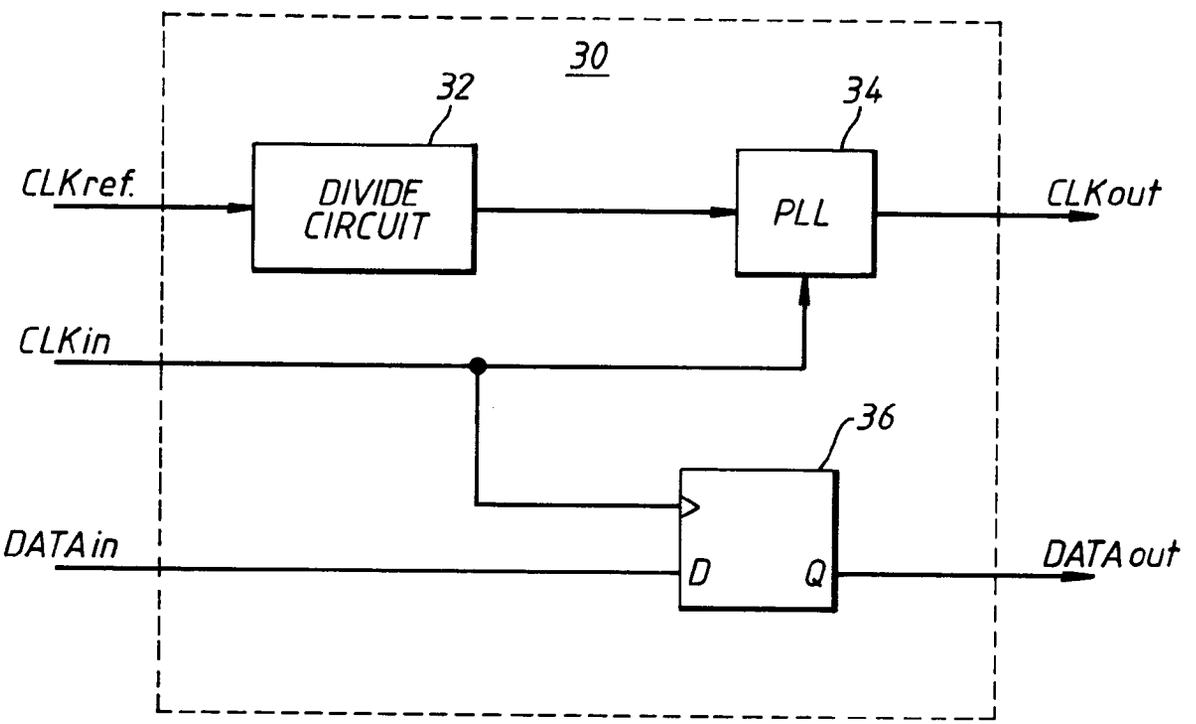

Fig. 3

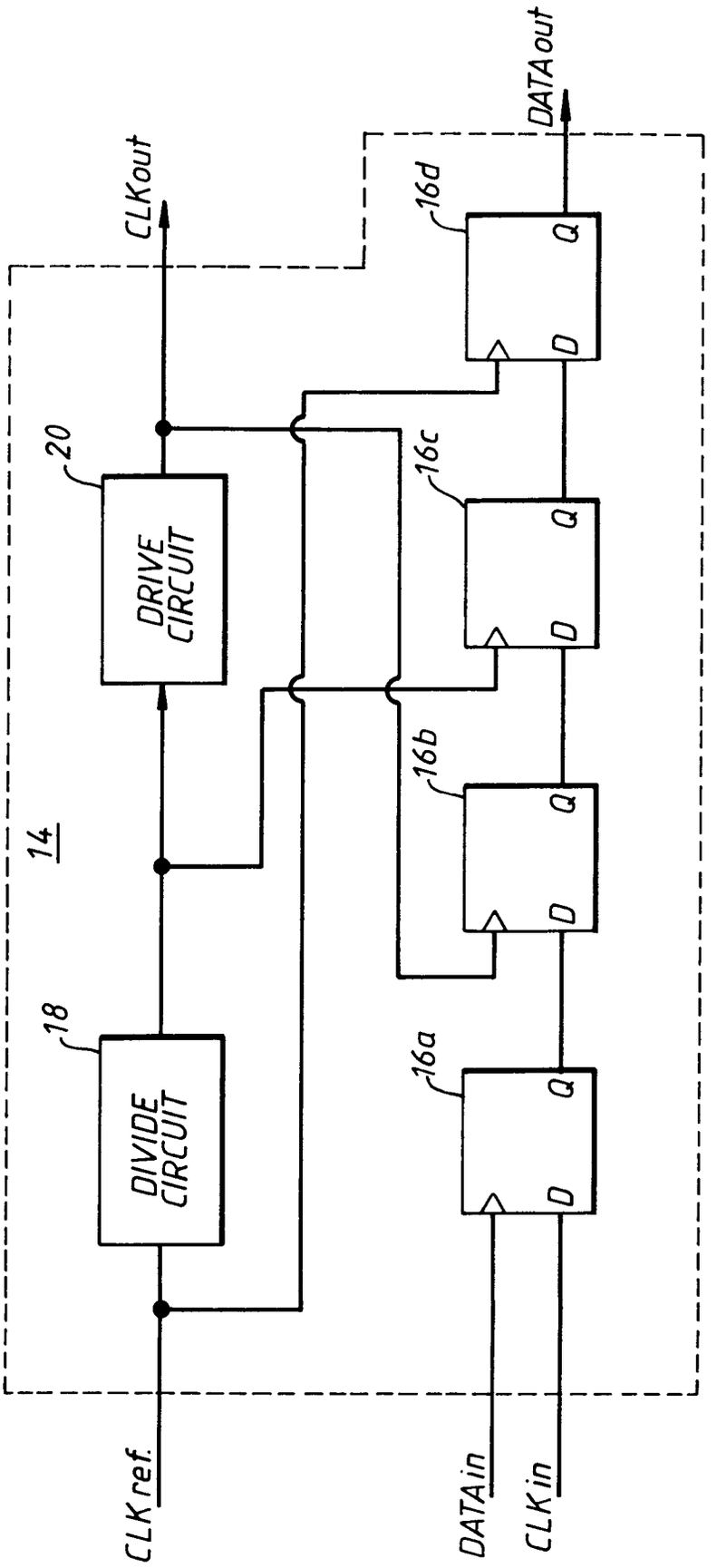

Fig. 2 (PRIOR ART)

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 94 30 6065

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
P,X P,A	US-A-5 291 187 (WOOD ET AL.) * column 3, line 11 - column 5, line 52 * * column 6, line 48 - column 7, line 25 * * column 7, line 62 - column 8, line 15 * * column 13, line 39 - column 16, line 13 * * figures 2-5 *	1,4 2,3,5-10	G09G5/06
A	ELEKTRONIK, vol.41, no.19, September 1992, MUNCHEN DE pages 72 - 76 J. KLIMEK 'Hardware für XGA' * page 75, left column, paragraph 3 - page 76, left column, paragraph 1 *	1,4	
A	EP-A-0 354 480 (SEIKO EPSON CO.) * column 2, line 28 - column 3, line 52 * * column 6, line 44 - column 9, line 14 * * figures 3,4,8 *	1,4	
A	IBM TECHNICAL DISCLOSURE BULLETIN, vol.29, no.11, April 1987, NEW YORK US pages 4859 - 4860 'Programmable dot clock for video adapter' * the whole document *	3,5-8	TECHNICAL FIELDS SEARCHED (Int.Cl.6) G09G

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	6 December 1994	FARRICELLA, L

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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