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(54) Full adder circuit.

(57) A full adder circuit having a plurality of full adders each provided for each bit, each full adder comprising: a calculation block (31a) responsive to a first carry signal given by a preceding stage bit as a differential signal and two external input data (A1,B1) to be added at a present stage bit, for outputting addition data calculated on the basis of the first carry signal and the external input data as two differential signals, and further outputting a second carry signal to a succeeding bit as a differential signal indicative of whether a carry is generated by the present stage bit or not; and a latch type sense amplifier (16a) for outputting an addition result (SUM) of the present stage bit, after having differentially amplified and latched the addition data outputted by the calculation block. Since the addition operation is made on the basis of a minute potential difference (before amplification), it is possible to shorten the required charging time and to reduce the current consumption. In addition, since the sense amplifiers (16a) are provided with the latch function (18a), it is possible to control the differential amplification operation and the latch operation on the basis of a common sense amplifier activating signal (SAB), so that the number of elements can be reduced.

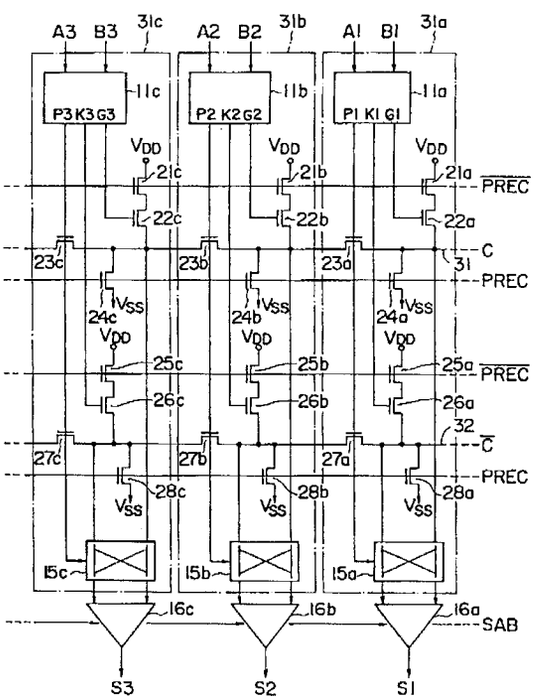

FIG. 2

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BACKGROUND OF THE INVENTION

The present invention relates to a full adder circuit, and more specifically to a full adder circuit for transmitting a carry signal differentially from a less significant bit full adder to a more significant bit full adder.

Fig. 1 shows an adder circuit related to the present invention, in which two carry signals are inputted from a preceding stage full adder as complementary differential carry signals; addition data is obtained on the basis of the carry signals and data to be added; and the other carry signals are transmitted to a succeeding stage full adder.

In more detail, the complementary carry signals Cin and /Cin are inputted from the preceding stage full adder to the present full adder. In this full adder, when the signal level of the carry signal Cin is higher than that of the carry signal /Cin, a carry is not generated to the succeeding stage bit. In contrast with this, when the signal level of the carry signal Cin is lower than that of the carry signal /Cin, a carry is generated to the succeeding stage bit. Between two input terminals for inputting the carry signals C and /C from the preceding stage bit and two output terminals for outputting the carry signals Cout and /Cout to the succeeding stage bit, two signal lines 131 and 133 are connected to transmit the carry signals, respectively. Between the two signal lines 131 and 133, two N-channel transistors 127 and 129 are provided as transfer gates of the signal lines.

Before operation, a precharge signal PREC is inputted to the gates of two N-channel transistors 137 and 139 to turn on these transistors, so that the signal lines 131 and 133 are precharged to a predetermined level. Further, the two signal lines 131 and 133 are equalized to the same potential through an N-channel transistor 142 also turned on in response to the precharge signal PREC. In the same way as above, the precharge signal PREC is inputted to the gate of an N-channel transistor 135 to turn on this transistor, so that the two input terminal for inputting the carry signals Cin and /Cin are equalized to the same potential through this N-channel transistor 135. After that, the transistors 137 and 139 are both turned off to execute the addition operation.

In the present stage bit, two data A and B are added. When both data are at the logical [1] level, a carry must be generated to the succeeding stage bit, irrespective of the carry signals Cin and /Cin applied by the lower significant bit. In this case, an EX-OR circuit 116 (to which two input data A and B are applied) outputs a logical [0] level signal to the gates of the N-channel transistors 127 and 129, so that these transistors are both turned off. As a result, the carry signals Cin and /Cin are both not transmitted to the succeeding stage bit.

The EX-OR circuit 116 and a NAND circuit 117 (to both of which the input data A and B are applied) output both a logical [0] level signal, respectively. These two logical [0] level signal of the circuits 116 and 117 and the logical [0] level signal of the precharge signal PREC are all inputted to a NAND circuit 120, so that the NAND circuit 120 outputs the logical [1] level signal. This signal is given to the gate of an N-channel transistor 123 to turn it on, with the result that the signal line 131 is discharged to a low potential Vss. In contrast with this, a NAND circuit 121 outputs a logical [0] level signal. This signal is given to the gate of an N-channel transistor 125 to turn it off, with the result that the signal line 133 is held at the precharged potential PREC. Therefore, the potential of the signal line 131 becomes lower than that of the signal line 133, so that the potential of the carry signal Cout becomes lower than that of the carry signal /Cout. As a result, a carry is generated to the succeeding stage bit.

On the other hand, when both data are at the logical [0] level, a carry is not generated to the succeeding stage bit, irrespective of the carry signals Cin and /Cin applied by the lower significant bit. In this case, the EX-OR circuit 116 (to which two input data A and B are applied) outputs a logical [0] level signal to the gates of the N-channel transistors 127 and 129, so that these transistors are both turned off. As a result, the carry signals Cin and /Cin are both not transmitted to the succeeding stage bit.

The EX-OR circuit 116 (to which the input data A and B are applied) outputs the logical [0] level signal. The NAND circuit 117 (to which the input data A and B are applied in the same way) outputs the logical [1] level signal. This signal is inverted to the logical [0] level signal by an inverter 119. These two logical [0] level signals of the circuits 116 and 117 and the logical [0] level signal of the precharge signal PREC are all inputted to the NAND circuit 121, so that the NAND circuit 121 outputs the logical [1] level signal. This signal is given to the gate of the N-channel transistor 125 to turn it on, with the result that the signal line 133 is discharged to a low potential Vss. In contrast with this, the NAND circuit 120 outputs a logical [0] level signal. This signal is given to the gate of the N-channel transistor 123 to turn it off, with the result that the signal line 133 is held at the precharged potential PREC. Therefore, the potential of the signal line 131 becomes higher than that of the signal line 133, so that the potential of the carry signal Cout becomes higher than that of the carry signal /Cout. As a result, a carry is not generated to the succeeding stage bit.

When the input data A and B are at the logical [0] level and [1] level, respectively or at the logical [1] level and [0] level, respectively, the carry signals Cin and /Cin applied by the less significant bit decide whether a carry must be generated or not to the succeeding stage bit. When the input data A and B are inputted to the EX-OR circuit 116, the logical [1] level signal is inputted to the gates of the N-channel transistors 127 and 129 to turn them on, respectively. Further, the logical [0] level signal is outputted from the two NAND circuits 120 and 121 to turn off both the N-channel transistors 123 and 125, respectively. As a result, the carry signals Cin and /Cin from the preceding stage bit are outputted, as they are, to the succeeding stage bit as the carry signals Cout and /Cout.

Further, the bits are added as follows: the output result of the EX-OR circuit 116 for inputting input data A and B and the amplified result of the preceding stage carry signal Cin and /Cin by a sense amplifier 113 are both inputted to an EX-OR circuit 118, and the logical operation result thereof is outputted to the outside as an addition data signal SUM OUT.

In the circuit shown in Fig. 1, the carry signals Cin and /Cin inputted from the preceding stage bit are minute-level differential signals and therefore the potential difference between the two is small. After having been amplified by the sense amplifier 113, a differential signal between the two signals Cin and /Cin are inputted to the EX-OR circuit 118 together with the input data A and B. In other words, the addition result can be obtained on the basis of the differential signal with a large amplitude amplified by the sense amplifier 113, without use of the minute-amplitude differential carry signals Cin and /Cin. Accordingly, there exists such a problem in that it takes time to charge and discharge the signal amplified by the sense amplifier, so that the operational speed decreases and simultaneously the current consumption increases.

In addition, the addition data signal SUM OUT outputted by EX-OR circuit 118 must be latched by a latch circuit (not shown) connected to an output terminal of the EX-OR circuit 118. Since this latch circuit is provided separately from the sense amplifier 113, another signal for deciding the latch timing is additionally required, thus causing another problem in that the number of the elements inevitably increases.

SUMMARY OF THE INVENTION

Accordingly, it is the object of the present invention to provide a full adder circuit which can increase the operational speed, decrease the current consumption, and further reduce the number of elements.

To achieve the above-mentioned object, the present invention provides a full adder circuit having a plurality of full adders each provided for each bit, each full adder comprising: a calculation block responsive to a first carry signal given by a preceding stage bit as a differential signal and two external input data to be added at a present stage bit, for outputting addition data calculated on the basis of the first carry signal and the external input data as two differential signals, and further outputting a second carry signal to a succeeding bit as a differential signal indicative of whether a carry is generated by the present stage bit or not; and a latch type sense amplifier for outputting an addition result of the present stage bit, after having differentially amplified and latched the addition data outputted by said calculation block.

When the addition is executed on the basis of the differential carry signals of large level difference obtained after having been sense-amplified as with the case of the above mentioned circuit related to the present invention, a long charging time and a large current consumption are required. In the present invention, however, since the addition is executed by the calculating block on the basis of the differential carry signals of minute level difference obtained before amplified by the sense amplifier, it is possible to increase the operational speed and decrease the current consumption. Further, since the addition result is amplified and further latched by the latch type sense amplifier, it is possible to reduce the number of the required elements, as compared to the case when the addition calculation is executed on the basis of the signals amplified by the sense amplifier and further the calculated result is latched by another latch circuit provided separately from the sense amplifier.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a circuit diagram showing a full adder circuit related to the present invention;

Fig. 2 is a circuit diagram showing an embodiment of the full adder circuit according to the present invention;

Fig. 3 is a circuit diagram showing an input block structure of the full adder circuit shown in Fig. 2;

Fig. 4 is a circuit diagram showing a switching circuit and a latch type sense amplifier circuit of the full adder circuit shown in Fig. 2;

Fig. 5 is a circuit diagram showing an example of a circuit for generating control signals used for the full adder circuit shown in Fig. 2; and

Fig. 6 is a timing chart showing the waveforms of various signals of the full adder circuit shown in Fig. 2.

DETAILED DESCRIPTION OF THE EMBODIMENTS

An embodiment of the full adder circuit according to the present invention will be described hereinbelow with reference to the attached drawings.

Fig. 2 shows a 3-bit full adder circuit of the present invention. A full adder circuit is composed of three calculation blocks 31a, 31b and 31c for obtaining an addition data and carry signals C and /C to be outputted to the succeeding stage bit, for each bit. To each calculation block 31a, 31b, or 31c, input data A1 and B1, A2 and B2, or A3 and B3 and carry signals C and /C of the preceding stage bit are inputted.

Further, each calculation block 31a (as an example of three blocks) is composed of an input block 11a; two N-channel transistors 21a and 22a for charging a signal line 31 for transmitting the carry signal C from the preceding stage bit to the succeeding stage bit; an N-channel transistor 23a (as a transfer gate) for activating or deactivating the signal line 31; an N-channel transistor 24a for charging the signal line 31; two N-channel transistors 25a and 26a for charging a signal line 32 for transmitting the carry signal /C from the preceding stage bit to the succeeding stage bit; an N-channel transistor 27a (as a transfer gate) for activating or deactivating the signal line 32; an N-channel transistor 28a for discharging the signal line 32; and a switching circuit 15a for executing EX-OR operation on the basis of a control signal P1 and carry signals C and /C (described later).

The input block 11a inputs the input data A1 and B1 (as described later), and generates control signals P1, K1 and G1, respectively. The operation of the transistors 23a and 27a is controlled on the basis of this control signal P1, respectively.

The N-channel transistor 21a is operated in response to a precharge signal /PREC applied to the gate thereof, and the N-channel transistor 22a is controlled in response to a control signal G1 outputted from the input block 11a to the gate thereof.

The N-channel transistor 24a is operated in response to a precharge signal PREC applied to the gate thereof.

The N-channel transistor 25a is operated in response to a precharge signal /PREC applied to the gate thereof, and the N-channel transistor 26a is controlled in response to a control signal K1 outputted from the input block 11a to the gate thereof.

The N-channel transistor 28a is operated in response to a precharge signal PREC applied to the gate thereof.

The switching circuit 15a switches the outputs of the carry signals C and /C on the basis of the control signal P1 given by the input block 11a, as described above, and executes EX-OR operation necessary for addition operation. The output of the switching circuit 15a corresponds to the addition data of the present bit. This addition data is a differential signal having a minute potential difference. This signal is inputted to a latch type sense amplifier 16a, differentially amplified to a necessary level, and then outputted as an addition data signal S1. Further, this latch type sense amplifier 16a is also provided with such a function as to latch the addition data signal S1 in response to the sense amplifier activation signal SAB.

Other calculation blocks 31b and 31c are basically the same as the calculation block 31a described above, so that any detailed description thereof is omitted herein,

The operation of the calculation block 31a and the latch type sense amplifier 16a shown in Fig. 2 will be described hereinbelow.

Prior to the addition operation of each bit, the signal lines 31 and 32 for transmitting the carry signals C and /C are precharged. The precharge signal PREC is set to the logical [1] level, and the signals lines 31 and 32 are both discharged to the logical [0] level. After precharge, the precharge signal PREC is set to the logical [0] level, and the precharge signal /PREC is set to the logical [1] level.

Here, the input data A1 and B1 are inputted to the input block 11a. Fig. 3 shows the circuit construction of this input block 11a, In Fig. 3, input data A1 and B1 are inputted to an EX-OR circuit 12a, a NOR circuit 13a, and an AND circuit 14a, respectively, to output the control signals P1, K1 and G1, respectively.

In the case where the input data A1 and B1 are at the logical [1] level and [0] level, respectively or at the logical [0] level and [1] level, respectively, the logical [1] level control signal P1 is outputted by only the EX-OR circuit 12a. Therefore, the N-channel transistors 23a and 27a are turned on, so that the carry signals C and /C transmitted from the preceding stage bit are transmitted, as they are, to the succeeding stage bit through the signal lines 31 and 32, respectively.

When the input data A1 and B1 are both at the logical [1] level, it is necessary to generate a carry to the succeeding stage bit, irrespective of the carry signals C and /C of the preceding stage bit. In this case, only the AND circuit 14a outputs the logical [1] level control signal G1. This control signal G1 is inputted to the gate of the N-channel transistor 22a to turn it on, so that the signal line 31 is charged in cooperation with the N-channel transistor 21a turned on in response to the logical [1]

level precharge signal /PREC applied to the gate thereof. Since the N-channel transistor 26a is turned off by the logical [0] level control signal K1, the signal line 32 is not charged. Accordingly, the level of the carry signal C is higher than that of the carry signal /C.

As a result, the carry signals C and /C indicative of a carry are outputted to the succeeding stage bit.

When the input data A1 and B1 are both at the logical [0] level, a carry is not generated, irrespective of the carry signals C and /C of the preceding stage bit. In this case, only the NOR circuit 13a outputs the logical [1] level control signal K1. This control signal K1 is inputted to the gate of the N-channel transistor 26a to turn it on, so that the signal line 32 is charged in cooperation with the N-channel transistor 25a turned on in response to the logical [1] level precharge signal /PREC applied to the gate thereof. Since the N-channel transistor 22a is turned off by the logical [0] level control signal G1, the signal line 31 is not charged. Accordingly, the level of the carry signal /C is higher than that of the carry signal C.

As a result, the carry signals C and /C indicative of no carry are outputted to the succeeding stage bit.

The same operation as above is executed in the other calculation blocks 31b and 31c, respectively.

Here, it is necessary to determine the sizes of the N-channel transistors 21a to 21c, 22a to 22c, 23a to 23c, 24a to 24c all connected to the signal line 31, and the sizes of the N-channel transistors 25a to 25c, 26a to 26c, 27a to 27c, 28a to 28c all connected to the signal line 32, under consideration of the following points:

In the case of the signal line 31, for example, the level of the carry signal C transmitted to the signal line 31 is minimized when the carry signal C generated and outputted by the least significant bit is transmitted to the most significant bit via all the N-channel transistors 23a, 23b, 23c, ... Therefore, it is necessary to determine the dimensions of the transistors 21a to 21c, 22a to 22c, 23a to 23c, so that the carry signal of the minimum level can be sensed by the sense amplifier for the least significant bit (in other words, the sizes of the transistors must be large enough to transmit the carry signal without excessively reducing the potential level of the carry signal). These transistor dimensions are related to the required operational speed. That is, when a high speed operation is required, the carry signal must be sensed at early timing in the process during which the signal line 31 is charged by the transistors 21a to 21c and 22a to 22c and thereby the potential thereat increases. Therefore, it is necessary to determine the dimensions of the transistors to be large enough. Further, the size of the transistor 24a must be determined in such a way that the precharge can be completed within the precharge cycle.

Here, the operation of the carry signals C and /C whose levels have been decided, the switching circuit 15a for executing the EX-OR operation on the basis of the control signal P outputted by the input block 11a, and the latch type sense amplifier 16a will be described hereinbelow. The switching circuit 15a and the latch type sense amplifier 16a are constructed as shown in Fig. 4.

The switching circuit 15a is composed of N-channel transistors N1 and N3 to each gate of which the control signal /P1 is inputted, and N-channel transistors N2 and N4 to each gate of which the control signal P1 is inputted. The carry signal /C is inputted to one end of the N-channel transistor N1, and the carry signal C is inputted to one end of the N-channel transistor N2. The other ends of both the N-channel transistors N1 and N2 are connected to the gate of a P-channel transistor P3 of the latch type sense amplifier 16a. In the same way as above, the carry signal C is inputted to one end of the N-channel transistor N3, and the carry signal /C is inputted to one end of the N-channel transistor N4. The other ends of both the N-channel transistors N3 and N4 are connected to the gate of a P-channel transistor P2 of the latch type sense amplifier 16a. When the control signal P1 is at the logical [1] level, (the signal /P is at the logical [0] level), the N-channel transistors N2 and N4 are both turned on. Therefore, the carry signal C is inputted to the gate of the P-channel transistor P3, and the carry signal /C is inputted to the gate of the P-channel transistor P2. In contrast with this, when the control signal P1 is at the logical [0] level, (the signal /P is at the logical [1] level), since the input conditions are switched, the carry signal /C is inputted to the gate of the P-channel transistor P3, and the carry signal C is inputted to the gate of the P-channel transistor P2.

The latch type sense amplifier 16a is provided with P-channel transistors P1 to P6, a current mirror type differential amplifier circuit composed of N-channel transistors N5 to N10, and a latch circuit 18a composed of two NOR circuits NR1 and NR2. The latch type sense amplifier 16a operates on the basis of the sense amplifier activating signal SAB inputted to the gate of the N-channel transistors N7 to N10. In other words, when the signal SAB is at the logical [1] level, the precharge is executed, so that the N-channel transistors N7 to N10 are turned on and thereby nodes N11 and N12 corresponding to the output terminals of the differential amplifier circuit are fixed to a ground potential Vss. When the signal SAB changes to the logical [0] level, since the N-channel transistors N7 to N10 are all

turned off, the sensing operation and the latch operation are both executed.

The carry signals C and /C are inputted from the switching circuit 15a to the latch type sense amplifier 16a, and then amplified differentially to decide both the levels of the output nodes N11 and N12. These levels at the output nodes N11 and N12 are inputted to the latch circuit 18a, so that the addition data signal SUM can be outputted through an output terminal of the latch circuit 18a.

In more practical, when the control signal P1 is at the logical [1] level (the signal /P1 is at the logical [0] level), the carry signal C is inputted to the gate of the P-channel transistor P3, and the signal /P is inputted to the gate of the P-channel transistor P2. Here, if the carry signal C is at the logical [1] level, (the signal /C is at the logical [0] level), the P-channel transistor P3 is turned off and the P-channel transistor P2 is turned on. In this case, the P-channel transistor P6 and N-channel transistor N5 are turned on, and the P-channel transistor P5 and N-channel transistor N6 are turned off. As a result, the output node N12 is at the logical [0] level and the output node N11 is at the logical [1] level, so that latch circuit 18a outputs a logical [0] level addition data signal SUM.

Here, the sense amplifier activating signal SAB and the precharge signal PREC are both generated by a clock signal CLOCK. Fig. 4 shows an example of the circuit for generating the sense amplifier activating signal SAB and the precharge signal PREC on the basis of the clock signal CLOCK. The circuit is composed of inverters IN11 to IN16, delay inverters DI11 to DI17, a NOR circuit NR11 and an AND circuit AN11.

Further, Fig. 6 shows a timing chart of the sense amplifier activating signal SAB and the precharge signal PREC both generated by the circuit shown in Fig. 5 in response to the clock signal CLOCK. Further, Fig. 6 shows the respective levels of the input data A1 and B1, the carry signals C and /C, and the addition data signal SUM, respectively.

With reference to Fig. 6, when the clock signal CLOCK rises, the precharge signal PREC also rises, so that the signal lines 31 and 32 are both precharged to ground potential Vss in Fig. 2. After that, when the precharge signal PREC falls, the difference between the two carry signals C and /C is calculated. Therefore, the relative potential difference between the two carry signals C and /C transmitted through the two signal lines 31 and 32 increases gradually as shown in Fig. 6.

In the succeeding cycle, when the clock CLOCK rises and the precharge signal PREC falls, the signal lines 31 and 32 are precharged again. At this time, the carry signals C and /C obtained by simultaneous calculation are inputted to the latch type sense amplifier 16a via the switching circuit 15a.

At the timing when the clock signal CLOCK rises and further the sense amplifier activating signal SAB drops to the logical [0] level, the latch type sense amplifier 16a amplifies the two inputted carry signals C and /C and latches the amplified signals. After the addition data SUM has been latched, the sense amplifier activating signal SAB rises to the logical [1] level, so that the latch type sense amplifier 16a is precharged. Further, the precharge signal PREC changes to the logical [1] level to precharge the signal lines 31 and 32, for the succeeding calculation.

In the embodiment as described above, the following effects can be obtained: In the circuit as shown in Fig. 1, after the minute differential carry signals C and /C have been amplified by the sense amplifier 113 to obtain a differential signal with a large level difference between the two, the differential carry signal is applied from the sense amplifier 113 to the EX-OR circuit 118 for addition operation. Therefore, a relatively long charge time is required and a relatively large current is consumed. In addition, the circuit for latching the addition result is provided separately from the sense amplifier, so that the number of the elements is large.

In contrast with this, in the circuit as shown in Fig. 2, the addition operation is executed by use of the carry signals C and /C of small difference level (before being amplified by the latch type sense amplifiers 16a to 16c). After that, the addition data outputted by the switching circuits 15a to 15c are inputted to the latch type sense amplifiers 16a to 16c to amplify the level thereof up to a required level. As described above, in the circuit according to the present invention, since the addition operation is made on the basis of the carry signals C and /C of a minute potential difference (obtained before being amplified by the sense amplifier), it is possible to shorten the required charging time and to reduce the current consumption. In addition, since the sense amplifiers 16a to 16c are provided with the latch function, respectively, it is possible to control the differential amplification operation and the latch operation on the basis of the common signal SAB, so that the number of elements can be reduced.

The embodiment of the full adder circuit according to the present invention has been explained only by way of example That is, the circuits shown in Figs. 2 to 5 are explained by way of examples, so that various modifications can be made without being limited to only those shown.

Further, in the timing chart shown in Fig. 6, the timing is so determined that after the latch operation of the latch type sense amplifiers 15a to 15c has been completed on the basis of the sense

amplifier activating signal SAB, the signal lines 31 and 32 are precharged on the basis of the precharge signal PREC. However, when a higher speed operation is needed, it is also possible to start the precharge operation for the signal lines 31 and 32, before the latch operation of the latch type sense amplifiers 15a to 15c ends completely. In this case, in Fig. 5, for instance, the node ND2 connected to the output terminal of the inverter IN14 is connected to the output terminal of the delay inverter DI12. By this connection, the precharge signal PREC can rise, before the sense amplifier activating signal SAB rises.

Claims

1. A full adder circuit having a plurality of full adders each provided for each bit, each full adder comprising:

a calculation block responsive to a first carry signal given by a preceding stage bit as a differential signal and two external input data to be added at a present stage bit, for outputting addition data calculated on the basis of the first carry signal and the external input data as two differential signals, and further outputting a second carry signal to a succeeding bit as a differential signal indicative of whether a carry is generated by the present stage bit or not; and

a latch type sense amplifier for outputting an addition result of the present stage bit, after having differentially amplified and latched the addition data outputted by said calculation block.

2. The full adder circuit of claim 1, wherein said calculation block comprises:

an input block responsive to the external input data, for generating and outputting first and second control signals;

a pair of carry signal lines provided between respective full adders, for applying the first carry signal generated at the preceding stage bit to the present bit and transmitting the second carry signal generated at the present bit to the succeeding stage bit;

precharging means responsive to external precharge signals, for precharging a pair of said carry signal lines to a predetermined potential, respectively;

second carry signal generating means responsive to the first control signal, for generating the second carry signal, after a pair of said carry signal lines have been precharged;

a transfer gate responsive to the second control signal, for turning on or off a pair of said carry signal lines, to transmit the first carry signal to the succeeding stage bit as the second carry signal in the case that a pair of said carry signal lines are turned on; and

a switching circuit responsive to the second carry signal and the second control signal, for switching outputs of the second carry signal on the basis of the second control signal, to output the addition data.

3. The full adder circuit of claim 2, wherein said input block applies:

when the external input data do not match in logical level, the second control signal to said transfer gate so that a pair of said carry signal lines can be turned on;

when the input data are both at a first logical level, the second control signal to said transfer gate so that a pair of said carry signal lines can be turned off, and further the first control signal to said second carry signal generating means so that the second carry signal is set to the first logical level; and

when the input data are both at a second logical level, the second control signal to said transfer gate so that a pair of the carry signal lines can be turned off, and further the first control signal to said second carry signal generating means so that the second carry signal is set to the second logical level; and

wherein said switching circuit executes exclusive OR calculation by switching a relative potential difference between a pair of said carry signal lines according to match or mismatch of the external input data, and applies the calculation result to said latch type sense amplifier as the addition data.

4. The full adder circuit of claim 2, wherein said input block comprises;

an AND circuit and a NOR circuit responsive to the external input data, for executing logical sum operation and logical product operation to output the first control signal as the differential signal; and

an EX-OR circuit responsive to the external input data, for executing exclusive logical sum operation to output the second control signal;

wherein said second carry signal generating means comprises two charging transistors provided for a pair of aid carry signal lines respectively and responsive to control signals outputted by said AND circuit and said NOR circuit to respective gates thereof respectively, for controlling charging operation of a pair of said carry signal lines; and

wherein said transfer gate comprises two gate transistors provided for a pair of said

carry signal lines respectively and responsive to the second control signal outputted by said EX-OR circuit to respective gates thereof, for controlling turn-on or turn-off operation of said transfer gate.

5. The full adder circuit of claim 4, wherein sizes of the two charging transistors of said second carry signal generating means and sizes of the two transistors of said transfer gate are so determined that when the first carry signal generated by the least significant bit is transmitted to the most significant bit as it is, said latch type sense amplifier at the least significant bit stage full adder can sense this first carry signal.

6. The full adder circuit of claim 2, wherein said latch type sense amplifier comprises:

a current mirror type differential amplifier circuit, responsive to a sense amplifier activating signal, for differentially amplifying the addition data and outputting the addition result of the present stage bit, and

a latch circuit responsive to the sense amplifier activating signal, for latching the outputted addition result and outputting the latched addition result to the outside.

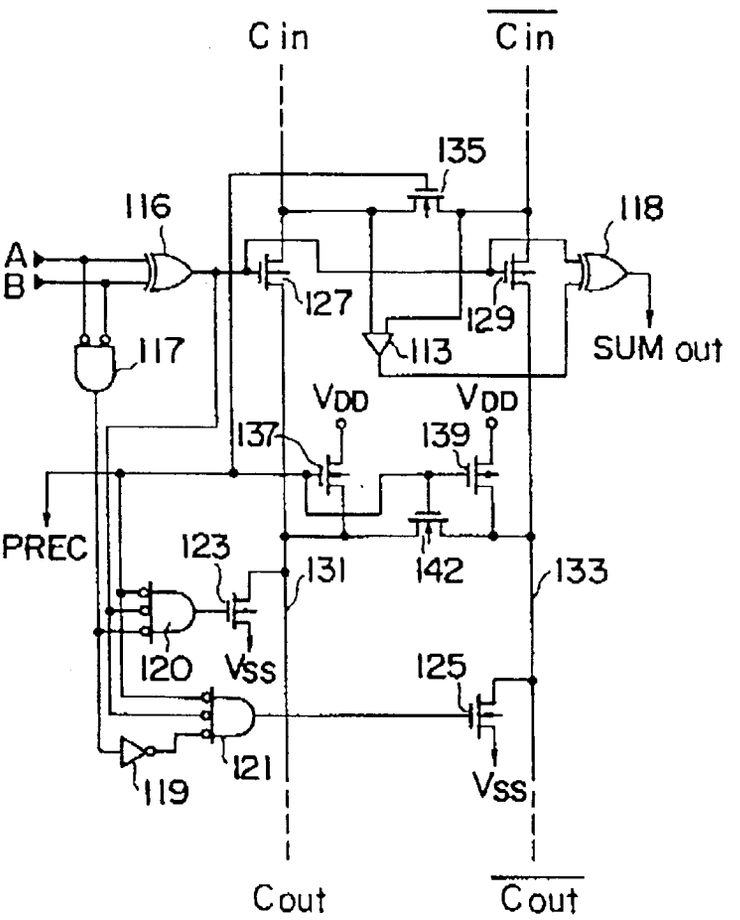
Cin
$\overline{Cin}$
135
116
118
A
B
127
129
117
113
SUM out
VDD
VDD
137
139
PREC
123
131
142
133
120
Vss
125
121
119
Vss
Cout
$\overline{Cout}$

FIG. 1

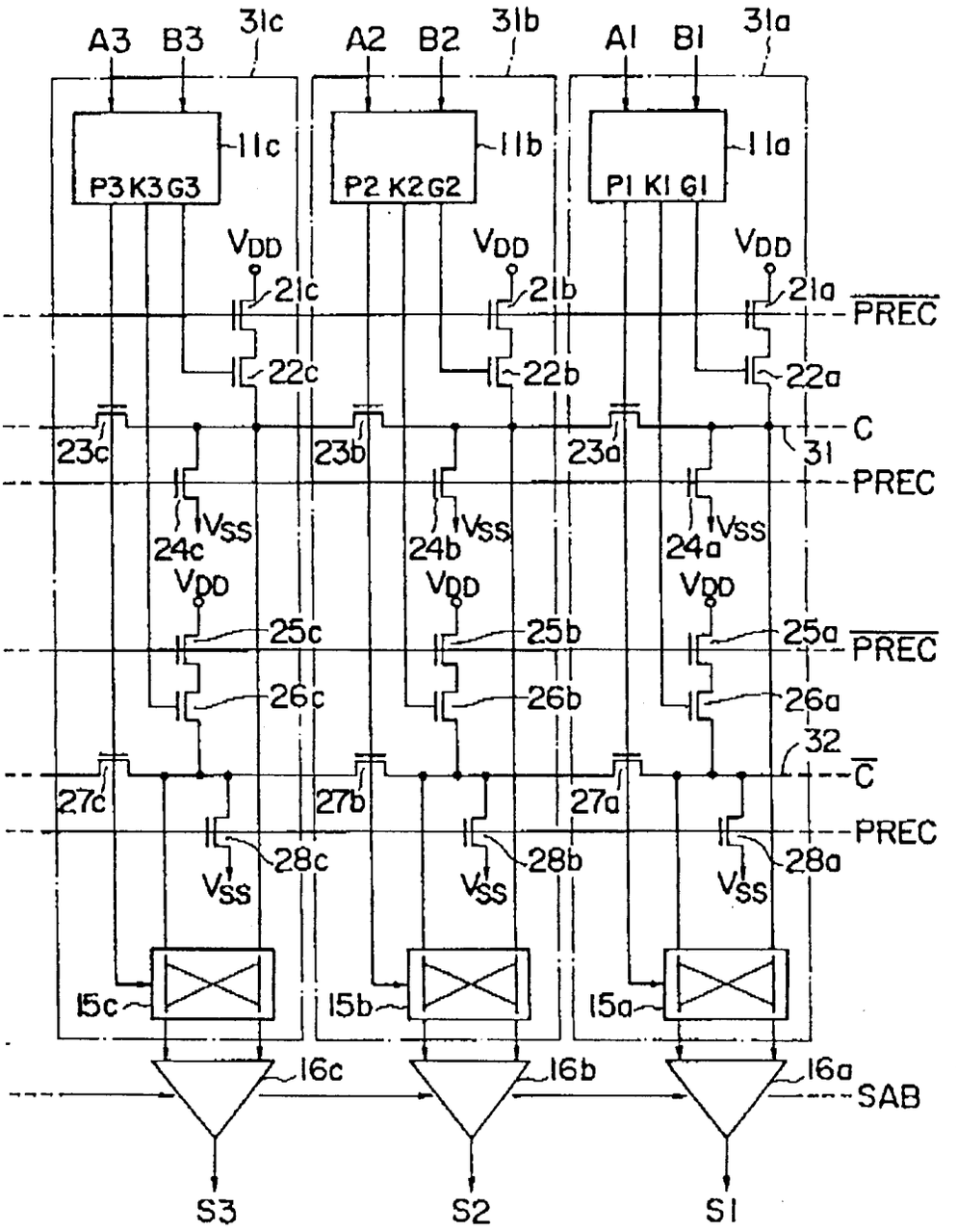
A3
B3
31c
A2
B2
31b
A1
B1
31a
11c
P3 K3 G3
11b
P2 K2 G2
11a
P1 K1 G1
VDD
21c
21b
21a
PREC
22c
22b
22a
C
23c
23b
23a
31
PREC
24c
24b
24a
Vss
VDD
25c
25b
25a
PREC
26c
26b
26a
32
C
27c
27b
27a
PREC
28c
28b
28a
Vss
15c
15b
15a
16c
16b
16a
SAB
S3
S2
S1

FIG. 2

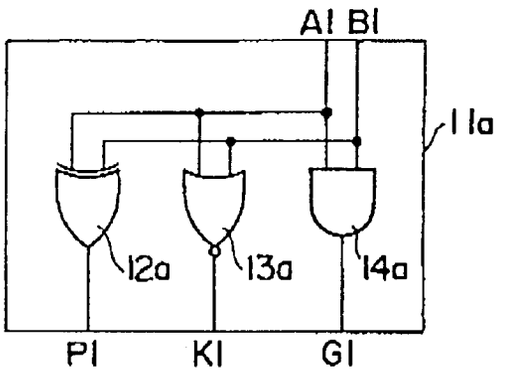
A1 B1
11a
12a
13a
14a
P1
K1
G1

FIG. 3

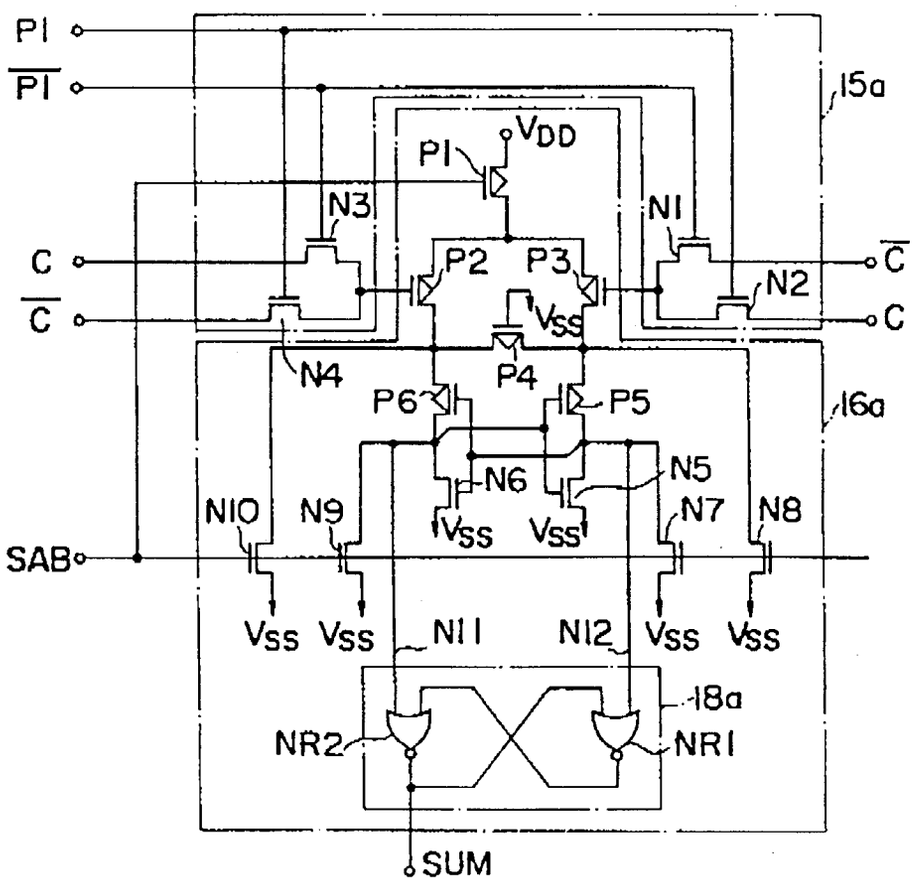
P1
P1
15a
VDD
P1
N3
N1
C
C
P2
P3
N2
C
C
Vss
N4
P4
P6
P5
16a
N6
N5
N10
N9
Vss
Vss
N7
N8
SAB
Vss
Vss
N11
N12
Vss
Vss
18a
NR2
NR1
SUM

FIG. 4

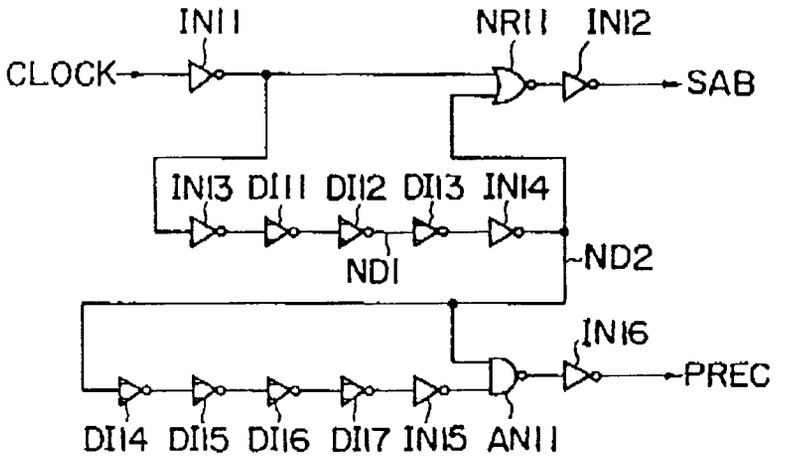
IN11
NR11
IN12
CLOCK
SAB
IN13
DI11
DI12
DI13
IN14
ND1
ND2
IN16
PREC
DI14
DI15
DI16
DI17
IN15
AN11

FIG. 5

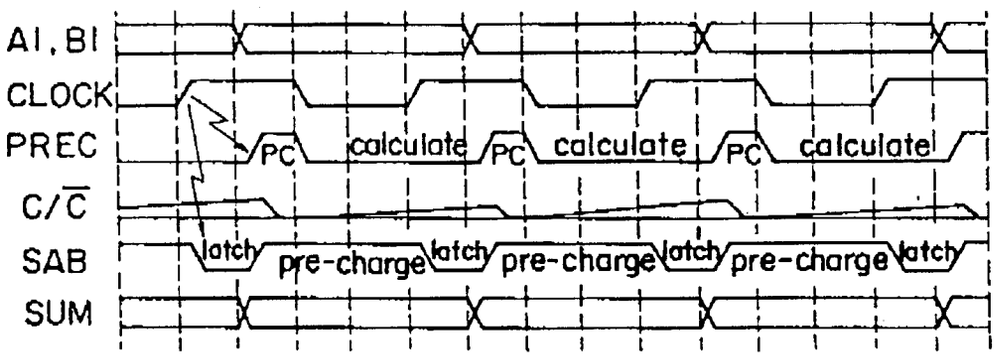
AI, BI
CLOCK
PREC
C/C̄
SAB
SUM
PC
calculate
PC
calculate
PC
calculate
latch
pre-charge
latch
pre-charge
latch
pre-charge
latch

FIG. 6

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 94 11 5592

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	PATENT ABSTRACTS OF JAPAN vol. 14, no. 500 (P-1125) 31 October 1990 & JP-A-02 206 831 (MITSUBISHI ELECTRIC CORP) 16 August 1990 * abstract * ---	1	G06F7/50
A	GB-A-2 069 785 (PHILIPS) * page 4, left column, line 11 - page 5, left column, line 3; figures 5-7 * ---	1-5	
A	WO-A-85 04965 (MOTOROLA) -----		

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

G06F

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	4 January 1995	Verhoof, P

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
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D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

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