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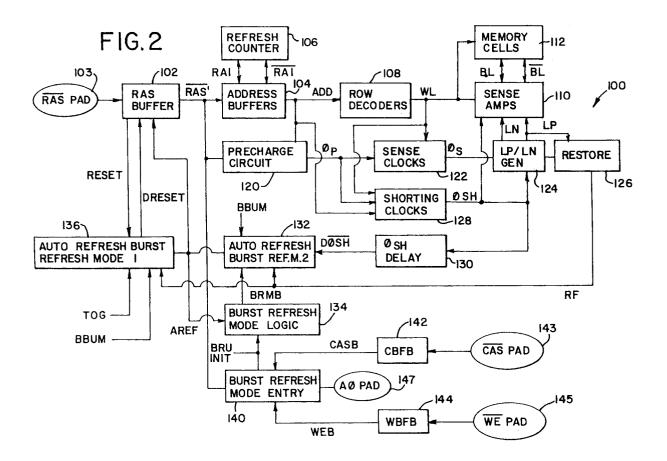
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## <sup>54</sup> Burst refresh mode for DRAMs.

© Burst refresh mode circuitry is provided for a memory (100) having cells (112) in rows and columns, sense amplifiers (110) and Latch N/Latch P driver circuitry (124), a RAS buffer (102), refresh counters (106), address buffers (104), row decoders (108), precharge circuitry (120) producing shorting clocks (128), and a refresh detector circuit coupled to the Latch P circuitry to provide a restore finished (RF) signal indicative that a refresh cycle is substantially completed. Burst refresh mode entry circuitry (140) detects proper conditions for entering burst

refresh mode. An auto-refresh burst refresh mode circuit (136) causes the RAS buffer (102) to generate a new internal RAS signal. Burst refresh mode logic (134) has counters to count the number of rows that have been refreshed. The system self-times the refreshing by responding to the restore finished signal. A delay circuit (130) interposes a short delay for the precharge before another row is automatically refreshed in the burst refresh mode. Battery back-up mode circuitry (132) is partially disabled.





## **EUROPEAN SEARCH REPORT**

Application Number EP 94 11 4186

ategory	Citation of document with in of relevant pas		Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.CL6)
A	US-A-4 984 209 (RAJ	ARAM ET AL.)	1,11,14, 17,19	G11C11/406
		- column 7, line 29;		
A	EP-A-0 307 945 (WAN	G LABORATORIES INC)	1,11,14, 17,19	
	* abstract * * page 7, line 9 -   figures 7,8 *	page 7, line 56;		
				TECHNICAL FIELDS SEARCHED (Int.Cl.6)
				G11C
	The present search report has be	<u> </u>		
THE HAGUE		Date of completion of the search  14 June 1995	Examiner Stecchina, A	
CATEGORY OF CITED DOCUMENTS T: theor E: earlie X: particularly relevant if taken alone after			y or principle underlying the invention er patent document, but published on, or the filing date ment cited in the application ment cited for other reasons	

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