



(12) **EUROPEAN PATENT APPLICATION**

(21) Application number : **94114202.8**

(51) Int. Cl.⁶ : **G05F 1/56**

(22) Date of filing : **09.09.94**

(30) Priority : **28.10.93 US 142035**

(43) Date of publication of application :
03.05.95 Bulletin 95/18

(84) Designated Contracting States :
DE FR GB

(71) Applicant : **ROCKWELL INTERNATIONAL CORPORATION**
2201 Seal Beach Boulevard
Seal Beach California 90740 (US)

(72) Inventor : **Gupta, Rajiv (NMI)**
1776 Moorpark Drive
Brea, California 92621 (US)
 Inventor : **Spence, John R.**
18141 Stratford Circle
Villa Park, California 92667 (US)
 Inventor : **Zhang, Ming Ming**
2 Stanford Court
Irvine, California 29715 (US)

(74) Representative : **Wagner, Karl H. et al**
WAGNER & GEYER
Patentanwälte
Gewürzmühlstrasse 5
D-80538 München (DE)

(54) **CMOS on-board voltage regulator.**

(57) A voltage regulator for regulating the voltage at a predetermined node connected to the core of a semiconductor device comprising reference voltage means for generating a reference voltage, an op-amp having said reference voltage as its reference input and the voltage at said predetermined node as its another input for adjusting the node voltage to match said reference voltage, series dropping means for supplying current load to the core, and filter capacitor coupled to said series dropping means for supplying transient current to said predetermined node.

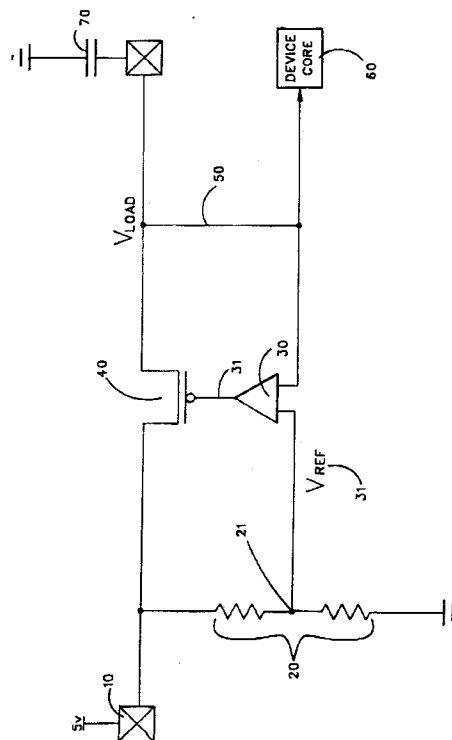


FIG. 1

BACKGROUND OF THE INVENTION

The present invention relates to voltage regulators and more specifically to on-board voltage regulators for semiconductor devices.

Electronic products, such as notebook computers, have become more portable in size due to advances in VLSI and semiconductor processing technology. With this trend, it has become quite desirable, if not entirely essential, to have components of those devices operating with less power consumption. Recently, the operating voltage for those on-board devices and components have been reduced from 5 volt to 3 volt, as technology has made low power applications possible and cost effective. However, the external environment, e.g. I/O and peripherals, of the components and chips still operate the interface at 5 volt level. Therefore, it has become desirable to maintain a 5 volt supply for interface with the external environment of a semiconductor device, while providing a 3 volt operating voltage to the core of the device. The semiconductor device would thus consume less power at the core without any impact on its external compatibility.

Voltage regulators are well known in the art. However, the present invention is capable of providing reduced voltage supply to the "core" of a semiconductor device for reduced power consumption when integrated on-board with the semiconductor device. A semiconductor device with this capability will thus be able to remain compatible with its external components and environment.

SUMMARY OF THE INVENTION

Therefore, it is an object of the present invention to provide a reduced operating voltage to the core of a semiconductor device for low power applications.

It is also an object of the present invention to provide a reduced operating voltage while maintaining a 5 volt level with the periphery of the device.

It is further an object of the present invention to integrate the reduced operating voltage supply with the semiconductor device without substantial increase in the silicon usage.

A voltage regulator for regulating the voltage supply to the core of a semiconductor device is disclosed. The voltage regulator comprises a reference voltage generator for generating a reference voltage based on the supply source, an operational amplifier for comparing the core voltage with the reference voltage, a series dropping PFET for maintaining the core voltage at the reference voltage level as its gate is operated by the output of the op-amp, and an external filter capacitor coupled to the core voltage node to supply transient current and hence stability during switching

BRIEF DESCRIPTION OF THE DRAWINGS

Further objects of the present invention will become apparent in the following description, wherein:

Figure 1 is a circuit diagram of the preferred embodiment of the present invention.

Figure 2 is a simplified block diagram to graphically illustrate the placement of the present invention.

Figure 3 is a circuit diagram of the op-amp used in connection with the preferred embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

A voltage regulator is disclosed for use with on-board low operating supply voltage. While the following description makes reference to specific circuits, transistors, electronic elements, etc., it should be apparent to those skilled in the art that their equivalents are readily available for achieving the same objectives according to the present invention.

With reference to Fig. 1, an on-board voltage regulator according to the present invention is disclosed. As shown in Figure 1, N-well resistor divider 20 is connected to a typical 5 volt supply 10 to generate a 3.3 volt reference voltage Vref 31 at node 21. Vref 31 is also connected to reference input of op-amp 30. It should be apparent to those skilled in the art that node 21, which is nominally at 3.3 volt, can be adjusted to other levels of reference voltage for their intended purposes. Load voltage for device core 60 is at node 50, which is connected to the other input terminal of op-amp 30. The output 31 of op-amp 30 is connected to the gate of a P-channel field effect transistor ("PFET") 40. The two ends of PFET 40 are connected to the 5 volt supply 10 and node 50. External capacitor 70 is connected to node 50 for filtering and supplying transient current during switching cycles. Capacitor 70 is "external" in that it is currently implemented outside of the integrated voltage regulator circuit, as is illustrated in Figure 2.

Figure 2 is a graphical representation of voltage regulator 100 relative to external filter capacitor 120. While voltage regulator 100 supplies, via V-load 150, core 110, capacitor 120 is connected to V-load 150 through pin 121. A 5 volt power supply is drawn from pin 140, which can supply I/O strip 130. Accordingly, device core 110 can be operated at 3.3 volt, while the periphery and I/O operating at 5 volt.

The operation of the voltage regulator according to the present invention will now be described with reference back to Figure 1. Vref 31 for op amp 30 is generated by N-well resistor divider 20 using 5 volt supply 10. V-load at node 50 is regulated by op-amp 30, which compares V-load at node 50 to match Vref 31 by turning ON and OFF PFET 40, which is a series dropping device, supplying the required current load to device core 60. PFET 40, as will be understood by

those skilled in the art, is properly sized to suit the intended current load requirement.

Also, PFET 40 serves to control the current flow to node 50. When V-load exceeds Vref 31, op amp 30 turns ON and thus turning PFET 40 into the direction of OFF. When V-load is below Vref 31, the OFF state of op amp 30 turns PFET 40 in the direction of ON to supply the current load required for device core 60.

External capacitor 70 is used for supplying transient current and filters load demand to avoid part failure due to VDD droop during switching. By implementing capacitor 70 externally, valuable silicon usage on the device can thus be optimized.

Figure 3 is a circuit diagram of op amp 30 as it is currently implemented. It is a conventional circuit as will be appreciated by those skilled in the art.

Claims

1. A voltage regulator for regulating the voltage at a predetermined node connected to the core of a semiconductor device, comprising:
reference voltage means for generating a reference voltage;
an op-amp having said reference voltage as its reference input and the voltage at said predetermined node as its another input, said op-amp adjusting the node voltage to match said reference voltage;
series dropping means for supplying current load to the core, said series dropping means, responsive to the output of said op-amp, increasing the voltage at said node until the voltage matches said reference voltage;
filter capacitor coupled to said series dropping means for supplying transient current to said predetermined node.
2. A voltage regulator according to claim 1, wherein said reference voltage means comprises a voltage divider using the supply voltage to generate said reference voltage for said op-amp.
3. A voltage regulator according to claim 2, wherein said voltage divider comprises an N-well resistor divider.
4. A voltage regulator according to claim 1, wherein said series dropping means comprises a P-channel field-effect transistor having one end of its path of conductance to the power supply and the other end to said node, the gate of said PFET coupled to received the output from said op-amp.
5. A voltage regulator according to claim 3, wherein said series dropping means comprises a P-channel field-effect transistor having one end of its

path of conductance to the power supply and the other end to said node, the gate of said PFET coupled to received the output from said op-amp.

6. A voltage regulator according to claim 1, wherein said reference voltage means, said op-amp, and said series means are integrated on board with the core of the semiconductor device and said filter capacitor is implemented external to the semiconductor device.
7. A voltage regulator for regulating the voltage at a predetermined node connected to the core of a semiconductor device, said semiconductor device being powered by a supply voltage, comprising:
N-well resistor divider coupled to said supply voltage for generating a reference voltage;
an op-amp having said reference voltage as one of its input and the voltage at said predetermined node as its other input, said op-amp adjusting the voltage at said node to match said reference voltage;
series dropping P-FET having its gate coupled to receive the output from said op-amp, one end of its path of conductance being coupled to said supply voltage and the other end of said path being coupled to said predetermined node such that the two ends are conducting when said gate is caused to turn OFF by said output from said op-amp;
external filter capacitor coupled to said predetermined node for supplying transient current to said predetermined node.
8. A voltage regulator for regulating the voltage at a semiconductor device, comprising:
reference voltage means for generating a reference voltage;
filter capacitor coupled to said series dropping means.

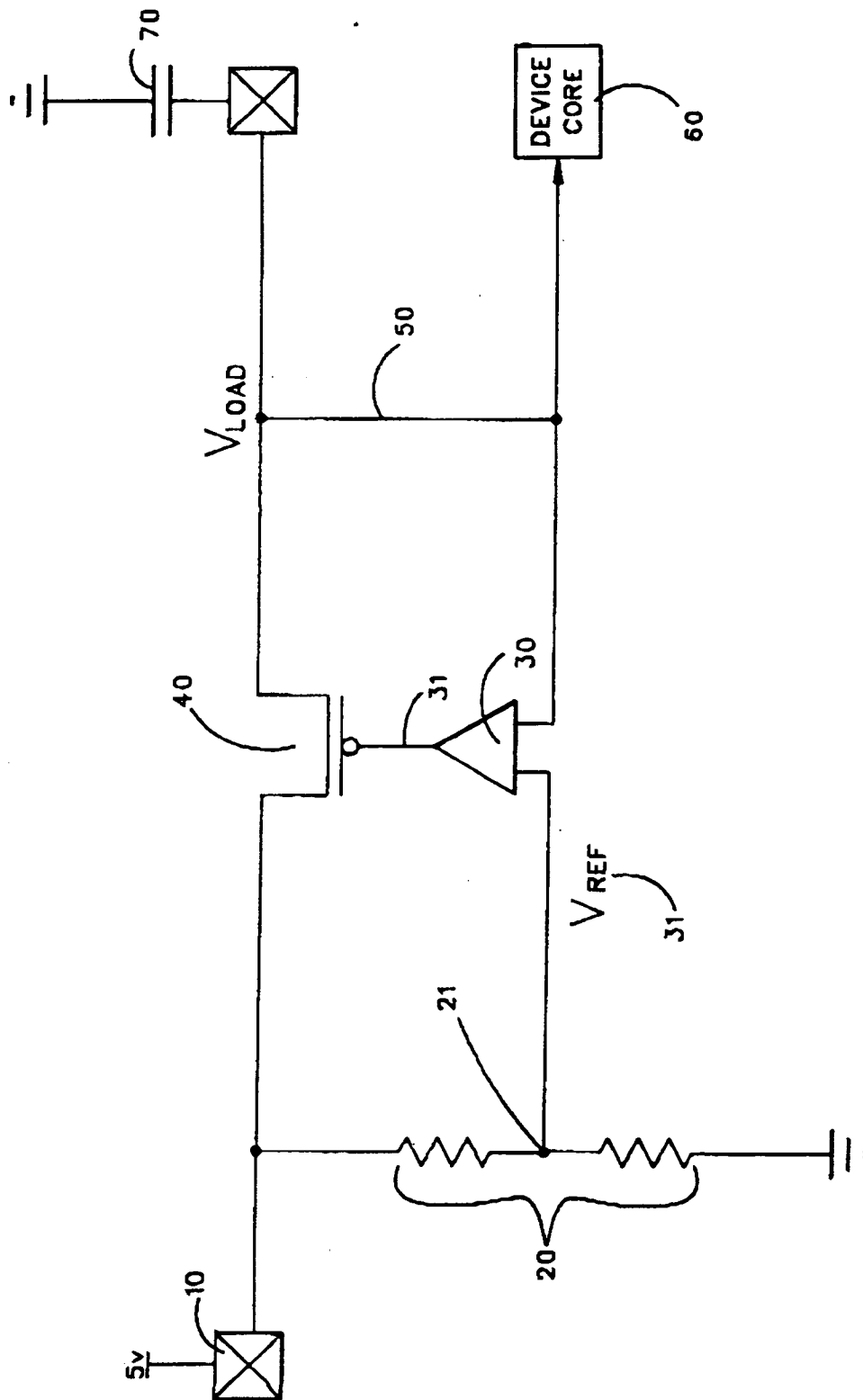


FIG. 1

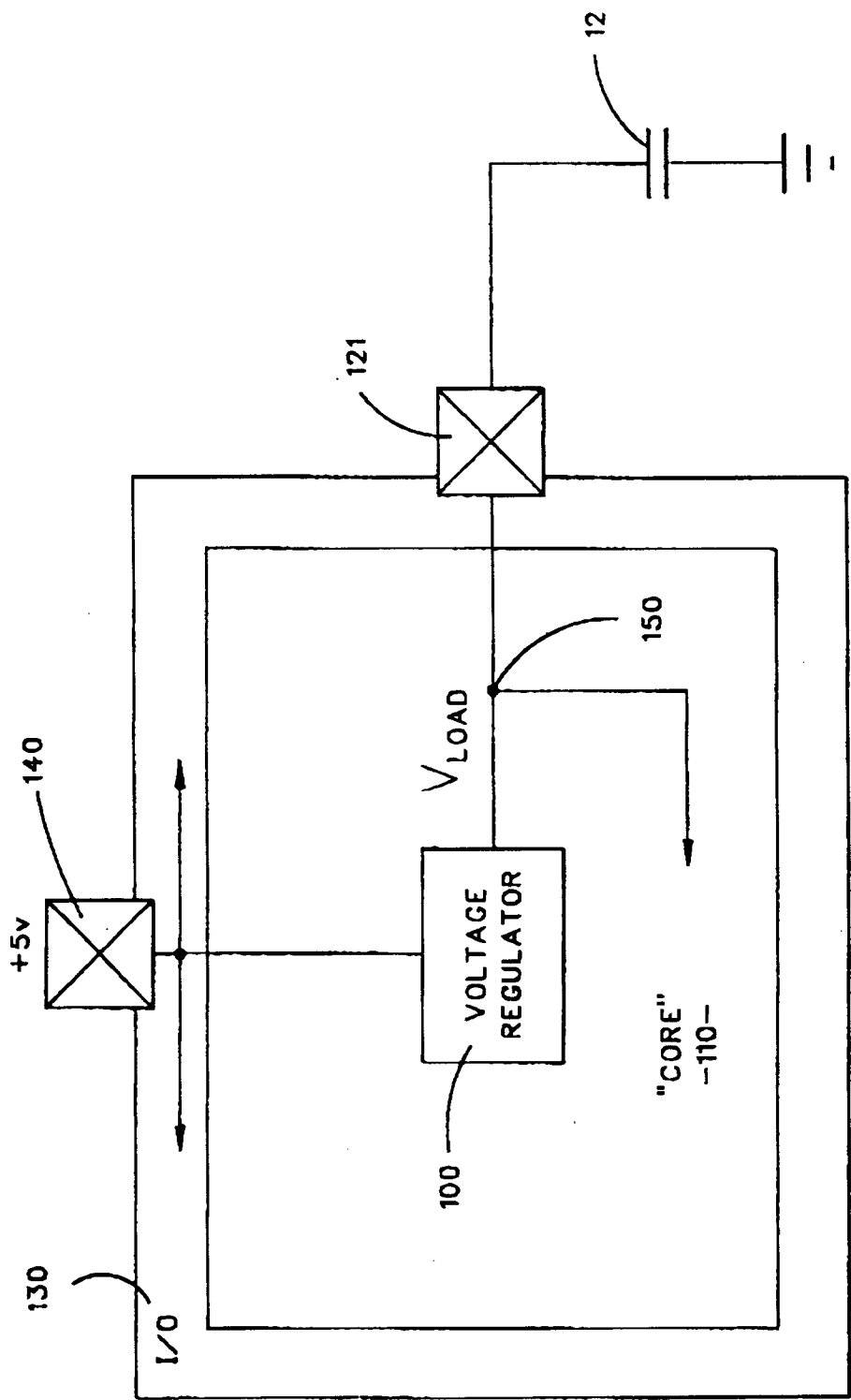


FIG. 2

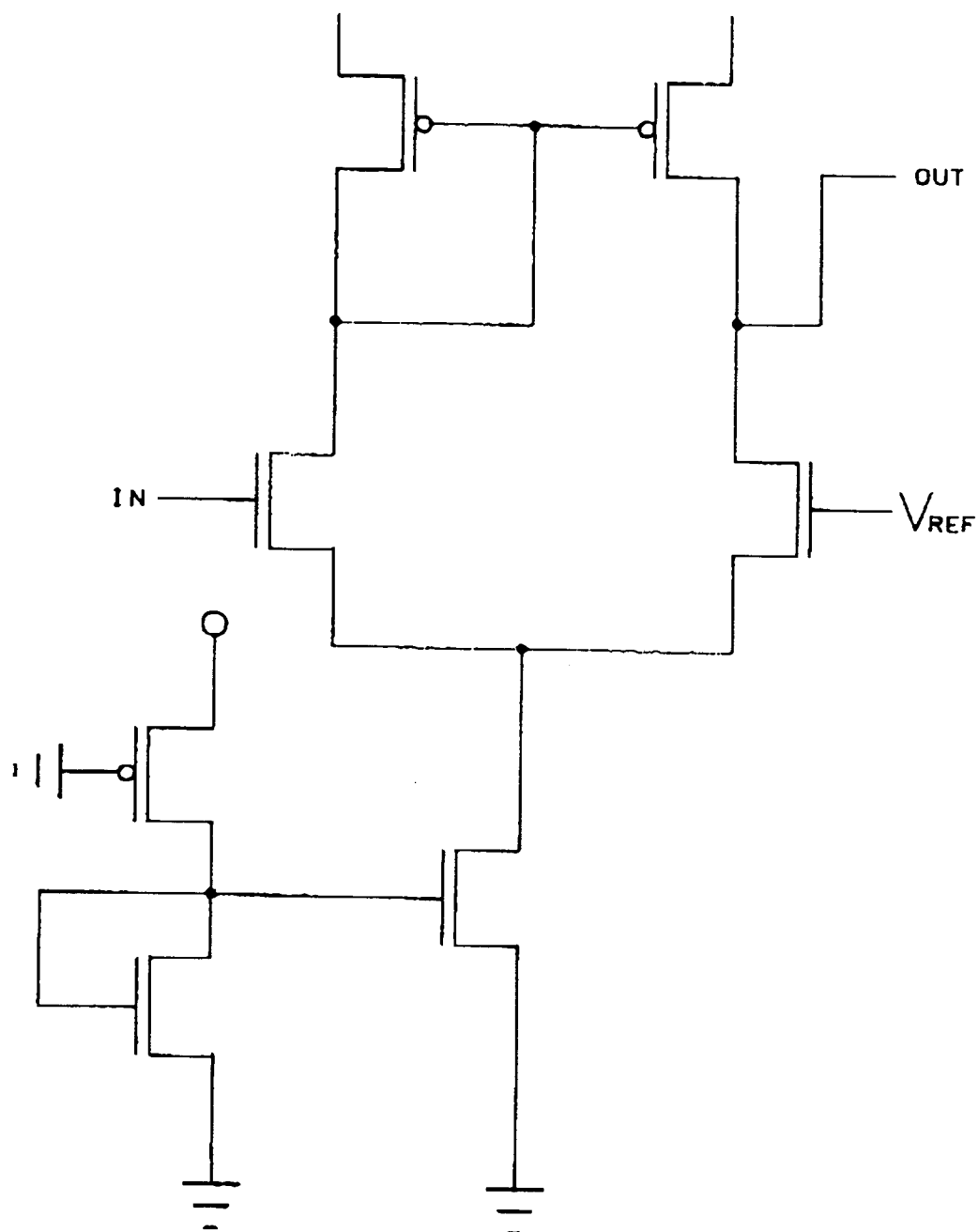


FIG. 3