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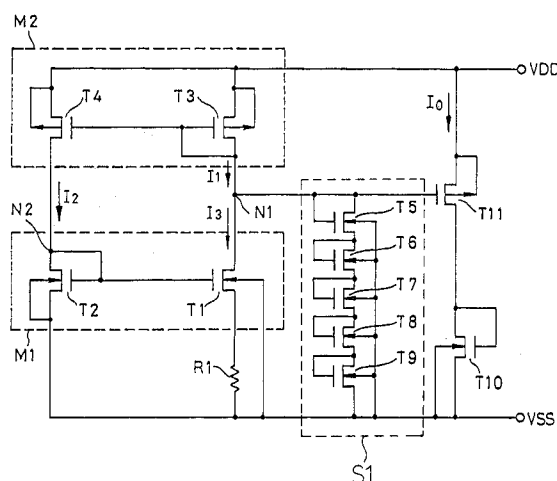
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D-80331 München (DE)(54) **Self-exciting constant current circuit.**

(57) A self-exciting constant current circuitry comprising first and second current mirror circuits (M1, M2) and a voltage control device. The first current mirror circuit (M1) is connected to a high voltage line supplying a high voltage and has an input side through which a first current flows and an output side through which a second current flows. The second current mirror circuit (M2) is connected to a low voltage line supplying a low voltage and has an output side being connected through a first node (N1) to the input side of the first current mirror circuit (M1) and an input side being connected through a second node (N2) to the output side of the first current mirror circuit (M1) in which the second current flows through the input side of the second current mirror circuit (M2) as well as a third current flows through the output side of the second current mirror circuit (M2). The voltage control device is electrically connected between the first node (N1) and the low voltage line for controlling, only in starting the circuitry, a potential of the first node (N1) at a predetermined stationary potential value where the first and second current mirror circuits (M1, M2) are in a stationary and operational state.

FIG. 3**EP 0 651 311 A2**

The invention relates to a constant current circuit, and more particularly to a circuitry for starting in self-excitation a constant current circuit involved in a CMOS integrated circuit.

A conventional constant current circuit involved in a CMOS integrated circuit will be described with reference to FIG. 1. The conventional constant current circuit includes first and second current mirror circuits M1 and M2 and a resistance R1, that are provided between high and low voltage lines that supply high and low voltages V_{DD} and V_{SS} respectively.

The first current mirror circuit M1 includes a first n-channel MOS transistor T1 and a second n-channel MOS transistor T2, while the second current mirror circuit M2 includes a first p-channel MOS transistor T3 and a second p-channel MOS transistor T4. The first n-channel MOS transistor T1 has a source electrically connected to a resistance R1 that is connected to the low voltage line V_{SS} , a drain electrically connected to a first node N1, a gate connected to a gate of the second n-channel MOS transistor T2 and a substrate electrically connected to the low voltage line. The second n-channel MOS transistor has the gate connected to the gate of the first n-channel MOS transistor, a drain electrically connected to the gate through a second node N2, a source electrically connected to the low voltage line and a substrate electrically connected to the source. The second n-channel MOS transistor including the gate-drain connection performs as a diode.

The second current mirror circuit M2 includes a first p-channel MOS transistor T3 and a second p-channel MOS transistor T4. The first p-channel MOS transistor T3 has a source electrically connected to the high voltage line, a drain electrically connected to the first node N1 that is connected to the drain of the first n-channel MOS transistor T1, a gate electrically connected both to a gate of the second p-channel MOS transistor T4 and to the drain thereof and a substrate connected to the source thereof. The first p-channel MOS transistor T3 having the gate drain connection performs as a diode. The second p-channel MOS transistor T4 has a source connected to the high voltage line, a drain connected to the second node N2 that is connected to the drain of the second n-channel MOS transistor T2, the gate connected to the first p-channel MOS transistor T3 and a substrate connected to the source thereof.

The conventional constant current circuit further includes a third p-channel MOS transistor T11 and third and fourth n-channel MOS transistors T10 and T12. The third p-channel MOS transistor T11 has a source connected to the high voltage line, a drain connected to a drain of the third n-channel MOS transistor T10, a gate connected to the first

node N1 and a substrate connected to the source thereof. The third n-channel MOS transistor T10 has a source connected to the low voltage line, the drain connected to the drain of the third p-channel MOS transistor T11, a gate connected to the drain thereof and a substrate connected to the source thereof. The fourth n-channel MOS transistor T12 has a source connected to the low voltage line, a drain connected to the first node N1, a gate receiving a start or reset signal and a substrate connected to the low voltage line and the source of the third n-channel MOS transistor T10. Then, the source and substrate of the third n-channel MOS transistor T10 as well as the substrate of the fourth n-channel MOS transistor T12 are connected to the low voltage line.

The third p-channel MOS transistor T11 is provided to form a third current mirror circuit in cooperation with the first p-channel MOS transistor T3. The first, second and third current mirror circuits have first, second and third current gain values respectively. The first n-channel MOS transistor T1 has a third drain current I_3 . The second n-channel MOS transistor T2 and the second p-channel MOS transistor T4 have a second drain current I_2 . The first p-channel MOS transistor T3 has a first drain current. The first current gain value of the first current mirror circuit M1 defines a ratio of the second drain current I_2 to the third drain current value I_3 . The first current gain value of the first current mirror circuit M1 depends upon a resistance value of the resistance R1. The second current gain value of the second current mirror circuit M1 defines a ratio of the second drain current I_2 to the first drain current value I_1 . The third drain current corresponds to the sum of the first drain current and a current flowing through the fourth n-channel MOS transistor T12. The third current mirror circuit comprising the first p-channel MOS transistor T3 and the third p-channel MOS transistor T11 performs to induce an output current I_0 from the high voltage line into the source of the third p-channel MOS transistor T11.

The description will focus on operations of the conventional constant current circuit. For starting the constant current circuit, the gate of the fourth n-channel MOS transistor receives a reset signal comprising a high voltage signal whereby the fourth n-channel MOS transistor turns ON. The low voltage V_{SS} is supplied from the low voltage line through the ON-state fourth n-channel MOS transistor T12 to the gates of the first to third p-channel MOS transistors T3, T4 and T11 thereby the first to third p-channel MOS transistors T3, T4 and T11 turn ON. The high voltage V_{DD} is supplied from the high voltage line through the second p-channel MOS transistor T4 into the second node N2. The high voltage V_{DD} of the second node N2 is then

supplied to the gates of the first and second n-channel MOS transistors thereby the first and second n-channel MOS transistors T1 and T2 turn ON. Further, the high voltage V_{SS} is supplied from the high voltage line through the third p-channel MOS transistor T11 to the gate of the third n-channel MOS transistor T10 thereby the third n-channel MOS transistor T10 turns ON. Namely, applying the high level signal to the gate of the fourth n-channel MOS transistor T12 results in turning ON of all the transistors. The operations of the constant current circuit is stabilized at an operational point where the product of the first and second current gains is 1. In the stable point, the output current is fetched through the third current mirror circuit including the third p-channel MOS transistor T11.

The above described convention constant current circuit has disadvantages as described below. The conventional circuit requires a further external circuit for generating a reset signal as an external signal to be applied to the gate of the fourth n-channel MOS transistor T10. The external circuit is required to have a detector for detecting applications of the high voltage and a trigger circuit for outputting the external signal. In the above circuit, it is possible that variations of the power source voltage, particularly in a rapid drop of the high voltage appears. The variation of the power source voltage such as the rapid drop of the high voltage results in that a closed loop circuit comprising the first and second current mirror circuits M1 and M2 may be made stable without any operational point where all of the transistors involved in the first and second current mirror circuits M1 and M2 are in Off state and then the constant current circuit exhibits no output current.

To combat the above problem, another type constant current circuit has been proposed in which the another constant current circuit is provided with a self-excitation starting circuit as disclosed in the Japanese laid-open patent application No. 4-111008. FIG. 3 illustrates a circuit configuration of the constant current circuit with the self-excitation starting circuit. The circuit configuration of the constant current circuit with the self-excitation starting circuit has the same structure of the conventional circuit as illustrated in FIG. 1 except for providing two of extra n-channel and p-channel MOS transistors T13 and T14 both between the first node N1 and the high voltage line and between the low voltage line and the second node N2.

Namely, the another conventional constant current circuit includes the first and second current mirror circuits M1 and M2 and a resistance R1, that are provided between the high and low voltage lines that supply the high and low voltages V_{DD} and V_{SS} respectively.

The first current mirror circuit M1 includes the first n-channel MOS transistor T1 and the second n-channel MOS transistor T2, while the second current mirror circuit M2 includes the first p-channel MOS transistor T3 and the second p-channel MOS transistor T4. The first n-channel MOS transistor T1 has the source electrically connected to the resistance R1 that is connected to the low voltage line V_{SS} , a drain electrically connected to the first node N1, a gate connected to a gate of the second n-channel MOS transistor T2 and a substrate electrically connected to the low voltage line. The second n-channel MOS transistor has the gate connected to the gate of the first n-channel MOS transistor, a drain electrically connected to the gate through the second node N2, the source electrically connected to the low voltage line and a substrate electrically connected to the source. The second n-channel MOS transistor including the gate-drain connection performs as a diode.

The second current mirror circuit M2 includes the first p-channel MOS transistor T3 and the second p-channel MOS transistor T4. The first p-channel MOS transistor T3 has the source electrically connected to the high voltage line, a drain electrically connected to the first node N1 that is connected to the drain of the first n-channel MOS transistor T1, a gate electrically connected both to a gate of the second p-channel MOS transistor T4 and to the drain thereof and a substrate connected to the source thereof. The first p-channel MOS transistor T3 having the gate drain connection performs as a diode. The second p-channel MOS transistor T4 has a source connected to the high voltage line, a drain connected to the second node N2 that is connected to the drain of the second n-channel MOS transistor T2, the gate connected to the first p-channel MOS transistor T3 and a substrate connected to the source thereof.

The conventional constant current circuit further includes the third p-channel MOS transistor T11 and the third and fourth n-channel MOS transistors T10 and T12. The third p-channel MOS transistor T11 has a source connected to the high voltage line, a drain connected to a drain of the third n-channel MOS transistor T10, a gate connected to the first node N1 and a substrate connected to the source thereof. The third n-channel MOS transistor T10 has a source connected to the low voltage line, the drain connected to the drain of the third p-channel MOS transistor T11, a gate connected to the drain thereof and a substrate connected to the source thereof. The fourth n-channel MOS transistor T12 has a source connected to the low voltage line, a drain connected to the first node N1, a gate receiving a start or reset signal and a substrate connected to the low voltage line and the source of the third n-channel MOS

transistor T10. Then, the source and substrate of the third n-channel MOS transistor T10 as well as the substrate of the fourth n-channel MOS transistor T12 are connected to the low voltage line.

The third p-channel MOS transistor T11 is provided to form a third current mirror circuit in cooperation with the first p-channel MOS transistor T3. The first, second and third current mirror circuits have first, second and third current gain values respectively. The first n-channel MOS transistor T1 has the third drain current I_3 . The second n-channel MOS transistor T2 and the second p-channel MOS transistor T4 have the second drain current I_2 . The first p-channel MOS transistor T3 has the first drain current. The first current gain value of the first current mirror circuit M1 defines a ratio of the second drain current I_2 to the third drain current value I_3 . The first current gain value of the first current mirror circuit M1 depends upon a resistance value of the resistance R1. The second current gain value of the second current mirror circuit M1 defines a ratio of the second drain current I_2 to the first drain current value I_1 . The third drain current corresponds to the sum of the first drain current and a current flowing through the fourth n-channel MOS transistor T12. The third current mirror circuit comprising the first p-channel MOS transistor T3 and the third p-channel MOS transistor T11 performs to induce an output current I_0 from the high voltage line into the source of the third p-channel MOS transistor T11.

As described below, the another conventional constant current circuit further includes the fifth n-channel MOS transistor T13 and the fourth p-channel MOS transistor T14. The fifth n-channel MOS transistor T13 is provided between the low voltage line and the second node N2. The fifth n-channel MOS transistor T13 has a gate electrically connected to the low voltage line, a source connected to the low voltage line, a drain connected to the second node N2 and a substrate connected to the low voltage line. The fourth p-channel MOS transistor T14 is provided between the high voltage line and the first node N1. The fourth p-channel MOS transistor T14 has a gate electrically connected to the high voltage line, a source connected to the high voltage line, a drain connected to the first node N2 and a substrate connected to the high voltage line. As described above, the gate of the fifth n-channel MOS transistor T13 is directly connected to the low voltage line so that the low level signal is always applied to the gate of the fifth n-channel MOS transistor T13 thereby the fifth n-channel MOS transistor T13 always remains in the off state. Also, the gate of the fourth p-channel MOS transistor T14 is directly connected to the high voltage line so that the high level signal is always applied to the gate of the fourth p-channel

MOS transistor T14 thereby the fourth p-channel MOS transistor T14 always remains in the off state. As a result, the fifth n-channel and fourth p-channel MOS transistors T13 and T14 may supply leakage currents in the off-state or off-leak current to the second and first nodes N2 and N1 respectively for realizing the self-excitation. Namely, the off-leak current is used as a self-excitation current.

The above self-excitation system using the off-leakage current is however engaged with the following problems. The off-leak current is kept to flow during the stationary state of the constant current circuit. This results in an increase of power consumptions. Further, the off-leak current causes a problem with unnecessary heat generation that makes it difficult to layout the circuit configuration in view of the circuit design. It would therefore be required to suppress any current flow for the self-exciting except for the time of starting the constant current circuit.

Accordingly, it is a primary object of the present invention to provide a novel constant current circuitry free from any problems or disadvantages as described above.

It is a further object of the present invention to provide a novel constant current circuitry permitting a current flow for a self-excitation but only in starting the constant current circuitry.

It is a still further object of the present invention to provide a novel constant current circuitry provided with a self-excitation circuit free from any stationary current flow.

It is a further more object of the present invention to provide a novel constant current circuitry exhibiting a low power consumption.

The above and other objects, features and advantages of the present invention will be apparent from the following descriptions.

The invention provides a circuitry comprising first and second current mirror circuits and a voltage control device. The first current mirror circuit is connected to a high voltage line that supplies a predetermined high voltage. The first current mirror circuit has an input side through which a first current flows and an output side through which a second current flows. The second current mirror circuit is connected to a low voltage line that supplies a predetermined low voltage. The second current mirror circuit has an output side being connected through a first node to the input side of the first current mirror circuit and an input side being connected through a second node to the output side of the first current mirror circuit in which the second current flows through the input side of the second current mirror circuit as well as a third current flows through the output side of the second current mirror circuit. The voltage control device is electrically connected between the first

node and the low voltage line for controlling, only in starting the circuitry, a potential of the first node at a predetermined stationary potential value where the first and second current mirror circuits are in a stationary and operational state.

The voltage control device may comprise a switching circuit being electrically connected between the first node and the low voltage line. The switching circuit has a threshold voltage that is just higher than the predetermined stationary potential value so that just when the potential of the first node comes beyond the predetermined stationary potential value then the switching circuit turns ON to thereby render the first node electrically conductive to the low voltage line for drop of the potential of the first node down to the predetermined stationary potential value. The switching circuit comprises a series connection of a plurality of field effect transistors between the first node and the low voltage line in which a sum of threshold voltages of the individual plural field effect transistors corresponds to the threshold voltage of the switching circuit. Each of the plural field effect transistors involved in the switching circuit has a substrate connected to the low voltage line and a gate connected at the first node side to an adjacent one of the field effect transistors to form a diode connection between the first node and the low voltage line.

Preferred embodiments of the present invention will hereinafter fully be described in detail with reference to the accompanying drawings.

FIG. 1 is a circuit diagram illustrative of the conventional constant current circuit.

FIG. 2 is a circuit diagram illustrative of the another conventional constant circuit.

FIG. 3 is a circuit diagram illustrative of a novel constant current circuit of a preferred embodiment according to the present invention.

A first embodiment of the present invention will be described with reference to FIG. 3 in which a novel constant current circuitry is provided.

The novel constant current circuit according to the present invention includes first and second current mirror circuits M1 and M2 and a resistance R1, that are provided between high and low voltage lines that supply high and low voltages V_{DD} and V_{SS} respectively as well as an improved self-exciting circuit comprising a switching circuit for realizing a self-excitation in which a current flow for self-excitation appears only in starting the constant current circuit. The improved self-exciting circuit as the switching circuit is provided between an output side of the second current mirror circuit and any one of the high and low voltage lines.

The first current mirror circuit M1 includes a first n-channel MOS transistor T1 and a second n-channel MOS transistor T2, while the second current mirror circuit M2 includes a first p-channel

MOS transistor T3 and a second p-channel MOS transistor T4. The first n-channel MOS transistor T1 has a source electrically connected to a resistance R1 that is connected to the low voltage line V_{SS} , a drain electrically connected to a first node N1, a gate connected to a gate of the second n-channel MOS transistor T2 and a substrate electrically connected to the low voltage line. The second n-channel MOS transistor has the gate connected to the gate of the first n-channel MOS transistor, a drain electrically connected to the gate through a second node N2, a source electrically connected to the low voltage line and a substrate electrically connected to the source. The second n-channel MOS transistor including the gate-drain connection performs as a diode.

The second current mirror circuit M2 includes a first p-channel MOS transistor T3 and a second p-channel MOS transistor T4. The first p-channel MOS transistor T3 has a source electrically connected to the high voltage line, a drain electrically connected to the first node N1 that is connected to the drain of the first n-channel MOS transistor T1, a gate electrically connected both to a gate of the second p-channel MOS transistor T4 and to the drain thereof and a substrate connected to the source thereof. The first p-channel MOS transistor T3 having the gate drain connection performs as a diode. The second p-channel MOS transistor T4 has a source connected to the high voltage line, a drain connected to the second node N2 that is connected to the drain of the second n-channel MOS transistor T2, the gate connected to the first p-channel MOS transistor T3 and a substrate connected to the source thereof.

The novel constant current circuit further includes a third p-channel MOS transistor T11 and a third n-channel MOS transistor T10. The third p-channel MOS transistor T11 has a source connected to the high voltage line, a drain connected to a drain of the third n-channel MOS transistor T10, a gate connected to the first node N1 and a substrate connected to the source thereof. The third n-channel MOS transistor T10 has a source connected to the low voltage line, the drain connected to the drain of the third p-channel MOS transistor T11, a gate connected to the drain thereof and a substrate connected to the low voltage line.

The novel constant current circuit further includes a switching circuit S1 for self-excitation of the constant current circuit. The switching circuit S1 is provided between the node N1 and the low voltage line. The switching circuit comprises series connections of five n-channel MOS transistors T5 to T9 between the low voltage line and the first node N1. The n-channel MOS transistor T5 has a source, a gate connected to the first node N1, a

drain connected to the first node N1 and a substrate connected to the low voltage line. The n-channel MOS transistor T6 has a source, a gate connected to the source of the n-channel MOS transistor T5, a drain connected to the source of the n-channel MOS transistor T5 and a substrate connected to the low voltage line. The n-channel MOS transistor T7 has a source, a gate connected to the source of the n-channel MOS transistor T6, a drain connected to the source of the n-channel MOS transistor T6 and a substrate connected to the low voltage line. The n-channel MOS transistor T8 has a source, a gate connected to the source of the n-channel MOS transistor T7, a drain connected to the source of the n-channel MOS transistor T7 and a substrate connected to the low voltage line. The n-channel MOS transistor T9 has a source connected to the low voltage line, a gate connected to the source of the n-channel MOS transistor T8, a drain connected to the source of the n-channel MOS transistor T8 and a substrate connected to the low voltage line. The switching circuit comprising the series connections of the n-channel MOS transistors T5 to T9 has a predetermined threshold voltage that almost corresponds to the sum of threshold voltages of the individual n-channel MOS transistors T5 to T9.

The third p-channel MOS transistor T11 is provided to form a third current mirror circuit in cooperation with the first p-channel MOS transistor T3. The first, second and third current mirror circuits have first, second and third current gain values respectively. The first n-channel MOS transistor T1 has a third drain current I_3 . The second n-channel MOS transistor T2 and the second p-channel MOS transistor T4 have a second drain current I_2 . The first p-channel MOS transistor T3 has a first drain current. The first current gain value of the first current mirror circuit M1 defines a ratio of the second drain current I_2 to the third drain current value I_3 . The first current gain value of the first current mirror circuit M1 depends upon a resistance value of the resistance R1. The second current gain value of the second current mirror circuit M1 defines a ratio of the second drain current I_2 to the first drain current value I_1 . The third drain current I_3 corresponds to the sum of the first drain current and a current flowing through the fourth n-channel MOS transistor T12. The third current mirror circuit comprising the first p-channel MOS transistor T3 and the third p-channel MOS transistor T11 performs to induce an output current I_0 from the high voltage line into the source of the third p-channel MOS transistor T11.

The description will focus on operations of the novel constant current circuit. The high and low voltage lines may have voltages of 5V and 0V respectively. The constant current circuit may be

stabilized at the operational point where the product of the first and second current gain values of the first and second current mirror circuits M1 and M2 comes into 1. The first drain current value I_1 is defined by both length and width of the individual gate of the first and second n-channel and p-channel MOS transistors T1, T2, T3 and T4 as well as a resistance value of the resistance R1. A potential V_{N1} of the first node N1 is varied in the range of from 0V to 5V by variation of the first drain current I_1 .

Power ON or rapid drop of the power source voltage may cause that a potential V_{N2} of the second node N2 comes into a lower voltage than a threshold voltage V_{thT2} of the second n-channel MOS transistor T2 as well as the potential V_{N1} of the first node N1 comes into a lower voltage than a threshold voltage V_{thT3} of the first p-channel MOS transistor T3. Under this state, all the first and second n-channel and p-channel MOS transistors T1, T2, T3 and T4 come into the cut-off state so that none of the first and second drain current flows. This cut-off state causes a voltage increase of first node N1 toward the high voltage V_{DD} of the high voltage line. When the voltage of the first node N1 comes beyond the threshold voltage of the switching circuit S1 or the sum of the threshold voltages of the n-channel MOS transistors T5, T6, T7, T8 and T9, then the switching circuit S1 comes into ON state thereby the first node N1 is made into electrically conductive to the low voltage line. This results in a potential drop of the first node N1. The potential drop of the first node N1 causes a current flow of the first drain current I_1 so that the first and second current mirror circuits M1 and M2 are stabilized at the operational point where product of the first and second current gain values of the first and second mirror circuits M1 and M2 comes into 1. Under the operational state of the constant current circuit, the n-channel MOS transistors T5, T6, T7, T8 and T9 connected in series between the low voltage line and the first node N1 remain in the cut-off state. The threshold voltage of the switching circuit S1 is required to be higher than a potential value of the first node N1 under the stable operational point of the constant current circuit but lower than the high voltage V_{DD} of the high voltage line. Consequently, under the stationary operational state of the constant current circuit, the switching circuit is kept in the off state, while in starting the constant current circuit the switching circuit comes into the ON state to thereby establish the self-exciting circuit with the negative feedback function.

Whereas modifications of the present invention will no doubt be apparent to a person having ordinary skill in the art, to which the invention pertains, it is to be understood that the embodiments

shown and described by way of illustrations are by no means intended to be considered in a limiting sense. Accordingly, it is to be intended to cover by claims all modifications of the present invention which fall within the spirit and scope of the invention.

Claims

1. A circuitry comprising a first current mirror circuit (M1) being connected to a high voltage line that supplies a predetermined high voltage, said first current mirror circuit (M1) having an input side through which a first current flows and an output side through which a second current flows, and a second current mirror circuit (M2) being connected to a low voltage line that supplies a predetermined low voltage, said second current mirror circuit (M2) having an output side being connected through a first node (N1) to said input side of said first current mirror circuit (M1) and an input side being connected through a second node (N2) to said output side of said first current mirror circuit (M1) in which said second current flows through said input side of said second current mirror circuit (M2) as well as a third current flows through said output side of said second current mirror circuit (M2), said circuitry being characterized by means (S1) being electrically connected between said first node (N1) and said low voltage line for controlling, only in starting said circuitry, a potential of said first node (N1) at a predetermined stationary potential value where said first and second current mirror circuits (M1, M2) are in a stationary and operational state.
2. The circuitry as claimed in claim 1, characterized in that said controlling means (S1) comprises a switching circuit being electrically connected between said first node (N1) and said low voltage line, said switching circuit having a threshold voltage that is just higher than said predetermined stationary potential value so that just when said potential of said first node (N1) comes beyond said predetermined stationary potential value then said switching circuit turns ON to thereby render said first node (N1) electrically conductive to said low voltage line for drop of said potential of said first node (N1) down to said predetermined stationary potential value.
3. The circuitry as claimed in claim 2, characterized in that said switching circuit comprises a series connection of a plurality of field effect transistors between said first node (N1) and said low voltage line in which a sum of threshold voltages of said individual plural field effect transistors corresponds to said threshold voltage of said switching circuit.
4. The circuitry as claimed in claim 3, characterized in that each of said plural field effect transistors involved in said switching circuit has a substrate connected to said low voltage line and a gate connected at said first node (N1) side to an adjacent one of said field effect transistors to form a diode connection between said first node (N1) and said low voltage line.
5. A self-excitation constant current circuitry comprising a first current mirror circuit (M1) being connected to a high voltage line that supplies a predetermined high voltage, said first current mirror circuit (M1) having an input side through which a first current flows and an output side through which a second current flows, and a second current mirror circuit (M2) being connected to a low voltage line that supplies a predetermined low voltage, said second current mirror circuit (M2) having an output side being connected through a first node (N1) to said input side of said first current mirror circuit (M1) and an input side being connected through a second node (N2) to said output side of said first current mirror circuit (M1) in which said second current flows through said input side of said second current mirror circuit (M2) as well as a third current flows through said output side of said second current mirror circuit (M2), said circuitry being characterized by a voltage controlling circuit (S1) being electrically connected between said first node (N1) and said low voltage line for controlling, only in starting said circuitry, a potential of said first node (N1) at a predetermined stationary potential value where said first and second current mirror circuits (M1, M2) are in a stationary and operational state.
6. The circuitry as claimed in claim 5, characterized in that said voltage controlling circuit (S1) comprises a switching circuit being electrically connected between said first node (N1) and said low voltage line, said switching circuit having a threshold voltage that is just higher than said predetermined stationary potential value so that just when said potential of said first node (N1) comes beyond said predetermined stationary potential value then said switching circuit turns ON to thereby render said first node (N1) electrically conductive to said low voltage line for drop of said potential of said first node (N1) down to said predetermined stationary potential value.

mined stationary potential value.

7. The circuitry as claimed in claim 6, characterized in that said switching circuit comprises a series connection of a plurality of field effect transistors between said first node (N1) and said low voltage line in which a sum of threshold voltages of said individual plural field effect transistors corresponds to said threshold voltage of said switching circuit.
8. The circuitry as claimed in claim 7, characterized in that each of said plural field effect transistors involved in said switching circuit has a substrate connected to said low voltage line and a gate connected at said first node (N1) side to an adjacent one of said field effect transistors to form a diode connection between said first node (N1) and said low voltage line.

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FIG. 1 PRIOR ART

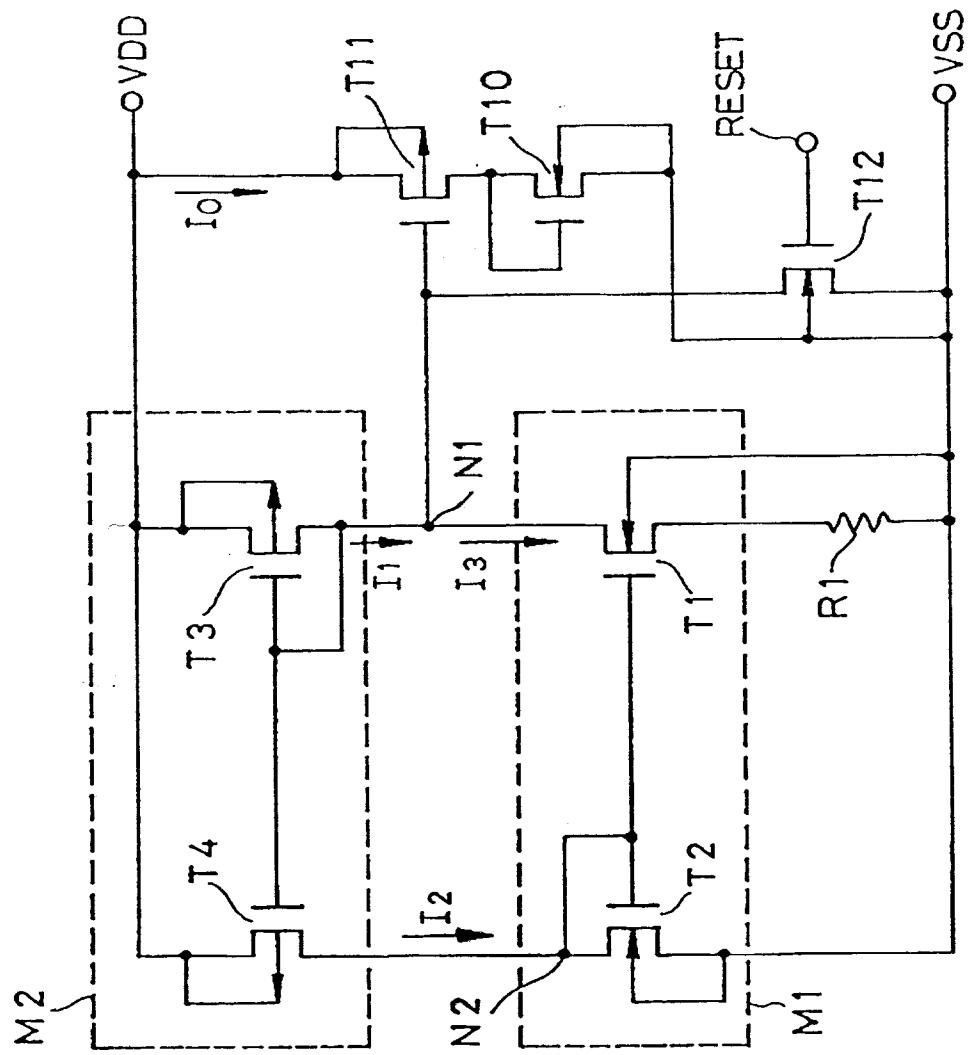


FIG. 2 PRIOR ART

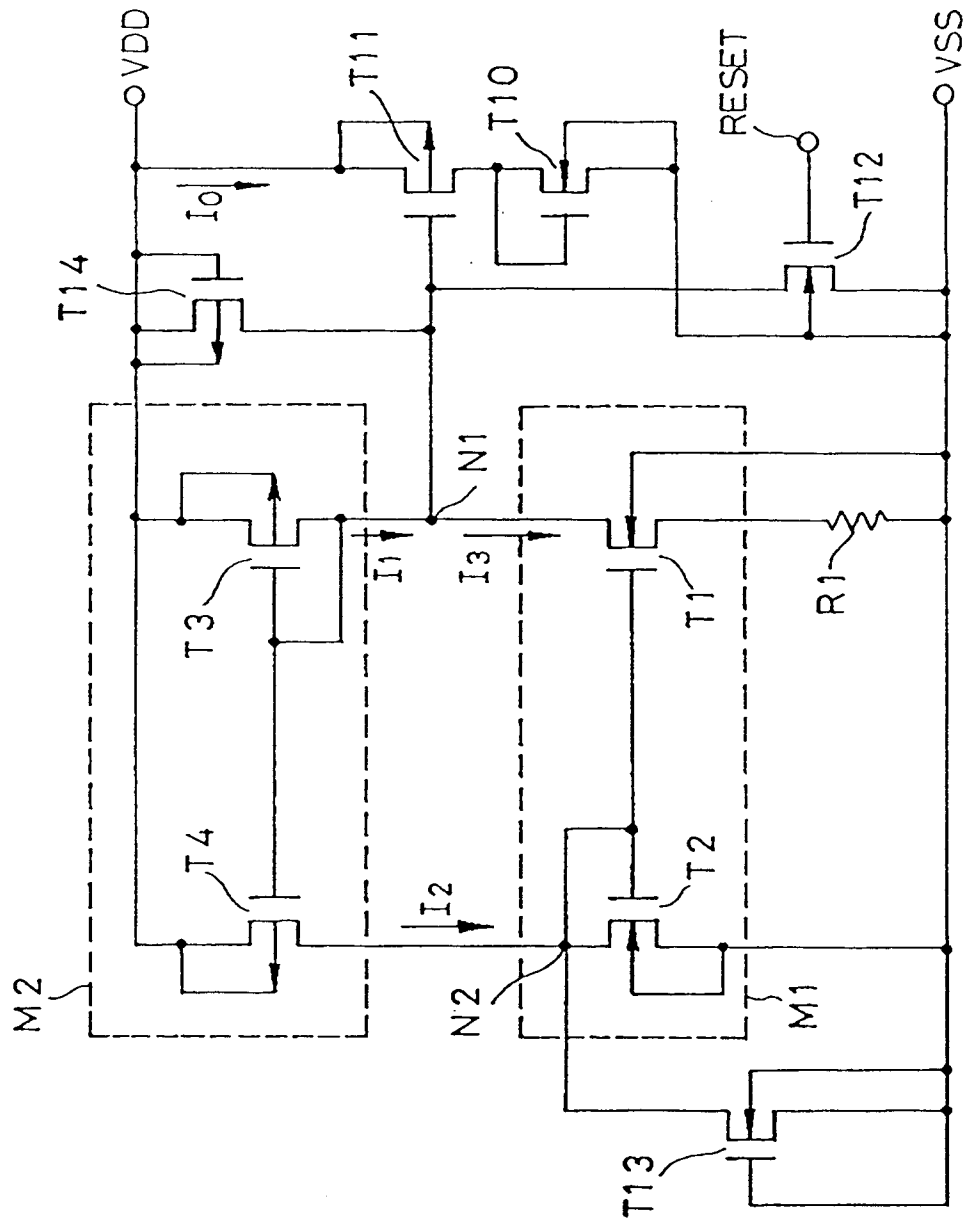


FIG. 3

