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(54) Cascaded sigma-delta modulators.

(57) A method of cascading sigma-delta modulators includes the step of feeding the input to the quantizer of each modulator stage to the subsequent stage. Therefore, the signal which is fed to each of the subsequent stages is the difference between the output and the quantization noise of the previous stage. The method also includes the step of removing the quantization noise of the first two stages, as well as the output of the first two stages, so that the final output of the cascaded modulators is a delayed version of the input, plus a scaled version of the last stage which has been shaped with a fourth-order high pass function.

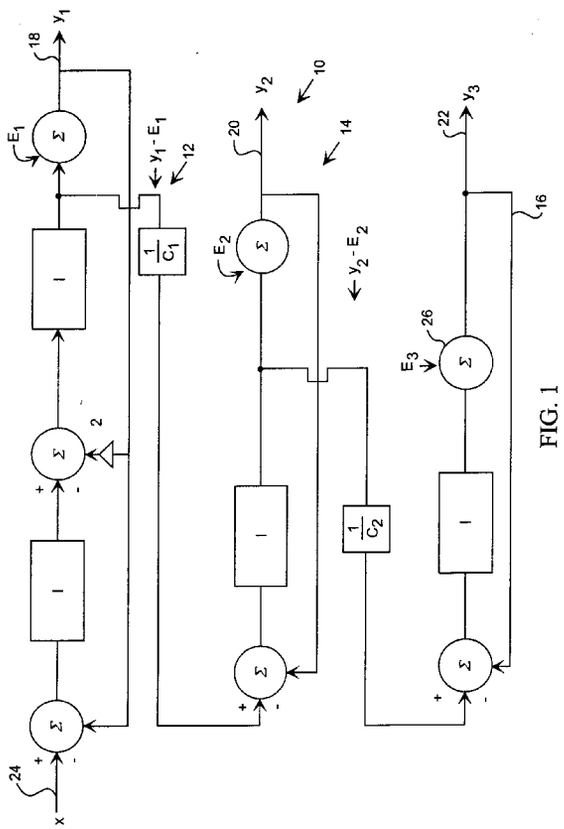


FIG. 1

EP 0 651 518 A1

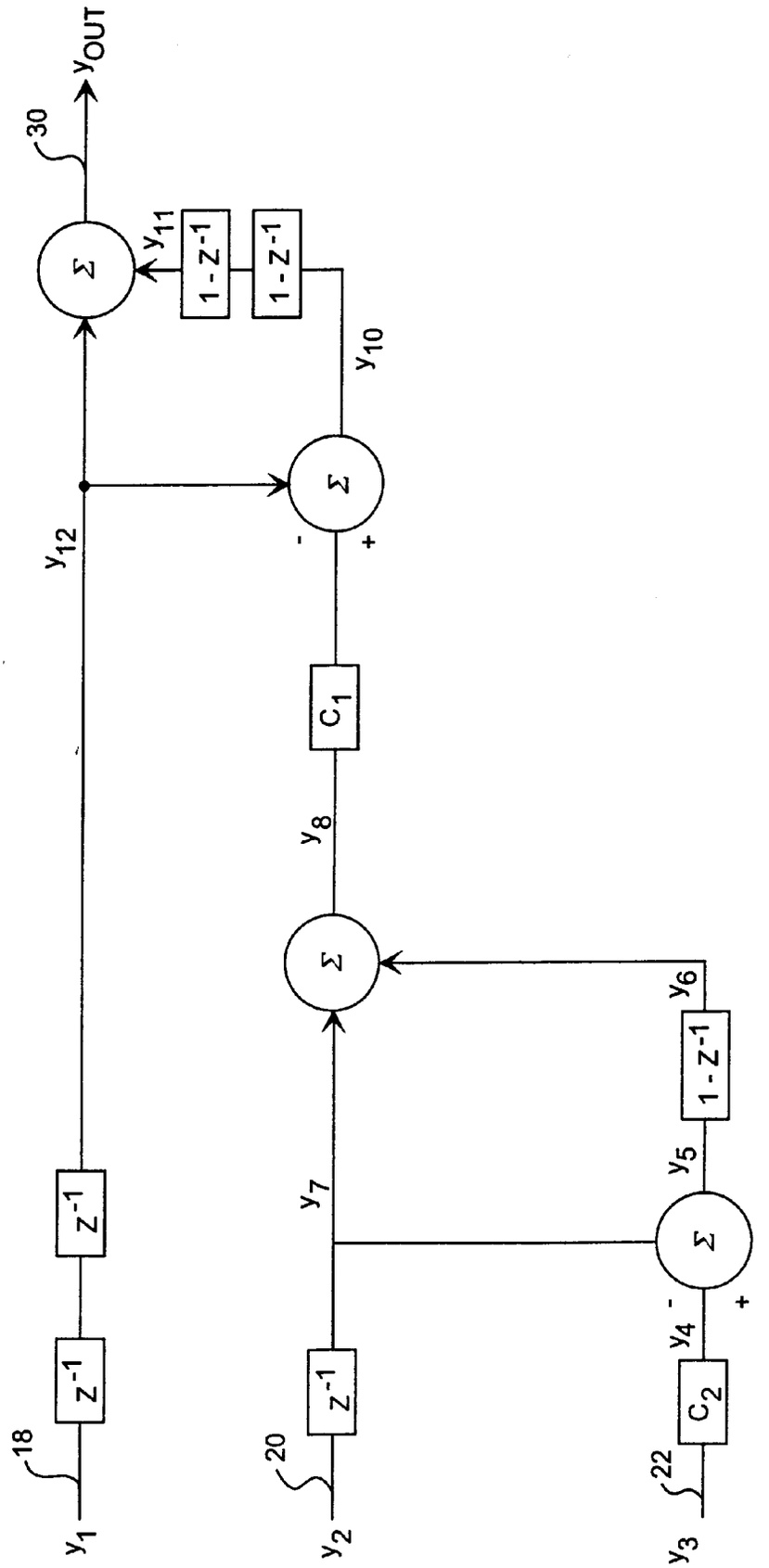

y_{OUT}
30
y_{11}
$1 - z^{-1}$
$1 - z^{-1}$
y_{10}
y_{12}
Σ
-
+
C_1
y_8
Σ
y_6
$1 - z^{-1}$
y_5
y_7
Σ
y_4
-
+
C_2
z^{-1}
z^{-1}
18
20
22
y_1
y_2
y_3

FIG. 2

The subject matter of this application is related to that in our copending application 94305762.0 and is incorporated herein by this reference thereto.

The present invention relates generally to sigma-delta modulators. More particularly, the present invention relates to methods of cascading sigma-delta modulators.

Description of Related Art

Oversampled interpolative (or sigma-delta) modulators comprise at least one integration stage or filter followed by a quantization stage (most typically a comparator) and a feedback from the output of the quantization stage to the input of the integration stage. Depending upon the number of integration stages, sigma-delta modulators can be divided into order types, e.g., second-order, third-order, or fourth-order.

Sigma-delta modulators have come to be commonly used to perform analog-to-digital (A/D) and digital-to-analog (D/A) conversion in a number of applications. These applications include coder-decoders (codecs), integrated services digital network (ISDN) equipment, and audio equipment.

The use of higher order sigma-delta modulators has become desirable in many applications for several reasons. One reason is because the introduction of higher order modulators increases the number of integrations to be carried out, which results in a decrease in the noise level of the passband as the quantization noise is shifted to a higher frequency level. Another reason is because the use of higher order modulators keeps the oversampling ratio (i.e., the ratio of the modulator clock to the Nyquist rate) low, which is desirable under certain conditions.

A number of efforts have heretofore been undertaken to develop higher order sigma-delta modulators. Five such efforts, those undertaken by Matsuya et al., Ribner, Chao et al., Karema et al., and the inventor of the present invention, Cabler, are discussed immediately below.

Matsuya, et al., in "A 16-Bit Oversampling A-D Conversion Technology Using Triple-Integration Noise Shaping", IEEE Journal of Solid State Circuits, Vol. SC-22, No. 6, pp. 921-929, Dec. 1987, have presented a method of cascading three or more first-order modulators in order to provide higher order noise shaping. A block diagram of this circuit is shown in FIG. 1 in our aforesaid application 94305762.0. The technique employed in this circuit, well known to those skilled in the art as the "MASH" technique, is described at length in U.S. Patent 5,061,928 to Karema. That discussion is incorporated herein by this reference thereto. Although the circuit in FIG. 1 of 94305762.0 could be discussed at length, given the level of skill of those skilled in the art, it suffices here to say that the circuit of that FIG. depicts three cascaded first-order modulators (each generally designated by reference numeral 2). Each first-order modulator 2 comprises an integrator 4 and a quantizer 6. The difference between the output signals of the integrators 4 and the quantizers 6 of the two topmost modulators 2 are fed to subsequent modulators 2. By doing this, quantized noise is moved up out of band, where it can be subsequently, and easily, filtered out. The MASH technique has a number of shortcomings however. First, the MASH technique requires tight matching of the characteristics of the modulators to achieve good resolution. The MASH technique also requires high op amp gains to accomplish the same results. Further, the technique has been shown to be quite sensitive to analog component mismatch when used as an A/D converter. Mismatches in the analog circuitry result in uncancelled quantization noise leaking into the passband. Theoretically, however, with regard to the circuit of FIG. 1 in 94305762.0, if the input to the converter is given as x, and the quantization error of the last modulator is given as E_3, the output, y, can be expressed as follows:

$$y = xz^{-3} + E_3(1 - z^{-1})^3$$

As previously mentioned, Ribner also has worked to develop higher order sigma-delta modulators. Ribner, in "A Third-Order Multistage Sigma-Delta Modulator with Reduced Sensitivity to Nonidealities", IEEE J. Solid-State Circuits, Vol. 26, No. 12, pp. 1764-1774, Dec. 1991, and in U.S. Patent Nos. 5,148,167, 5,148,166, and 5,065,157, has presented a method of cascading a second-order modulator with a first-order modulator. A block diagram of this circuit is shown in FIG. 2 of 94305762.0 wherein the second-order modulator is generally designated with reference numeral 8 and the first-order modulator generally designated with reference numeral 10. Referring to the bottommost portion of FIG. 2 in 94305762.0 it is depicted that Ribner teaches combining the quantized outputs y_1, y_2 of the modulators 8,10 in such a manner that the quantization noise of the second-order section is cancelled while the quantization noise of the first-order section is shaped in a third-order manner. Once again, mathematically, if the input to the converter is given as x, and the quantization error of the first-order modulator is given as E_2, the output, y, can be expressed as follows:

$$y = z^{-3}x + C(1 - z^{-1})^3 E_2$$

In this case a gain of 1/C was added between the modulators 8,10 in order to prevent the second modulator 10 from overflowing. In order to compensate for the factor of 1/C, a gain of C is added in the correction logic. This can be seen in FIG. 2 of 94305762.0 the form of element 12 (the gain adding portion) and element 14 (the compensation portion).

Chao et al., in "A Higher Order Topology for Interpolative Modulators For Oversampling A/D Converters, IEEE Transactions on Circuits and Systems, Vol. 37, No. 3, pp. 309-318, Mar. 1990, have proposed a single loop structure for higher order sigma-delta

modulators. These modulators consist of a multitude of integrators, feed-forward paths, feed-back paths, and a single quantizer in order to synthesize the desired noise shaping. These modulators suffer from the possibility that they may enter into a mode of self sustained oscillations for certain input values. Various methods have been proposed to desensitize these converters to this phenomena, all of which complicate the structure. It has been noted, however, that single stage first- and second-order modulators of this type do not suffer from this phenomena.

For audio applications, it is desired that the signal-to-total distortion, including noise, be equivalent to that of a standard 16-bit linear converter. Simulations have indicated that for an oversampling ratio of 64, and using practical circuit techniques, third-order modulators built based upon any of the above methods will exceed the performance of a standard 16-bit linear converter. However, the amount of margin beyond 16 bits is not very high. Therefore, it is desired that a sigma-delta converter be built with fourth- order noise shaping.

Karema et al., in U.S. Patent No. 5,061,924, have introduced a fourth- order topology which comprises of a cascade of two second-order modulators. This is shown in FIG. 3 of 94305762.0 wherein the two second- order modulators are generally designated with reference numeral 16. As shown therein, a gain of 1/C (in the form of gain element 18) has been added between the two modulators in order to prevent overflow of the second modulator. As in Ribner's modulator depicted in FIG. 2 discussed alone, a digital circuit is added to Karema et al.'s cascade. This circuit, generally designated by reference numeral 20, is set forth at the bottom of FIG. 3 in 94305762.0. This circuit combines the quantized outputs of the two second-order sections y_1, y_2 in such a manner that the quantization error of the first modulator is cancelled and the quantization error of the second modulator receives fourth-order shaping. Algebraically, if the input to the converter is given as x, and the quantization error of the second modulator is given as E_2, then the output y can be expressed as:

$$y = z^{-4} x + C(1 - z^{-1})^4 E_2$$

In our aforesaid application 94305762.0 we disclose a system and method for cascading three sigma-delta modulators. The system and method involves applying an error signal representing the quantization error of a preceding modulator to a subsequent modulator. The error signal is scaled by a factor before being applied to a subsequent modulator. The quantized error signal of the subsequent modulator is then scaled by the reciprocal of the original scaling factor before being combined with the quantized outputs of the previous modulators. Combining the quantized outputs of the three modulators is performed so as to cancel the quantization error of the previous stages while shaping the noise at the last stage so that most of the noise is placed at high frequencies.

Thus, in Cabler's design, the quantization noise of each stage is obtained by taking the difference between the output and the input of the quantizer of each stage. This quantization noise is then fed to the subsequent stage. A correction network then removes the quantization noise from each of the previous stages in such a manner that the output is simply a delayed version of the input, plus a scaled version of the quantization noise from the last stage which has been shaped with a fourth-order high pass function.

Based upon the foregoing, it should be understood and appreciated that fourth-order sigma-delta modulators have important advantages over lesser order modulators in certain applications. Further on this point, the signal-to-noise ratio (SNR) of ideal sigma-delta modulators is given by the following equation:

$$SNR = (2L + 1)\, 10 \log (OSR) - 10 \log (\pi^{2L}/2L + 1)$$

where OSR is the oversampling ratio and L is the order of the modulator. For example, if L = 3 and the OSR = 64, the SNR equals 105dB. If L=4 and OSR=64, the SNR equals 132.3dB. Thus, a fourth-order loop has more inherent margin for 16-bit performance than does a third-order loop with the same oversampling ratio. Although fourth-order sigma-delta modulators, such as that taught by Karema et al., have heretofore been proposed, it is a shortcoming and deficiency of the prior art that there are not additional types of such modulators to use.

As discussed at length in 94305762.0 the modulator disclosed therein constitutes a fourth-order sigma-delta modulator that strikes a good balance between use of first-order modulators (which are less expensive than second-order modulators) and use of second-order modulators (which are easier to match than first-order modulators, but which are more expensive). The modulator disclosed in 94305762.0 is, however, somewhat complex, and it therefore requires use of a number of analog components. It is a shortcoming and deficiency of the prior art that there is not available a simpler, less expensive version of this modulator, which could be fruitfully used in many applications.

We have overcome the shortcomings and deficiencies mentioned above by providing a new method of cascading three sigma-delta modulators. In this method, the input of the quantizer of each stage is fed to the subsequent stage. Thus, a difference between the output of each quantizer and the input of each quantizer need not be obtained. The signal which is fed to each of the subsequent stages is the difference between the output of the previous stage and the quantization noise of the previous stage. Embodiments of the present invention include a correction network which removes both the quantization noise

of the first two stages, as well as the output of the first two stages. Thus, the final output of the cascaded modulators is a delayed version of the input thereto, plus a scaled version of the last stage which has been shaped with a fourth-order high pass function.

Accordingly, we shall describe a system and method for accomplishing high resolution A/D conversion.

We shall also describe a new type of fourth-order sigma-delta modulator, and an A/D converter in which fewer subtractions must take place between stages as compared to prior art converters and, thus, in which fewer analog components are required.

In the accompanying drawings, by way of example only:-

FIG. 1 is a schematic diagram of an embodiment of the present invention;

FIG. 2 is a schematic diagram of a correction network according to the teachings of the present invention;

FIG. 3 is a schematic diagram of an alternative correction network according to the teachings of the present invention;

FIG. 4 is a schematic diagram of yet another alternative correction network according to the teachings of the present invention; and

FIG. 5 is a plot of simulated SNR performance for an embodiment of the present invention.

Referring now to the drawings wherein like or similar elements are designated with identical reference numerals throughout the several views and, more particularly, to FIG. 1, there is shown a schematic diagram of an embodiment of the present invention generally designated by reference numeral 10. The embodiment 10 comprises a conventional second-order sigma-delta modulator (generally designated by reference numeral 12), a first first-order sigma-delta modulator (generally designated by reference numeral 14), and a second first-order sigma-delta modulator (generally designated by reference numeral 16).

As is well known to those skilled in the art, the standard equation for a second-order sigma-delta modulator is:

$$y = z^{-2}x + (1 - z^{-1})^2E$$

where E is the quantization error. As is also well known to those skilled in the art, the standard equation for a first-order sigma-delta modulator is:

$$y = z^{-1}x + (1 - z^{-1})E.$$

Applying the standard equations to FIG. 1 yields:

1) $y_1 = z^{-2}x + (1-z^{-1})^2E_1$;

2) $y_2 = \frac{1}{C_1}z^{-1}y_1 - \frac{1}{C_1}z^{-1}E_1 + (1-z^{-1})E_2$; and

3) $y_3 = \frac{1}{C_2}z^{-1}y_2 - \frac{1}{C_2}z^{-1}E_2 + (1-z^{-1})E_3$.

To determine the most straightforward and useful correction logic, it is necessary to combine y_1, y_2, and y_3 so that the combined overall output ("y_{out}") is only a function of the input, x, and E_3 (which is fourth-order shaped).

This goal can be accomplished as follows:

Step 1) Multiply y_3 by C_2, resulting in y_4:

$$y_4 = z^{-1}y_2 - z^{-1}E_2 + C_2(1 - z^{-1})E_3$$

Step 2) Subtract $z^{-1}y_2$ from y_4, resulting in y_5:

$$y_5 = -z^{-1}E_2 + C_2(1 - z^{-1})E_3$$

Step 3) Multiply y_5 by $(1-z^{-1})$, resulting in y_6:

$$y_6 = -z^{-1}(1 - z^{-1})E_2 + C_2(1 - z^{-1})^2E_3$$

Step 4) Multiply y_2 by z^{-1}, resulting in y_7:

$$y_7 = \frac{1}{C_1}z^{-2}y_1 - \frac{1}{C_1}z^{-2}E_1 + z^{-1}(1 - z^{-1})E_2$$

Step 5) Add $y_6 + y_7$, resulting in y_8:

$$y_8 = \frac{1}{C_1}z^{-2}y_1 - \frac{1}{C_1}z^{-2}E_1 + C_2(1 - z^{-1})^2E_3$$

Step 6) Multiply y_8 by C_1, resulting in y_9:

$$y_9 = z^{-2}y_1 - z^{-2}E_1 + C_1C_2(1 - z^{-1})^2E_3$$

Step 7) Subtract $z^{-2}y_1$ from y_9, resulting in y_{10}:

$$y_{10} = -z^{-2}E_1 + C_1C_2(1 - z^{-1})^2E_3$$

Step 8) Multiply y_{10} by $(1-z^{-1})^2$, resulting in y_{11}:

$$y_{11} = -z^{-2}(1 - z^{-1})^2E_1 + C_1C_2(1 - z^{-1})^4E_3$$

Step 9) Multiply y_1 by z^{-2} yielding y_{12}:

$$y_{12} = z^{-4}x + z^{-2}(1 - z^{-1})^2E_1$$

Step 10) Add $y_{11} + y_{12}$, resulting in y_{out}:

$$y_{out} = z^{-4}x + C_1C_2(1 - z^{-1})^4E_3$$

The foregoing can be converted to block diagram form as depicted in FIG. 2. Thus the y_1, y_2, and y_3 outputs depicted in FIG. 1 and therein labeled with reference numerals 18, 20, and 22, respectively, which are generated in the circuit of FIG. 1 when an input x (labeled with reference numeral 24) is applied to it, can be "corrected" with the circuit of FIG. 2 to yield an overall output, y_{out} 30, that is a function only of the input x 24 and E_3 26 (which is fourth-order shaped).

Beginning with the same three equations set forth above, i.e.,

1) $y_1 = z^{-2}x + (1-z^{-1})^2E_1$;

2) $y_2 = \frac{1}{C_1}z^{-1}y_1 - \frac{1}{C_1}z^{-1}E_1 + (1-z^{-1})E_2$; and

3) $y_3 = \frac{1}{C_2}z^{-1}y_2 - \frac{1}{C_2}z^{-1}E_2 + (1-z^{-1})E_3$.

an alternative correction network can be obtained by performing the following steps:

Step 1) $y_4 = C_1y_2$
$= z^{-1}y_1 - z^{-1}E_1 + C_1(1-z^{-1})E_2$

Step 2) $y_5 = y_4 - z^{-1}y_1$
$= -z^{-1}E_1 + C_1(1-z^{-1})E_2$

Step 3) $y_6 = C_2y_3$
$= z^{-1}y_2 - z^{-1}E_2 + C_2(1-z^{-1})E_3$

Step 4) $y_7 = y_6 - z^{-1}y_2$
$= -z^{-1}E_2 + C_2(1-z^{-1})E_3$

Step 5) $y_8 = C_1(1-z^{-1})y_7$
$= -z^{-1}C_1(1-z^{-1})E_2 + C_1C_2(1-z^{-1})^2E_3$

Step 6) $y_9 = z^{-1}y_5$
$= -z^{-2}E_1 + C_1z^{-1}(1-z^{-1})E_2$

Step 7) $y_{10} = y_8 + y_9$

$= -z^{-2}E_1 + C_1C_2\,(1-z^{-1})^2E_3$

Step 8) $y_{11} = z^{-2}\,y_1$

$= z^{-4}\,x + z^{-2}\,(1-z^{-1})^2E_1$

Step 9) $y_{12} = (1-z^{-1})^2y_{10}$

$= -z^{-2}\,(1-z^{-1})^2E_1 + C_1C_2\,(1-z^{-1})^4E_3$

Step 10) $y_{out} = y_{11} + y_{12}$

$= z^{-4}\,x + C_1C_2\,(1-z^{-1})^4E_3$

The foregoing can be converted to block diagram form as depicted in FIG. 3.

Still yet another alternative "correction network" can be obtained as follows. Beginning with:

1) $y_1 = z^{-2}\,x + (1-z^{-1})^2E_1$;

2) $y_2 = \frac{1}{C_1}\,z^{-1}y_1 - \frac{1}{C_1}\,z^{-1}E_1 + (1-z^{-1})E_2$; and

3) $y_3 = \frac{1}{C_2}\,z^{-1}y_2 - \frac{1}{C_2}\,z^{-1}E_2 + (1-z^{-1})E_3$,

one can perform the following steps:

Step 1) Multiply y_2 by C_1, resulting in y_4:

$y_4 = z^{-1}y_1 - z^{-1}E_1 + C_1(1 - z^{-1})E_2$

Step 2) Subtract $z^{-1}y_1$ from y_4, resulting in y_5:

$y_5 = -z^{-1}E_1 + C_1(1 - z^{-1})E_2$

Step 3) Multiply y_5 by $(1-z^{-1})^2$, resulting in y_6:

$y_6 = -z^{-1}(1 - z^{-1})^2E_1 + C_1\,(1 - z^{-1})^3E_2$

Step 4) Multiply y_1 by z^{-1}, resulting in y_7:

$y_7 = z^{-3}\,x + z^{-1}\,(1 - z^{-1})^2E_1$

Step 5) Add y_6 to y_7, resulting in y_8:

$y_8 = z^{-3}x + C_1(1 - z^{-1})^3E_2$

Step 6) Multiply y_3 by C_2, resulting in y_9:

$y_9 = z^{-1}y_2 - z^{-1}E_2 + C_2(1 - z^{-1})E_3$

Step 7) Subtract $z^{-1}y_2$ from y_9, resulting in y_{10}:

$y_{10} = -z^{-1}E_2 + C_2\,(1 - z^{-1})E_3$

Step 8) Multiply y_{10} by $(1-z^{-1})^3$, resulting in y_{11}:

$y_{11} = -z^{-1}\,(1 - z^{-1})^3E_2 + C_2(1 - z^{-1})^4E_3$

Step 9) Multiply y_{11} by C_1, resulting in y_{12}:

$y_{12} = -C_1\,z^{-1}\,(1 - z^{-1})^3\,E_2 + C_1C_2\,(1 - z^{-1})^4E_3$

Step 10) Multiply y_8 by z^{-1}, resulting in y_{13}:

$y_{13} = z^{-4}\,x + C_1z^{-1}(1 - z^{-1})^3$

Step 11) Add y_{12} to y_{13}, resulting in y_{out}:

$y_{out} = z^{-4}x + C_1C_2(1 - z^{-1})^4E_3$

The foregoing can be converted to block diagram form as depicted in FIG. 4.

Referring now to FIG. 5, there is shown a plot of simulated Signal to Noise (SNR) performance for a "modified 2-1-1" modulator according to the teachings of the present invention with $C_1 = 4$ and $C_2 = 2$.

Based upon the foregoing, those skilled in the art should understand and appreciate how the present invention provides a new method of cascading three sigma-delta modulators. According to the teachings of the present invention, the input of the quantizer (E_1, E_2, E_3) of each stage is fed to the subsequent stage. Thus, the signal which is fed to each of the subsequent stages is the difference between the output of the previous stage and the quantization noise of the previous stage. Embodiments of the present invention include a correction network (three examples of which are explicitly depicted herein) which removes both the quantization noise of the first two stages, as well as the output of the first two stages. The final output, y_{out}, of embodiments of the present invention is a delayed version of the input, plus a scaled version of the last stage which has been shaped with a fourth-order high pass function. Embodiments of the present invention constitute a marked advance over the prior art, insofar as they constitute improved fourth-order sigma-delta modulators, improved systems and methods for accomplishing high resolution A/D conversion, and insofar as they can provide an A/D converter in which fewer subtractions must take place between stages as compared to prior art converters and, thus, in which fewer analog components are required.

Obviously, numerous modifications and variations are possible in view of the above teachings. Accordingly, within the scope of the appended claims, the present invention may be practiced otherwise than as specifically described hereinabove.

Claims

1. A method of cascading three sigma-delta modulators; each of said three sigma-delta modulators constituting a stage; said three stages interrelated as a first, a second, and a third stage; each of said stages having a quantizer; said method comprising the steps of:

   obtaining the input to said quantizer of said first stage;

   feeding the input to said quantizer of said first stage to said second stage;

   obtaining the input to said quantizer of said second stage;

   feeding the input to said quantizer of said second stage to said third stage; and

   from the final, third stage output signal, removing the quantization noise of said first stage and said second stage, and further removing said output of said first stage and said second stage, whereby the final output of said cascaded three sigma-delta modulators is a delayed version of the input thereto plus a scaled version of the quantization noise of the third stage which has been shaped with a fourth-order high pass filter.

2. The method as recited in claim 1, wherein said first stage comprises a second-order sigma-delta modulator.

3. The method as recited in claim 2, wherein said second stage comprises a first-order sigma-delta modulator.

4. The method as recited in claim 3, wherein said third stage comprises a first-order sigma-delta

modulator.

5. The method as recited in claim 1, wherein said step of removing is accomplished by applying the following equation;

$$y_{out} = z^{-4}x + C_1C_2(1 - z^{-1})^4E_3$$

where x is the input, z values arise from integration operations, E_3 is the quantization noise of the third stage, and C_1 and C_2 are constants.

6. A sigma-delta modulator system; said system including three sigma-delta modulators; each of said three sigma-delta modulators constituting a stage; said three stages interrelated as a first, a second and a third stage, each of said stages having a quantizer; said system comprising:

means for obtaining the input to said quantizer of said first stage;

means for feeding the input to said quantizer of said first stage to said second stage;

means for obtaining the input to the quantizer of said second stage;

means for feeding the input to said quantizer of said second stage to said third stage; and

means for, from the final, third stage output signal, removing the quantization noise of said first stage and said second stage, and further removing said output of said first stage and said second stage, whereby the final output of said system is a delayed version of the input thereto plus a scaled version of the quantization noise of the third stage which has been shaped with a fourth-order high pass filter.

7. The system as recited in claim 6, wherein said first stages comprises a second-order sigma-delta modulator.

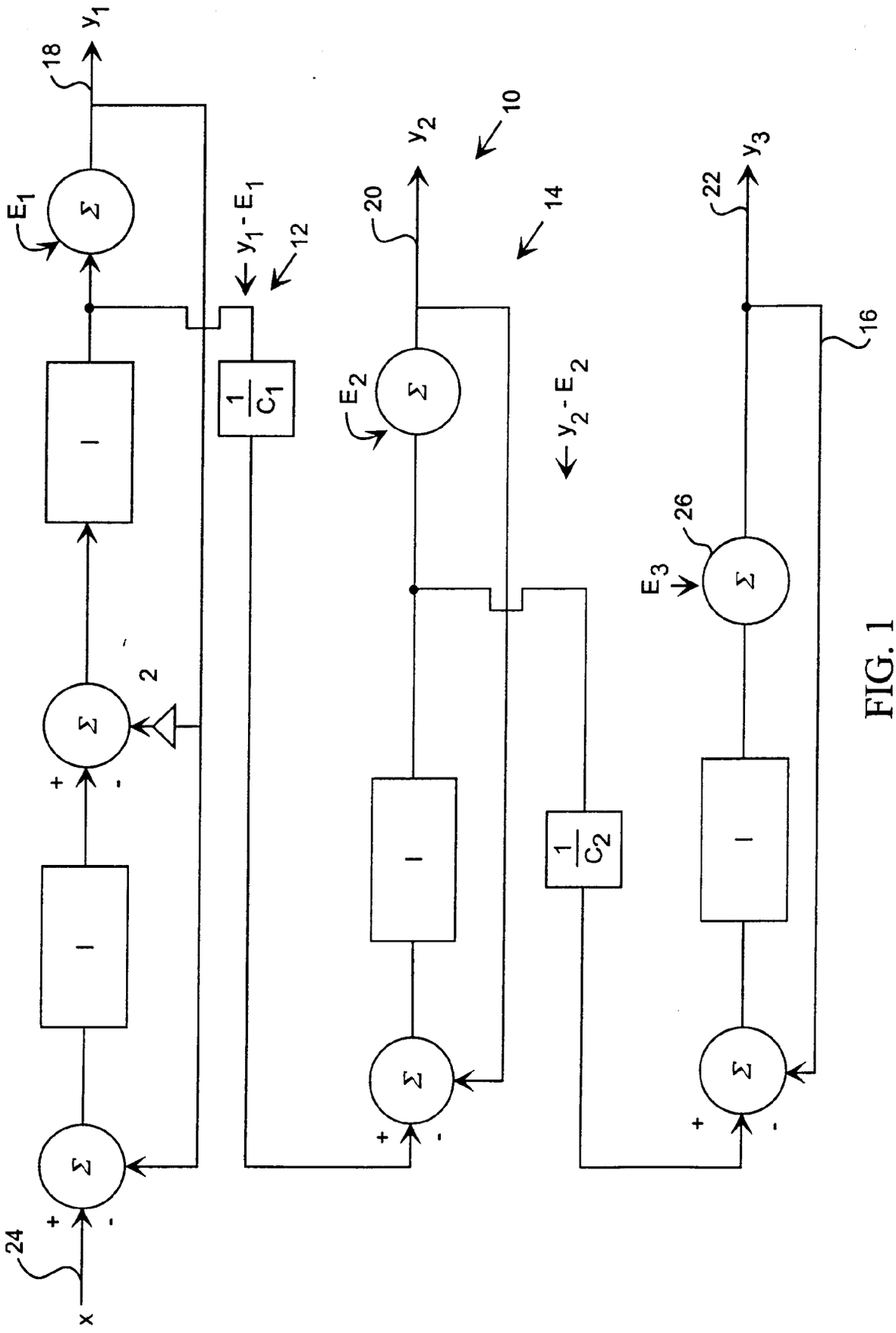
8. The system as recited in claim 7, wherein said second stage comprises a first-order sigma-delta modulator.

9. The system as recited in claim 8, wherein said third stage comprises a first-order sigma delta modulator.

10. The system as recited in claim 6, wherein said means for removing comprises means for applying the following equation:

$$y_{out} = z^{-4}x + C_1C_2(1 - z^{-1})^4E_3$$

where x is the input, z values arise from integration operations, E_3 is the quantization noise of the third stage, and C_1 and C_2 are constants.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y2
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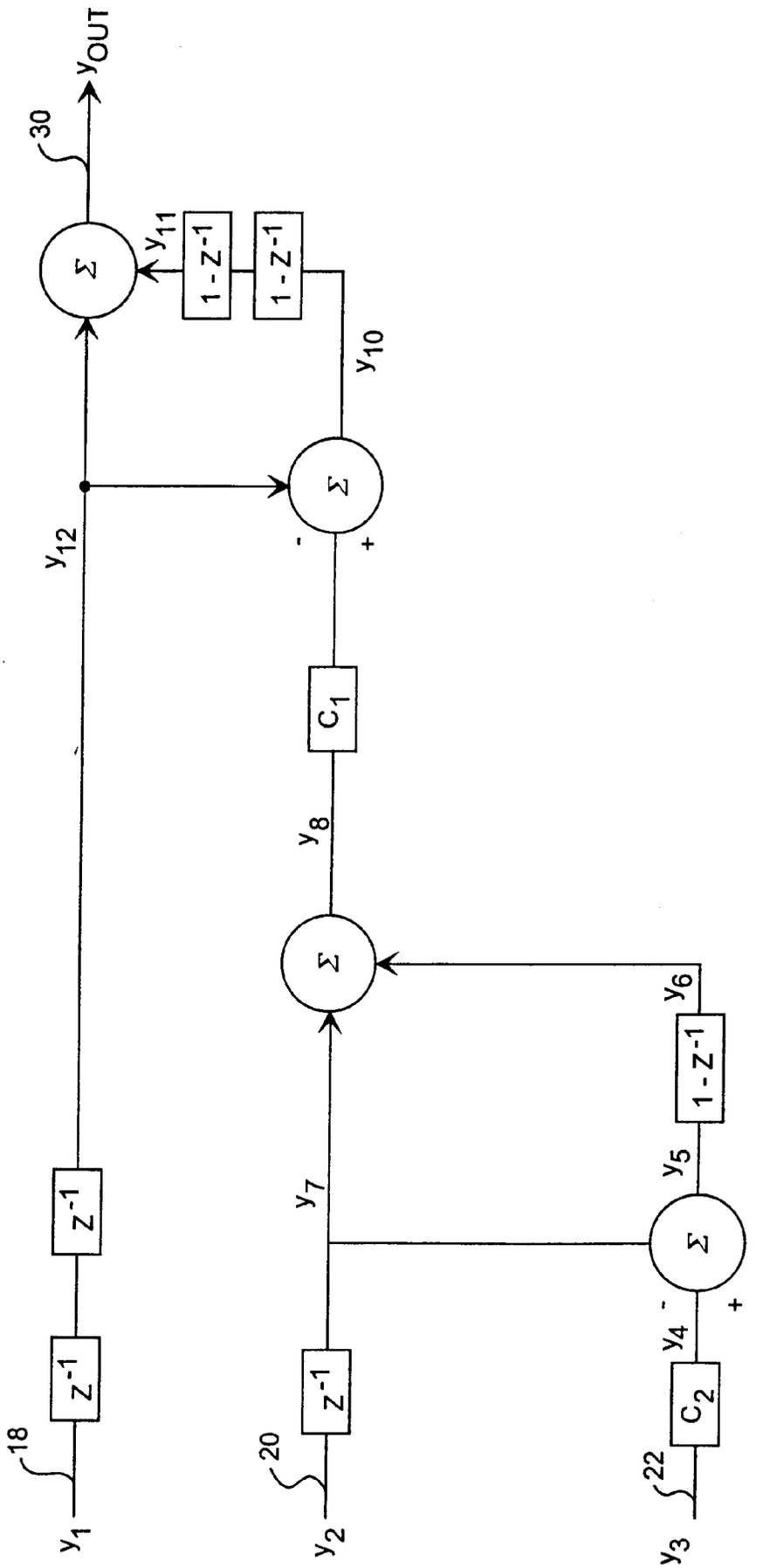
FIG. 1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30
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y_{11}
$1 - z^{-1}$
$1 - z^{-1}$
y_{10}
Σ
-
+
y_{12}
C_1
y_8
Σ
y_6
$1 - z^{-1}$
y_5
y_7
Σ
-
+
y_4
C_2
z^{-1}
z^{-1}
18
20
22
y_1
y_2
y_3

FIG. 2

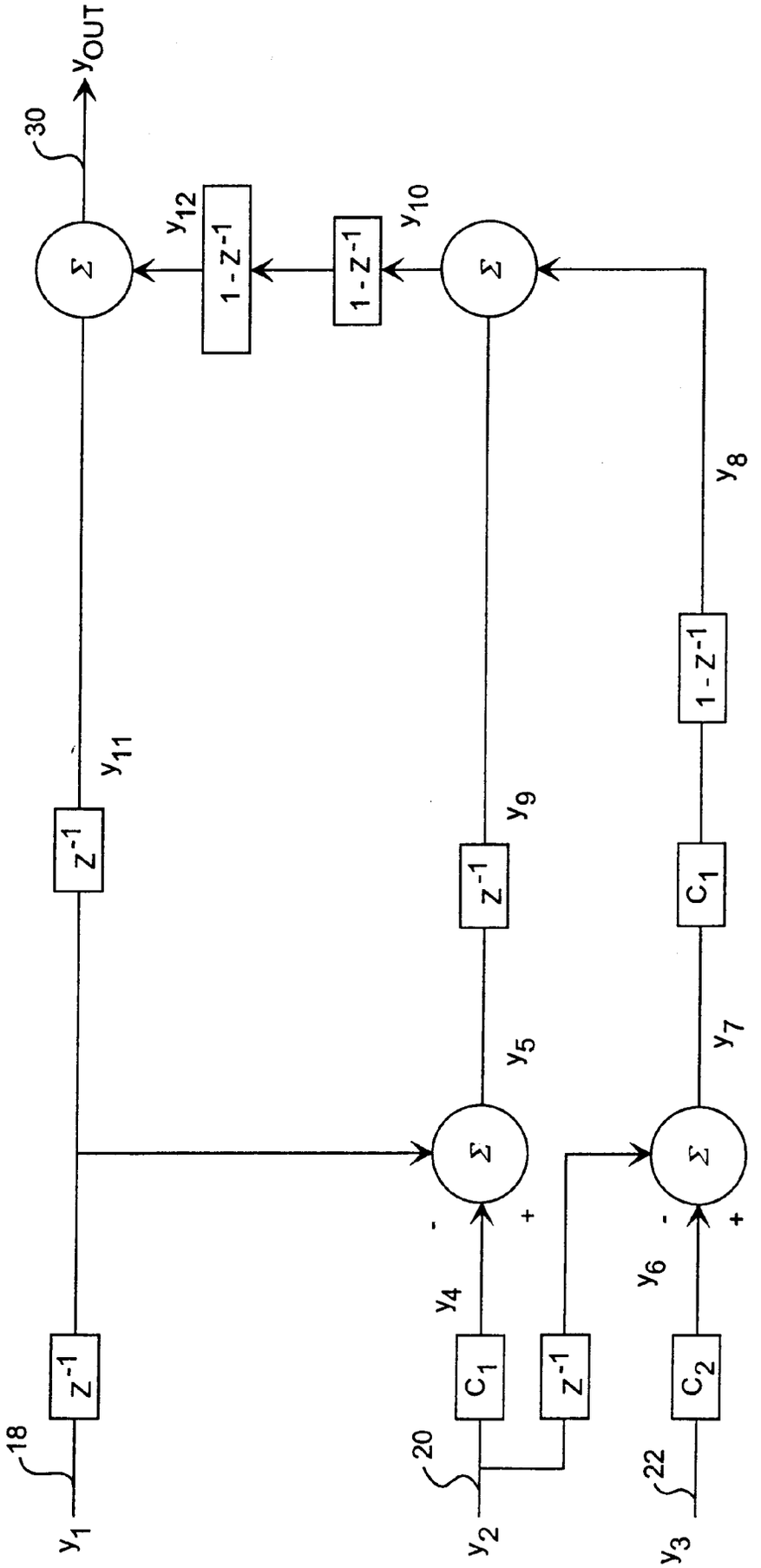

y_{OUT}
30
y_{12}
y_{10}
y_8
y_{11}
y_9
y_5
y_7
y_4
y_6
18
20
22
y_1
y_2
y_3
z^{-1}
$1 - z^{-1}$
C_1
C_2
Σ
+
-

FIG. 3

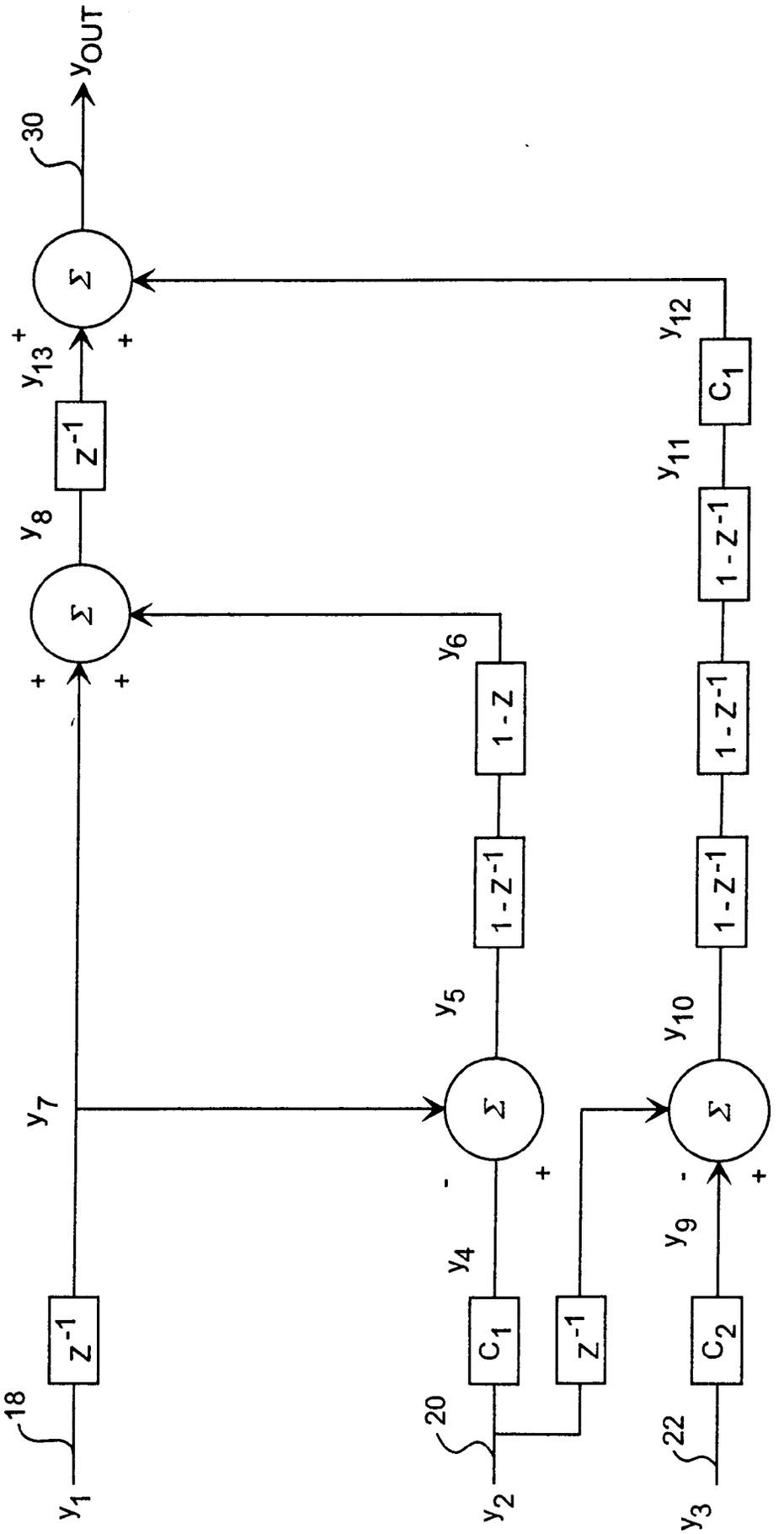
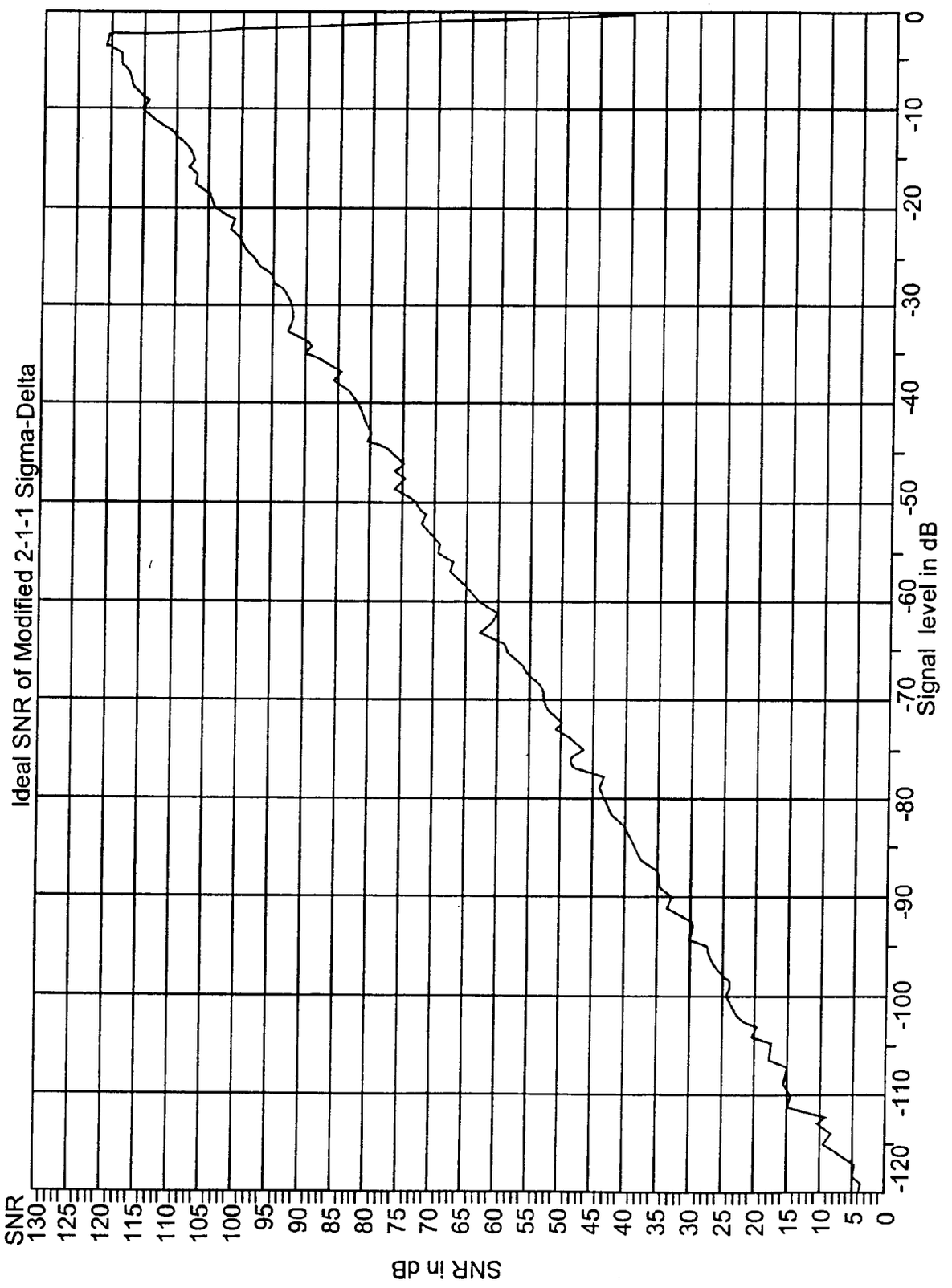

y_{OUT}
30
y_{13}
y_8
y_7
y_6
y_5
y_4
y_{12}
y_{11}
y_{10}
y_9
18
20
22
y_1
y_2
y_3
z^{-1}
C_1
C_2
$1 - z$
$1 - z^{-1}$
Σ
+
-

FIG. 4

FIG. 5


Ideal SNR of Modified 2-1-1 Sigma-Delta
SNR
SNR in dB
Signal level in dB
130
125
120
115
110
105
100
95
90
85
80
75
70
65
60
55
50
45
40
35
30
25
20
15
10
5
0
-120
-110
-100
-90
-80
-70
-60
-50
-40
-30
-20
-10
0

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 94 30 7873

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS, vol.38, no.2, February 1991, NEW YORK US, XP000224212 D. B. RIBNER 'A Comparision of Modulator Networks for High-Order Oversampled Sigma Delta Analog-to-Digital Converters' * page 149, right column, paragraph 3 - page 150, right column, last paragraph; figures 6,7 * ---	1-5	H03M3/02
A	US-A-5 084 702 (D. B. RIBNER) * column 15, line 5 - line 37; figure 8 * -----	1-5	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

H03M

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	20 December 1994	Blaas, D-L

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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