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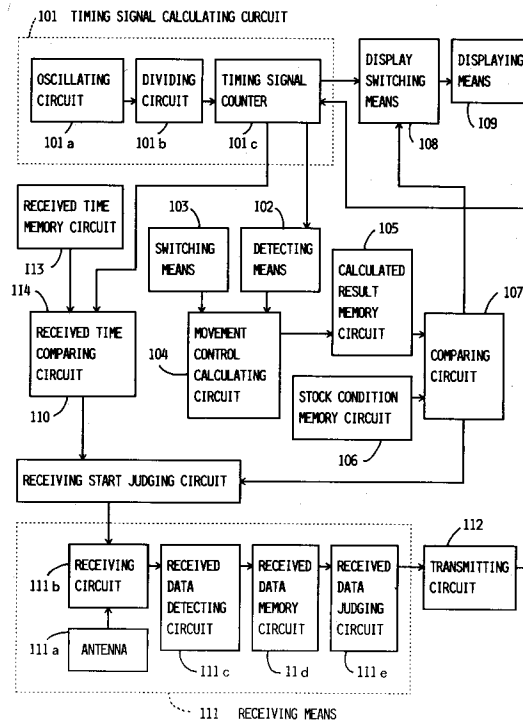
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54 **Radio-corrected electronic timepiece.**

57 A radio-corrected electronic timepiece by placing it into a power save state according to whether or not the user is actually using the timepiece.

A detecting means 102 detects whether not the timepiece is in use. A stock condition memory circuit 106 stores power save mode conditions. A comparing circuit 107 makes a comparison between output signals from a calculated result memory circuit 105 and the stock condition memory circuit 106. A receiving start judging circuit 110 judges whether or not a receiving means 111 should be started. A display switching means 108 judges whether or not timing and other information should be outputted to a displaying means 109 on the basis of a result of the comparison made by the comparing circuit 107.

FIG. 1



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BACKGROUND OF THE INVENTION

The present invention relates to a radio-corrected electronic timepiece which is designed so that the current consumption is reduced, and accurate time is obtained.

Conventional radio-corrected electronic timepieces have heretofore been arranged to automatically enter a receiving state every predetermined time until the battery becomes dead.

Fig. 3 is a system block diagram of a conventional electronic timepiece. A received time comparing circuit 306 is supplied with an output signal from a timing signal calculating circuit 301, which arithmetically processes timing and other information, and an output signal from a received time memory circuit 305 previously stored with predetermined time (time at which receiving is to be started), and makes a comparison to judge whether or not timing data obtained from the timing signal calculating circuit 301 matches timing data stored in the received time memory circuit 305. When the result of the comparison shows that the two pieces of timing data match each other, a receiving means 302 is activated. The receiving means 302 is normally in a receiving stop state, but when brought into a receiving start state, it receives an externally transmitted standard timing signal, judges whether or not the received data has predetermined information and outputs a signal to a transmitting circuit 303 that outputs a correction pulse to the timing signal calculating circuit 301. A displaying means 304 is supplied with an output signal from the timing signal calculating circuit 301 and displays timing and other information.

The above-described conventional structure is disclosed in, for example, Japanese Patent Application Laid-Open JP-A-54-97462(1979).

However, the conventional radio-corrected electronic timepiece performs receiving until a power source, e.g., a battery, becomes dead regardless of whether or not the user carries (uses) it.

SUMMARY OF THE INVENTION

Accordingly, an object of the present invention is to provide an electronic timepiece arranged such that whether or not the user carries (uses) the electronic timepiece is detected, and when the user does not carry (use) it, the timepiece is inhibited from receiving; in the case of a digital timepiece, an LCD or the like is turned off to place the timepiece into a power save state, thereby extending the battery lifetime. It is another object of the present invention to provide a radio-corrected electronic timepiece which is compellingly placed into a receiving state when it is detected that the

timepiece has been brought into a carried (used) state from a non-carried (unused) state, thereby enabling the timepiece to display accurate time.

To attain the above-described problem, the present invention provides a radio-corrected electronic timepiece comprising: detecting means for detecting whether or not the timepiece is in use on the basis of an output signal from a timing signal calculating circuit; a movement control calculating circuit for arithmetically processing output signals from the detecting means and switching means; a calculated result memory circuit for storing an output signal from the movement control calculating circuit; a stock condition memory circuit for storing conditions under which operations of receiving means and so forth are stopped; a comparing circuit for making a comparison between an output signal from the calculated result memory circuit and an output signal from the stock condition memory circuit; a receiving start judging circuit for judging whether or not the receiving means should be started on the basis of an output signal from a received time comparing circuit and an output signal from the comparing circuit and for outputting a result of the judgment to the receiving means; and display switching means for receiving the output signals from the timing signal calculating circuit and the comparing circuit and for judging whether or not the output signal from the timing signal calculating circuit should be outputted to displaying means for displaying timing and other information on the basis of a result of the comparison made by the comparing circuit.

In addition, the present invention provides a radio-corrected electronic timepiece comprising: detecting means for detecting whether or not the timepiece is in use on the basis of an output signal from a timing signal calculating circuit; a movement control calculating circuit for arithmetically processing output signals from the detecting means and switching means; a calculated result memory circuit for storing an output signal from the movement control calculating circuit; a stock condition memory circuit for storing conditions under which operations of receiving means and so forth are stopped; a comparing circuit for making a comparison between an output signal from the calculated result memory circuit and an output signal from the stock condition memory circuit; a receiving start judging circuit for judging whether or not the receiving means should be started on the basis of an output signal from received time comparing circuit and an output signal from the comparing circuit and for outputting a result of the judgment to the receiving means; a compelled receiving start circuit for activating the receiving means when an output signal from the comparing circuit changes from a match state to a mismatch state; and display switching

means for receiving the output signals from the timing signal calculating circuit and the comparing circuit and for judging whether or not the output signal from the timing signal calculating circuit should be outputted to displaying means for displaying timing and other information on the basis of a result of the comparison made by the comparing circuit.

Fig. 1 is a system block diagram showing one example of a typical arrangement of the radio-corrected electronic timepiece according to the present invention.

A timing signal calculating circuit 101 arithmetically processes timing and other information. A detecting means 102 is supplied with an output signal from the timing signal calculating circuit 101 and activates a photo sensor, a temperature sensor or other circuit to detect whether or not the timepiece is in use. A switching means 103 judges whether or not an external operating member has been activated. A movement control calculating circuit 104 arithmetically processes output signals from the detecting means 102 and switching means 103. A calculated result memory circuit 105 stores an output signal from the movement control calculating circuit 104. A stock condition memory circuit 106 stores conditions under which the timepiece is placed into a power save mode in which, for example, the display is turned off, or receiving is inhibited. A comparing circuit 107 makes a comparison between an output signal from the calculated result memory circuit 105 and an output signal from the stock condition memory circuit 106.

A receiving means 111 is normally in a receiving stop state, but when brought into a receiving start state, it receives an externally transmitted standard timing signal, and judges whether or not the received data has predetermined information. A transmitting circuit 112 receives an output signal from the receiving means 111 and outputs a correction pulse to the timing signal calculating circuit 101. A received time memory circuit 113 stores predetermined time (time at which receiving is to be started). A received time comparing circuit 114 makes a comparison between an output signal from the timing signal calculating circuit 101 and an output signal from the received time memory circuit 113. A receiving start judging circuit 110 judges whether or not the receiving means 111 should be started on the basis of output signals from the received time comparing circuit 114 and the comparing circuit 107, and outputs a result of the judgment to the receiving means 111. A display switching means 108 receives the output signals from the timing signal calculating circuit 101 and the comparing circuit 107 and judges whether or not the output signal from the timing signal cal-

culating circuit 101 should be outputted to a displaying means 109 for displaying timing and other information on the basis of a result of the comparison made by the comparing circuit 107.

Fig. 2 is a system block diagram showing another example of a typical arrangement of the radio-corrected electronic timepiece according to the present invention.

A timing signal calculating circuit 201 arithmetically processes timing and other information. A detecting means 202 is supplied with an output signal from the timing signal calculating circuit 201 and activates a photo sensor, a temperature sensor or other circuit to detect whether or not the timepiece is in use. A switching means 203 judges whether or not an external operating member has been activated. A movement control calculating circuit 204 arithmetically processes output signals from the detecting means 202 and switching means 203. A calculated result memory circuit 205 stores an output signal from the movement control calculating circuit 204. A stock condition memory circuit 206 stores conditions under which the timepiece is placed into a power save mode in which, for example, the display is turned off, or receiving is inhibited. A comparing circuit 207 makes a comparison between an output signal from the calculated result memory circuit 205 and an output signal from the stock condition memory circuit 206.

A receiving means 211 is normally in a receiving stop state, but when brought into a receiving start state, it receives an externally transmitted standard timing signal, and judges whether or not the received data has predetermined information. A transmitting circuit 212 receives an output signal from the receiving means 211 and outputs a correction pulse to the timing signal calculating circuit 201. A received time memory circuit 213 stores predetermined time (time at which receiving is to be started). A received time comparing circuit 214 makes a comparison between an output signal from the timing signal calculating circuit 201 and an output signal from the received time memory circuit 213. A receiving start judging circuit 210 judges whether or not the receiving means 211 should be started on the basis of output signals from the received time comparing circuit 214 and the comparing circuit 207, and outputs a result of the judgment to the receiving means 211. A compelled receiving start circuit 215 activates the receiving means 211 when an output signal from the comparing circuit 207 changes from a match state to a mismatch state. A display switching means 208 receives the output signals from the timing signal calculating circuit 201 and the comparing circuit 207 and judges whether or not the output signal from the timing signal calculating circuit 201

should be outputted to a displaying means 209 for displaying timing and other information on the basis of a result of the comparison made by the comparing circuit 207.

Thus, the radio-corrected electronic timepiece of the present invention judges whether or not the user is actually carrying (using) the timepiece, and controls the receiving circuit or display according to a result of the judgment, thereby enabling the current consumption to be reduced. When it is detected that the timepiece has been brought into a carried (used) state from a non-carried (unused) state, the timepiece is compellingly placed into a receiving state at once, thereby allowing the timepiece to display accurate time.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a system block diagram showing one example of a typical arrangement of the radio-corrected electronic timepiece according to the present invention.

Fig. 2 is a system block diagram showing another example of a typical arrangement of the radio-corrected electronic timepiece according to the present invention.

Fig. 3 is a functional block diagram of a conventional radio-corrected electronic timepiece.

Fig. 4 is a detailed block diagram showing a receiving start judging circuit and a stock condition comparing circuit, together with peripheral circuits thereof, in a first embodiment of the radio-corrected electronic timepiece according to the present invention.

Fig. 5 is a flowchart schematically showing operations of a received time comparing circuit, stock condition comparing circuit and receiving start judging circuit in the first embodiment of the radio-corrected electronic timepiece according to the present invention.

Fig. 6 is a detailed timing chart of receiving start processing and LCD display ON/OFF control, which are executed when the timepiece is brought into a stock condition from a non-stock condition in the first embodiment of the radio-corrected electronic timepiece according to the present invention.

Fig. 7 is a detailed block diagram showing a compelled receiving start circuit, a receiving start judging circuit and a stock condition comparing circuit, together with peripheral circuits thereof, which are arranged to compel the timepiece to perform receiving when it returns to a normal condition from a stock condition in a second embodiment of the radio-corrected electronic timepiece according to the present invention.

Fig. 8 is a flowchart schematically showing stock condition setting and canceling processing in the second embodiment of the radio-corrected

electronic timepiece according to the present invention.

Fig. 9 is a detailed timing chart of receiving start processing and LCD display ON/OFF control, which accompany the stock condition setting and canceling processing, in the second embodiment of the radio-corrected electronic timepiece according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Embodiments of the present invention will be described below with reference to the accompanying drawings.

(1) First Embodiment

Figs. 4, 5 and 6 relate to a radio-corrected electronic timepiece according to the present invention arranged such that when the timepiece is found to be in such conditions that it has been impossible to detect light for 10 days and the external switch has not been pressed for 10 days (i.e., stock condition), the LCD display is turned off, and the timepiece is inhibited from performing receiving, which is carried out at 2 o'clock every day.

Fig. 4 is a detailed block diagram of an arrangement for ON/OFF controlling the LCD display and judging whether or not the receiving circuit should be activated according to whether or not the timepiece is in the stock condition. A received time memory circuit 401, which is comprised of a ROM, stores data "2 o'clock 00 minute". A received time comparing circuit 403 makes a comparison to judge whether or not the data stored in the received time memory circuit 401 and the data of a timing signal counter 402 match each other. As long as the two pieces of data match each other, a HIGH signal is outputted.

A stock condition memory circuit 404, which is comprised of a ROM, has previously been stored with data "10 days". A movement control calculating circuit 407 resets calculation data when an external switch 405 is pressed, or a photo sensor 406 detects light. When the date has changed without the external switch 405 being pressed and without the photo sensor 406 detecting light, the movement control calculating circuit 407 adds "1" to the calculation data. A calculated result memory circuit 408 stores the data calculated by the movement control calculating circuit 407. A stock condition comparing circuit 409 makes a comparison to judge whether or not the data stored in the stock condition memory circuit 404 and the data of the calculated result memory circuit 408 match each other. As long as the two pieces of data match each other, a HIGH signal is outputted.

A receiving start judging circuit 410 is comprised of a 2-input AND gate 410a which is supplied at one input end thereof with an output signal from the received time comparing circuit 403 and which is supplied at another input end thereof with an output signal from the stock condition comparing circuit 409 through an inverter 410b.

A receiving circuit 411 is supplied with an output signal from the receiving start judging circuit 410 as an input signal. When it is detected that the input signal has risen from LOW to HIGH, the receiving circuit 411 is activated.

An LCD ON/OFF switching circuit 412 is supplied with an output signal from the stock condition comparing circuit 409 as an input signal. When the input signal is LOW, the switching circuit 412 turns on the LCD display (i.e., timing information display state), whereas, when the input signal is HIGH, the switching circuit 412 turns off the LCD display.

Fig. 5 is a flowchart schematically showing the operations of the received time comparing circuit 403, the stock condition comparing circuit 409 and the receiving start judging circuit 410. It is judged by the stock condition comparing circuit 409 whether or not the timepiece is in such conditions that no switch input has been available and no light has been detected for 10 days (i.e., stock condition) (Step 501). When it is judged that the timepiece is in the stock condition, the LCD display is turned off, and the process is terminated without making judgment for receiving start conditions (Step 502). When it is judged that the timepiece is not in the stock condition, the LCD display is turned on (Step 503), and it is judged by the received time comparing circuit 403 whether or not it is 2 o'clock 00 minute (Step 504). When it is not 2 o'clock 00 minute, the process is terminated as it is. When it is 2 o'clock 00 minute, receiving start processing is executed, and then the process is terminated (Step 505).

Fig. 6 is a detailed timing chart of the receiving start processing and the LCD display ON/OFF control, which are executed when the timepiece is brought into a stock condition (i.e., conditions where no switch input is available and no light is detected for 10 days) from a non-stock condition. It should be noted that the movement control calculating circuit 407 is assumed to be adapted to add "1" to the calculation data when the date has changed. The output signal A from the received time memory circuit 401 has data indicating "2 o'clock 00 minute". The received time comparing circuit 403 is supplied with the signals A and B as input signals. When the signals A and B match each other (i.e., 2 o'clock 00 minute), the output signal E from the received time comparing circuit 403 becomes HIGH.

The output signal C from the stock condition memory circuit 404 has data indicating a given number of days (e.g., 10 days) by which a stock condition judgment is made. The stock condition comparing circuit 409 is supplied with the signals C and D as input signals. When the signals C and D match each other (i.e., when conditions of stock condition are satisfied), the output signals F and H of the stock condition comparing circuit 409 become HIGH.

When the two pieces of data for "2 o'clock 00 minute" first match each other, the signals C and D do not match (i.e., the timepiece is not in the stock condition). Therefore, a receiving start pulse is outputted in the form of the signal G, and the LCD display remains in a normal state. If the next day comes without any switch input and without light being detected thereafter, the signals C and D match each other (i.e., the stock condition). Accordingly, the signals F and H become HIGH, and the LCD display is turned off. When it is 2 o'clock 00 minute on that day, the signals A and B match each other. However, since the signal F outputted from the stock condition comparing circuit 409 is HIGH, the signal G outputted from the 2-input AND gate 410a is LOW. Therefore, the timepiece is inhibited from starting receiving. This state continues until either a switch input or light is detected.

(1) Second Embodiment

Figs. 7, 8 and 9 relate to a radio-corrected electronic timepiece obtained by modifying the first embodiment of the present invention such that the timepiece is compelled to perform receiving when it returns to the normal condition from the stock condition (where no receiving is permitted and the LCD is off).

Fig. 7 is a detailed block diagram showing a compelled receiving start circuit, a receiving start judging circuit and a stock condition comparing circuit, together with peripheral circuits thereof, which are arranged to compel the timepiece to perform receiving when it returns to the normal condition from the stock condition. The arrangement is the same as that described in connection with Fig. 4 with regard to the receiving start judging circuit, the stock condition comparing circuit and their peripheral circuits. The compelled receiving start circuit 713 is supplied with an output signal from the stock condition comparing circuit 709 as an input signal. When the input signal changes from HIGH to LOW, the compelled receiving start circuit 713 outputs a compelled receiving start pulse to the receiving circuit 711.

Fig. 8 is a flowchart schematically showing stock condition setting and canceling processing. Processing executed when neither switch input nor

light has been detected is the same as that described in connection with Fig. 5. When a switch input is available (Step 801) or light is detected (Step 802), data used to calculate a number of days for which neither switch input nor light has been detected is reset (Step 803), and the LCD display is turned on (Step 804). Then, it is judged whether or not the timepiece was in the stock condition when the switch input or light was detected (Step 805). When it is judged that the timepiece was not in the stock condition, the processing carried out at and after Step 504, described in connection with Fig. 5, is executed, whereas, when it is judged that the timepiece was in the stock condition, receiving is immediately started.

Fig. 9 is a detailed timing chart of the receiving start processing and the LCD display ON/OFF control, which accompany the stock condition setting and canceling processing. The timing chart of the receiving start processing the LCD display ON/OFF control, which are executed when the timepiece is brought into a stock condition from a non-stock condition, is the same as that described in connection with Fig. 6. When either a switch input or light is detected in the stock condition, the output signals F, H and I from the stock condition comparing circuit 709 become LOW. When the compelled receiving start circuit 713 detects a fall of the input signal I, it outputs a receiving start pulse signal J to the receiving circuit 711.

The radio-corrected electronic timepiece of the present invention has a detecting means for detecting whether or not the timepiece is in use on the basis of an output signal from a timing signal calculating circuit, a stock condition memory circuit for storing conditions under which the receiving means is inhibited, and a receiving start judging circuit for judging whether or not a receiving means should be started and for outputting a result of the judgment to the receiving means.

Further, the radio-corrected electronic timepiece of the present invention may have a compelled receiving start circuit that activates the receiving means on the basis of an output signal from the detecting means, in addition to the above-described arrangement. Thus, the present invention has the following advantageous effects:

(1) Since the timepiece is inhibited from receiving and effecting display when it is not carried (used) (e.g., during the time interval between the shipment of the timepiece from the factory and the delivery of it to the user), the lifetime of the battery can be extended.

(2) Since the timepiece is automatically placed into a compelled receiving state when it is detected that the timepiece has been brought into a carried (used) state from a non-carried (un-

used) state, accurate time can be obtained.

Claims

- 5 1. A radio-corrected electronic timepiece comprising:
 - 10 a timing signal calculating circuit for arithmetically processing timing and other information;
 - 15 detecting means for detecting whether or not said timepiece is in use on the basis of an output signal from said timing signal calculating circuit;
 - switching means for judging whether or not an external operating member has been activated;
 - a movement control calculating circuit for arithmetically processing output signals from said detecting means and switching means;
 - 20 a calculated result memory circuit for storing an output signal from said movement control calculating circuit;
 - a stock condition memory circuit for storing conditions under which operations of receiving means and so forth are stopped;
 - 25 a comparing circuit for making a comparison between an output signal from said calculated result memory circuit and an output signal from said stock condition memory circuit;
 - 30 said receiving means being arranged such that it is normally in a receiving stop state, but when brought into a receiving start state, said receiving means receives an externally transmitted standard timing signal and judges whether or not the received data has predetermined information;
 - 35 a transmitting circuit for receiving an output signal from said receiving means and for outputting a correction pulse to said timing signal calculating circuit;
 - a received time memory circuit for storing predetermined time at which receiving is to be started;
 - 40 a received time comparing circuit for making a comparison between an output signal from said timing signal calculating circuit and an output signal from said received time memory circuit;
 - 45 a receiving start judging circuit for judging whether or not said receiving means should be started on the basis of an output signal from said received time comparing circuit and an output signal from said comparing circuit and for outputting a result of the judgment to said receiving means; and
 - 50 display switching means for receiving the output signals from said timing signal calculating

ing circuit and comparing circuit and for judging whether or not the output signal from said timing signal calculating circuit should be outputted to displaying means for displaying timing and other information on the basis of a result of the comparison made by said comparing circuit.

2. A radio-corrected electronic timepiece comprising:

a timing signal calculating circuit for arithmetically processing timing and other information;

detecting means for detecting whether or not said timepiece is in use on the basis of an output signal from said timing signal calculating circuit;

switching means for judging whether or not an external operating member has been activated;

a movement control calculating circuit for arithmetically processing output signals from said detecting means and switching means;

a calculated result memory circuit for storing an output signal from said movement control calculating circuit;

a stock condition memory circuit for storing conditions under which operations of receiving means and so forth are stopped;

a comparing circuit for making a comparison between an output signal from said calculated result memory circuit and an output signal from said stock condition memory circuit;

said receiving means being arranged such that it is normally in a receiving stop state, but when brought into a receiving start state, said receiving means receives an externally transmitted standard timing signal and judges whether or not the received data has predetermined information;

a transmitting circuit for receiving an output signal from said receiving means and for outputting a correction pulse to said timing signal calculating circuit;

a received time memory circuit for storing predetermined time at which receiving is to be started;

a received time comparing circuit for making a comparison between an output signal from said timing signal calculating circuit and an output signal from said received time memory circuit;

a receiving start judging circuit for judging whether or not said receiving means should be started on the basis of an output signal from said received time comparing circuit and an output signal from said comparing circuit and

for outputting a result of the judgment to said receiving means;

a compelled receiving start circuit for activating said receiving means when an output signal from said comparing circuit changes from a match state to a mismatch state; and

display switching means for receiving the output signals from said timing signal calculating circuit and comparing circuit and for judging whether or not the output signal from said timing signal calculating circuit should be outputted to displaying means for displaying timing and other information on the basis of a result of the comparison made by said comparing circuit.

3. A radio-corrected electronic timepiece comprising:

stock condition detecting means for detecting a condition of use of said timepiece;

receiving means for receiving an externally transmitted standard timing signal;

received time control means for controlling a time at which said receiving means is to be activated; and

receiving start judging means for judging whether or not an operation of said received time control means should be started on the basis of an output signal from said stock condition detecting means,

said receiving means being activated on the basis of an output signal from said receiving start judging means.

4. A radio-corrected electronic timepiece according to Claim 3, further comprising:

timing signal calculating means for calculating timing and other information;

display switching means for receiving an output signal from said timing signal calculating means and for switching a state of displaying timing and other information on the basis of an output signal from said stock condition detecting means; and

displaying means for displaying time and other information on the basis of an output signal from said display switching means.

5. A radio-corrected electronic timepiece according to Claim 3, further comprising compelled receiving start means for controlling an operation of said receiving means on the basis of an output signal from said stock condition detecting means.

FIG. 1

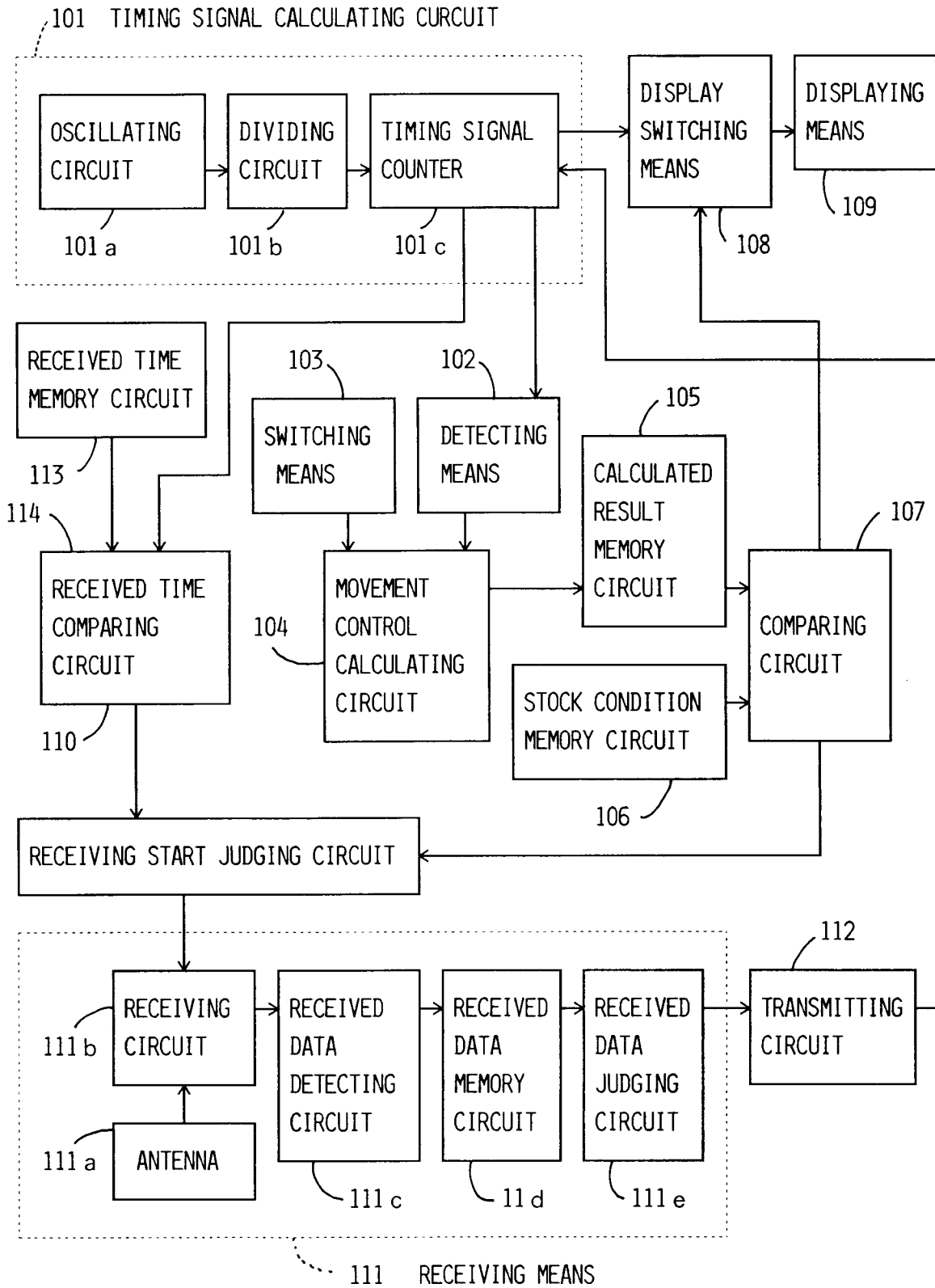


FIG. 2

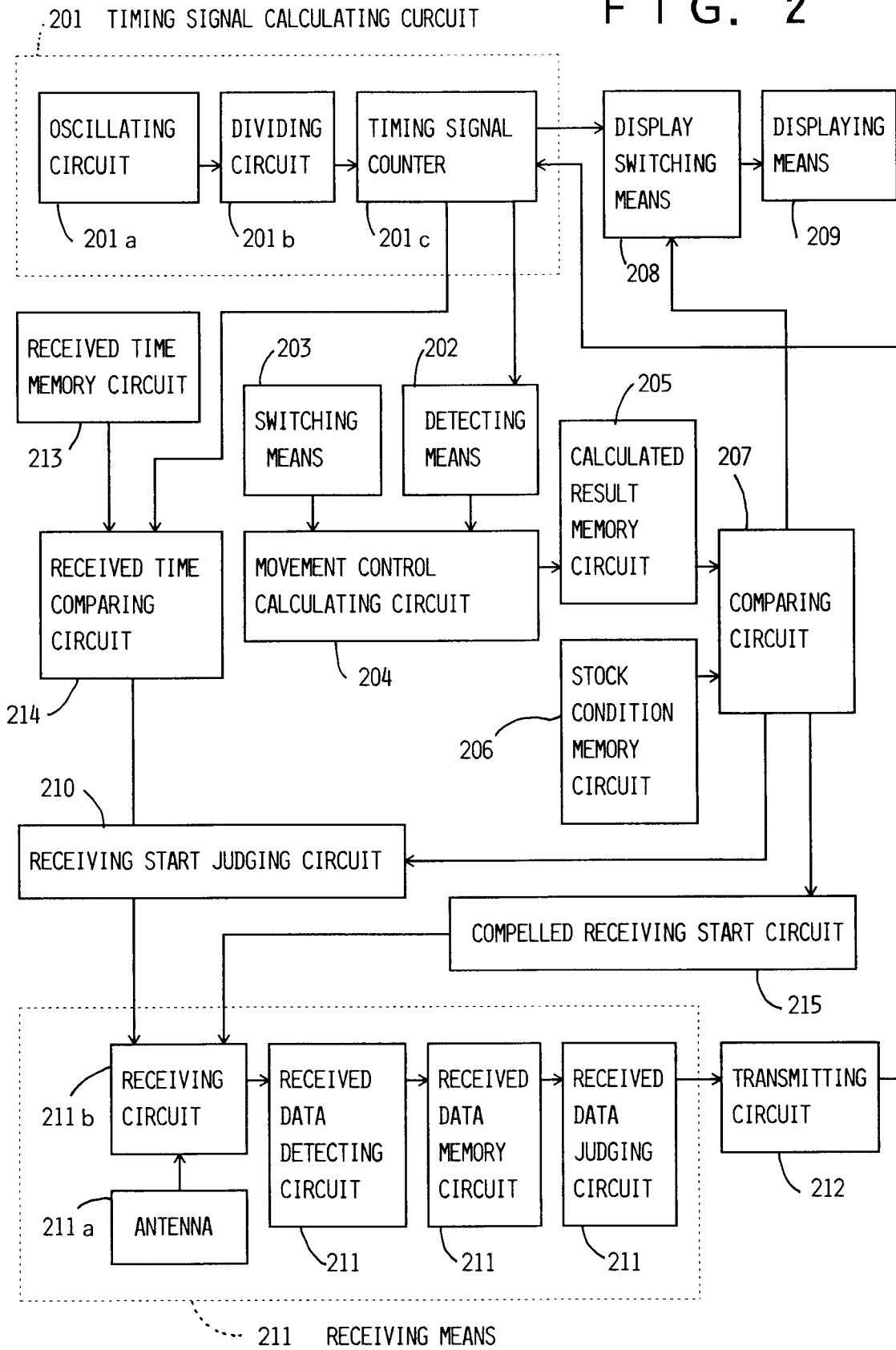


FIG. 3 PRIOR ART

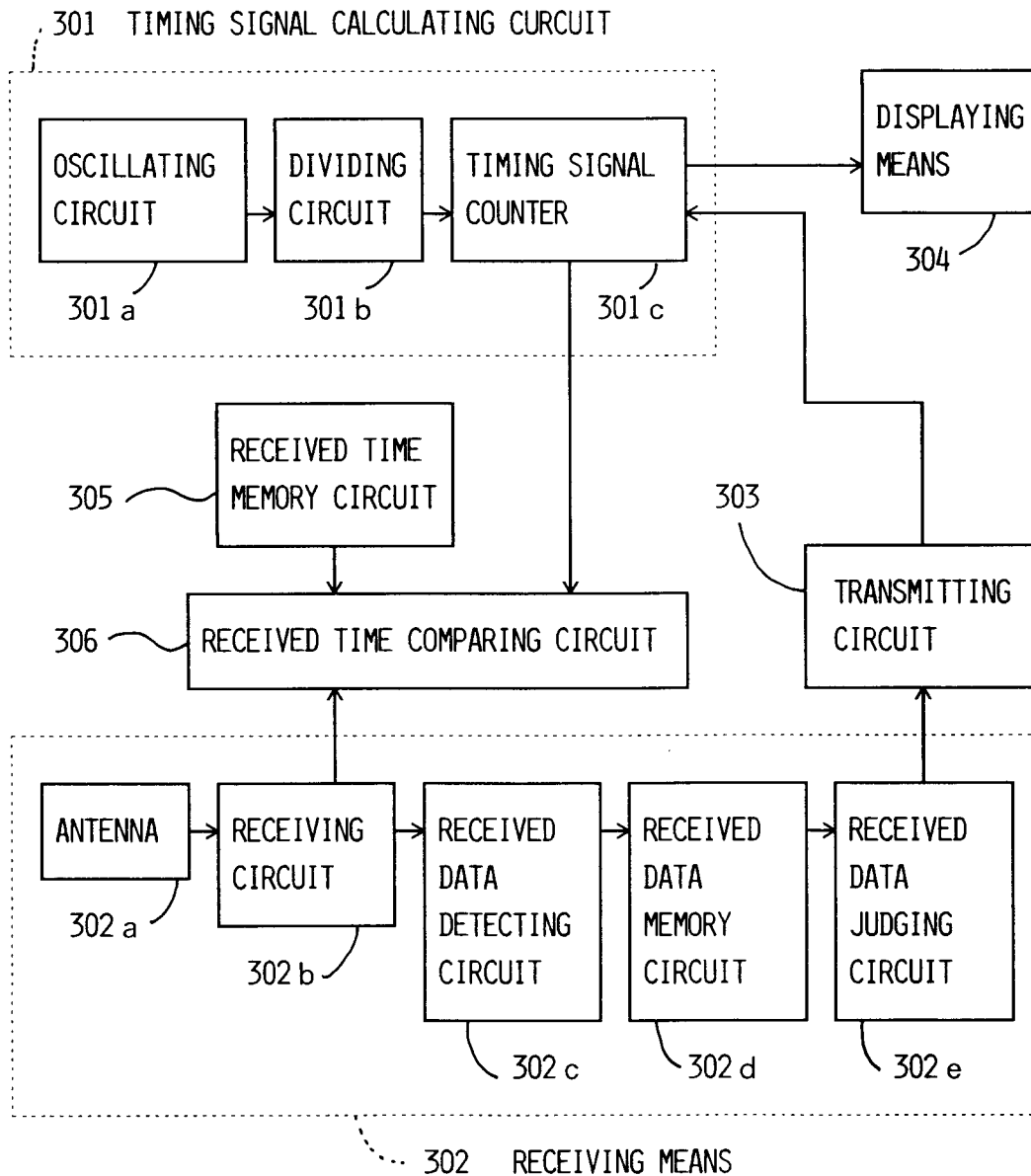


FIG. 4

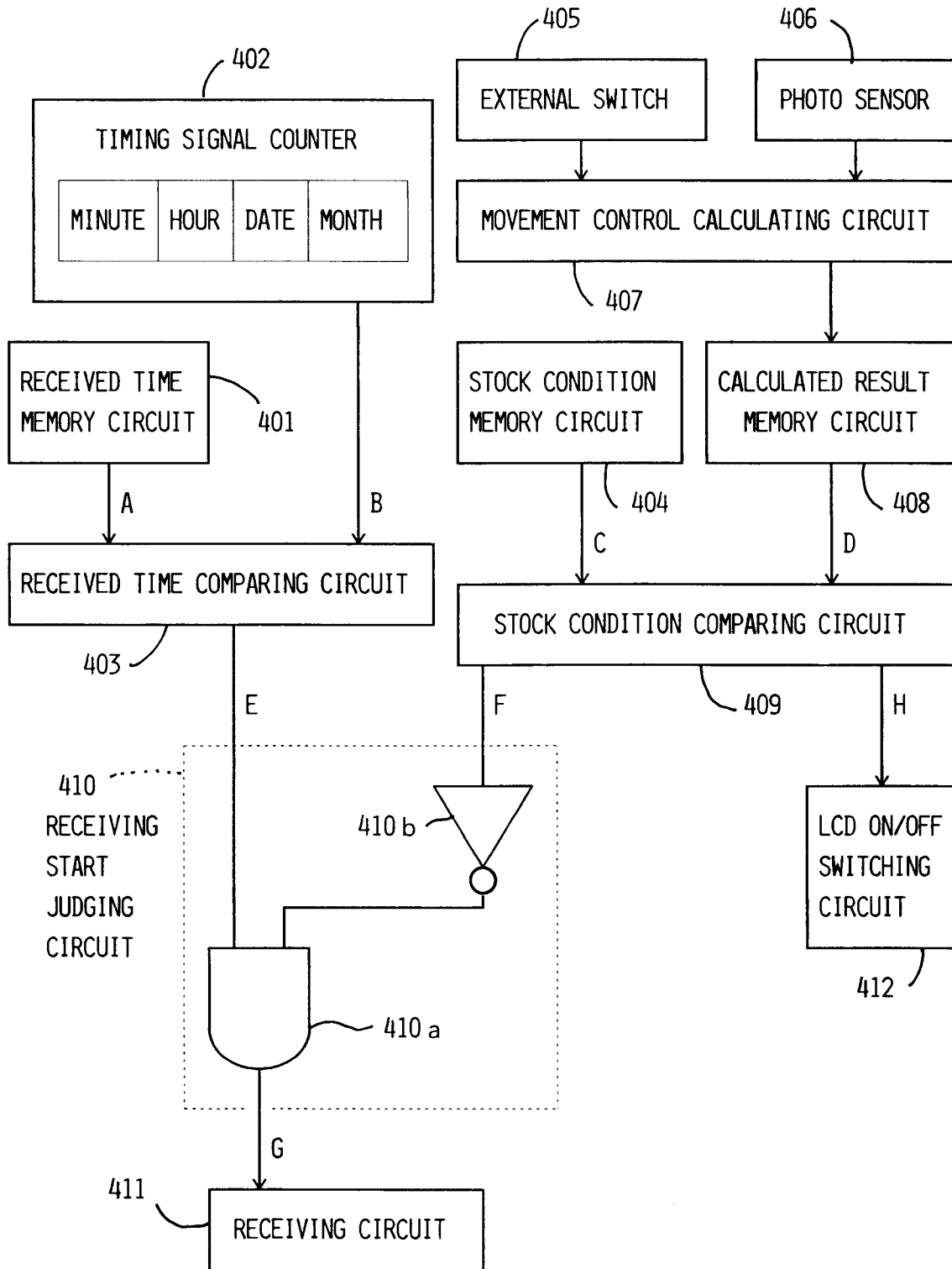


FIG. 5

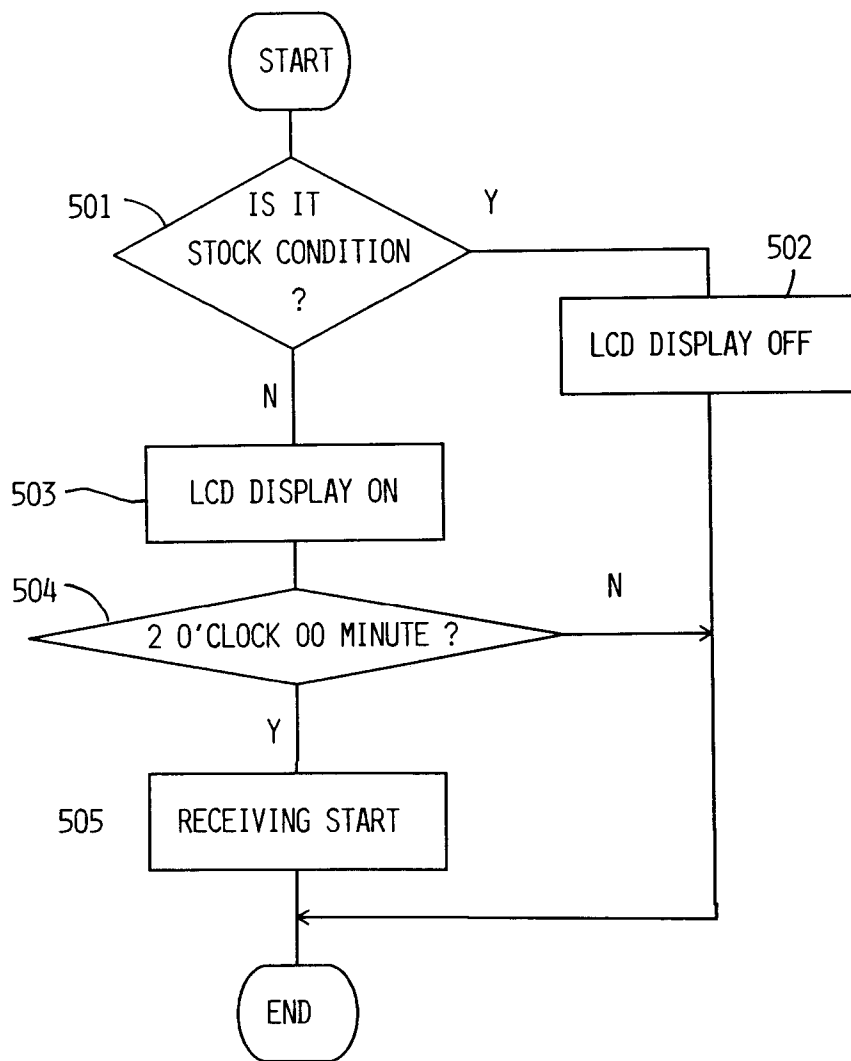


FIG. 6

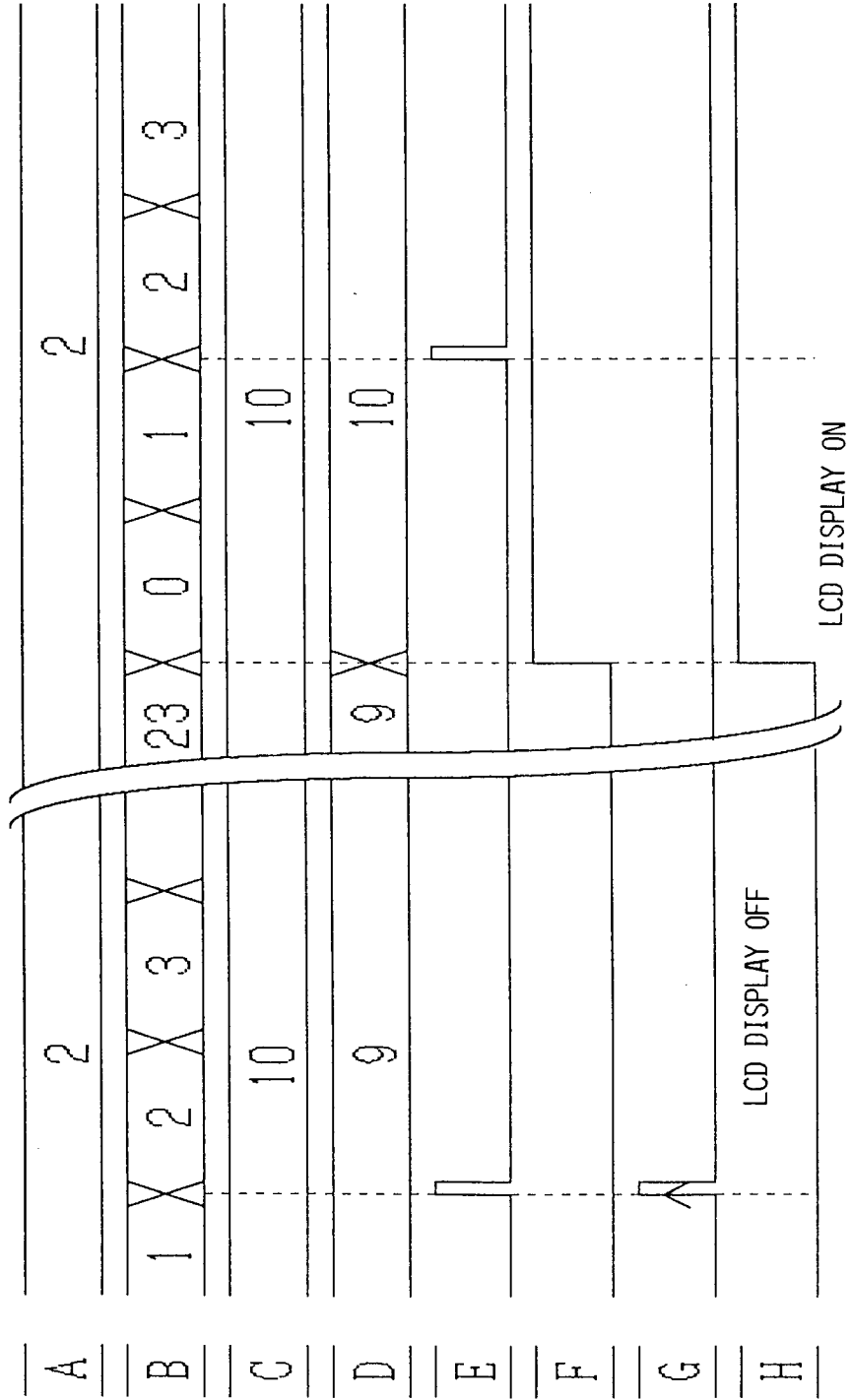


FIG. 7

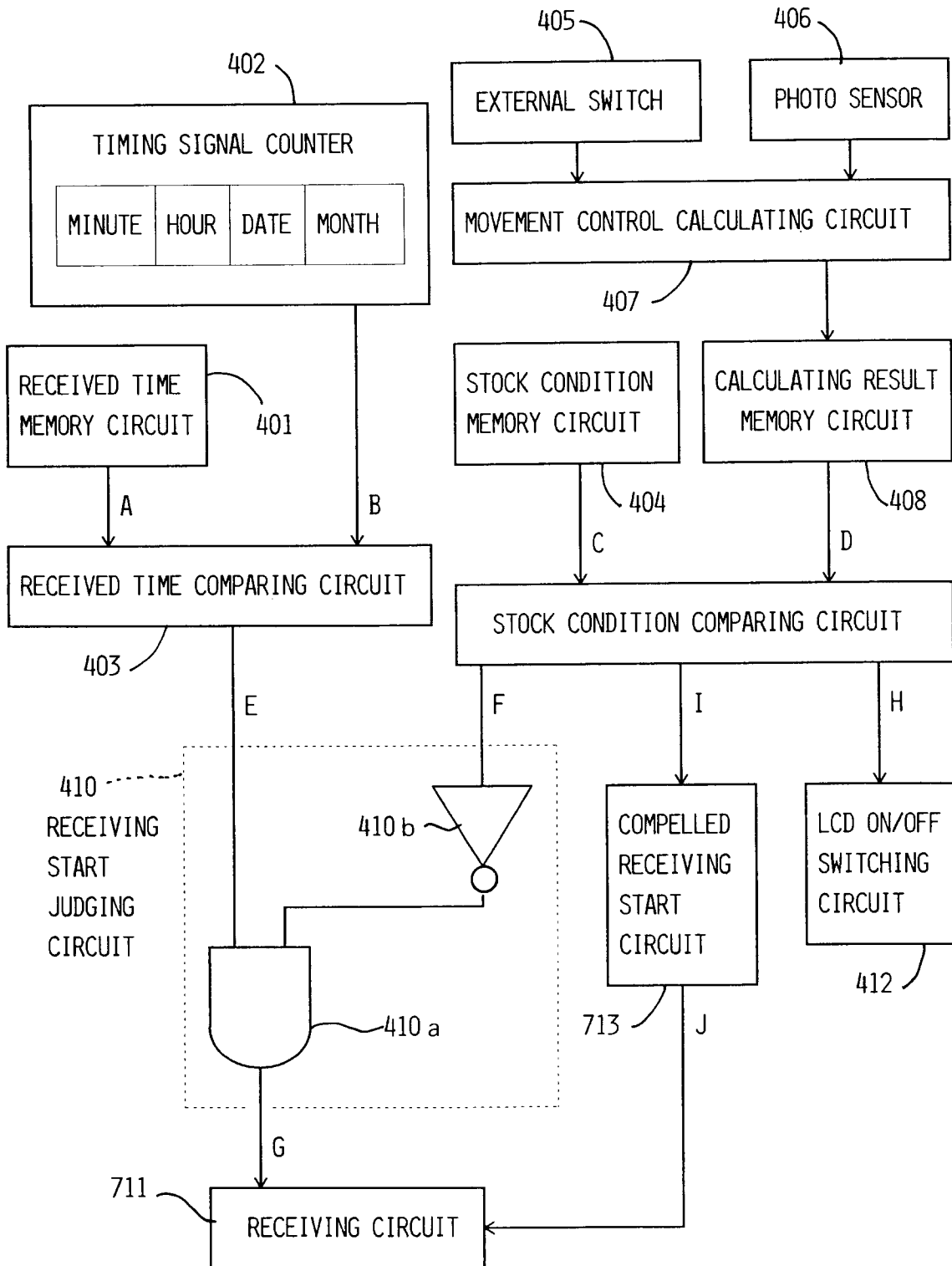


FIG. 8

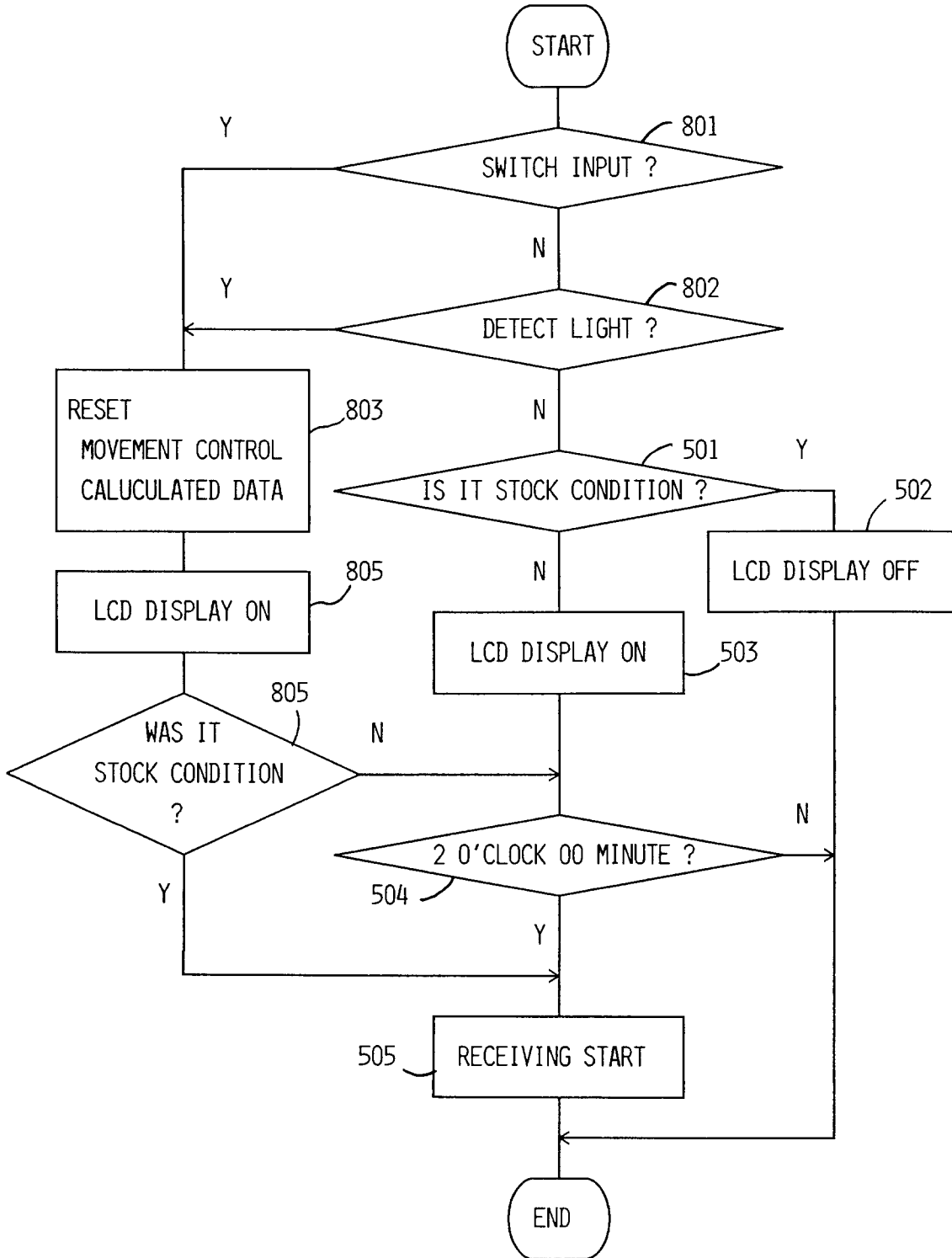
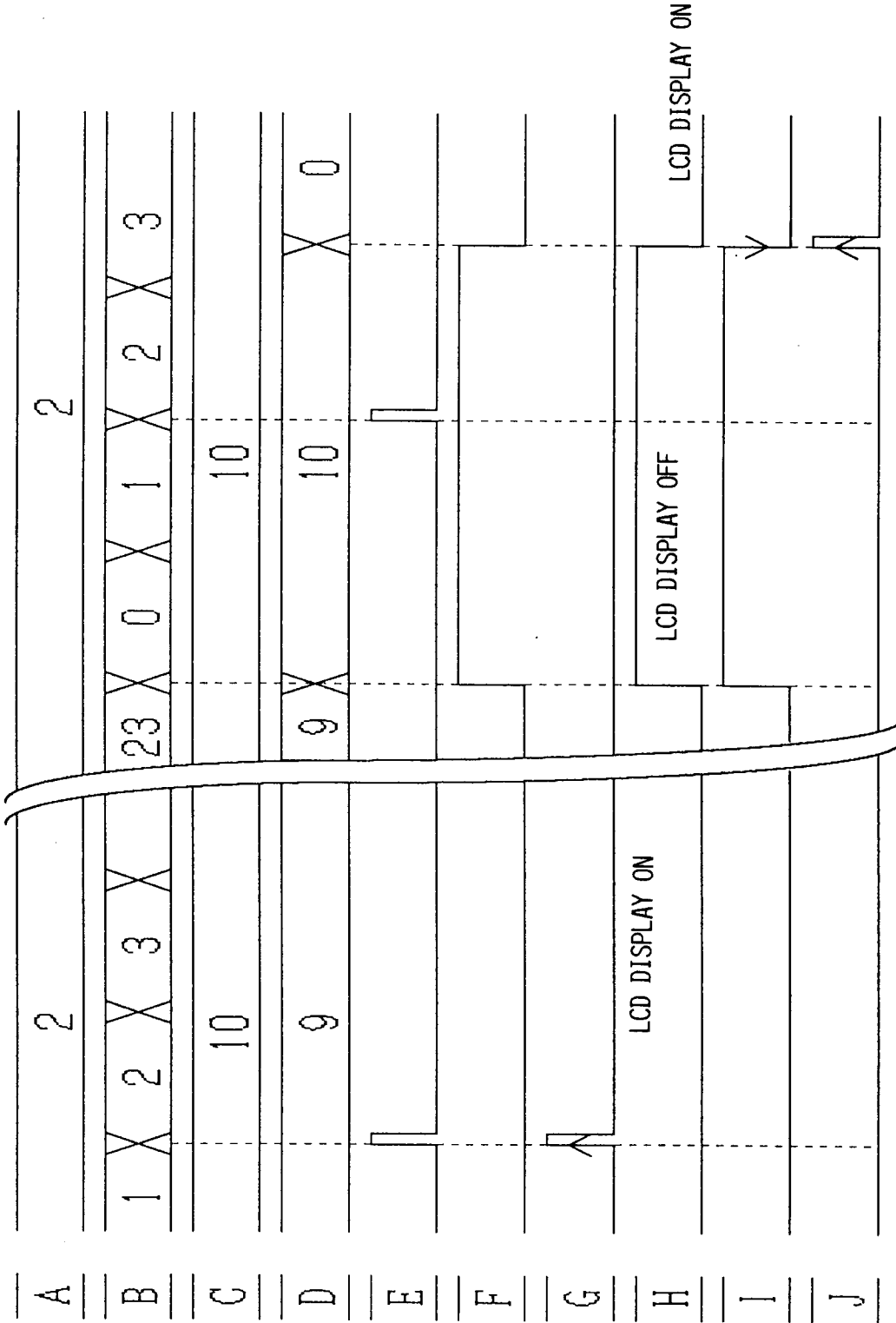


FIG. 9





DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	EP-A-0 439 725 (JUNGHANS UHREN GMBH) * column 2, line 26 - column 4, line 40; figure 1 * ---	1-5	G04G1/00 G04G5/00
A	EP-A-0 221 363 (ETA SA FABRIQUES D'EBAUCHES) * column 1, line 1 - column 2, line 31 * ---	1-5	
A	DE-A-27 30 330 (EBAUCHES ELECTRONIQUES S. A.) * page 6, paragraph 2 * -----	1-5	
			TECHNICAL FIELDS SEARCHED (Int.Cl.6)
			G04G
The present search report has been drawn up for all claims			
Place of search		Date of completion of the search	Examiner
THE HAGUE		14 March 1995	Exelmans, U
CATEGORY OF CITED DOCUMENTS			
X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document	