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(54) Active matrix display device with additional dummy datalines.

(57) The active matrix display device has a plurality of gate lines X provided on horizontal lines, a plurality of data lines Y provided on vertical lines, and a plurality of picture elements PXL provided at each intersection of both lines. The picture elements PXL provided horizontally and vertically constitute the display region 1. The vertical scanning circuit 2 scans vertically each gate line X sequentially, and selects picture elements on a respective one horizontal line every one horizontal period. The horizontal scanning circuit 3 scans each data line Y sequentially in one horizontal period, samples image signal Vsig, and writes by dot sequential scanning the image signal Vsig on picture elements PXL of a respective selected horizontal line. The data lines are defined in two sections, real data lines Y1, Y2, ...,YL provided in the display region 1, and dummy data lines YD1, YD2, YD3, and YD4 provided outside the display region, which dummy data lines intersect with the end section of the gate lines. The horizontal scanning circuit 3 scans horizontally the real data lines Y1, Y2,...,YL with a sampling timing overlapping a plurality of the real data lines, subsequently continues to scan the dummy data lines YD1, YD2, YD3 and YD4 with the overlapped sampling timing. Thereby, a band defect usually appearing on the side end of the screen when an active matrix display device is driven dot sequentially, is eliminated.

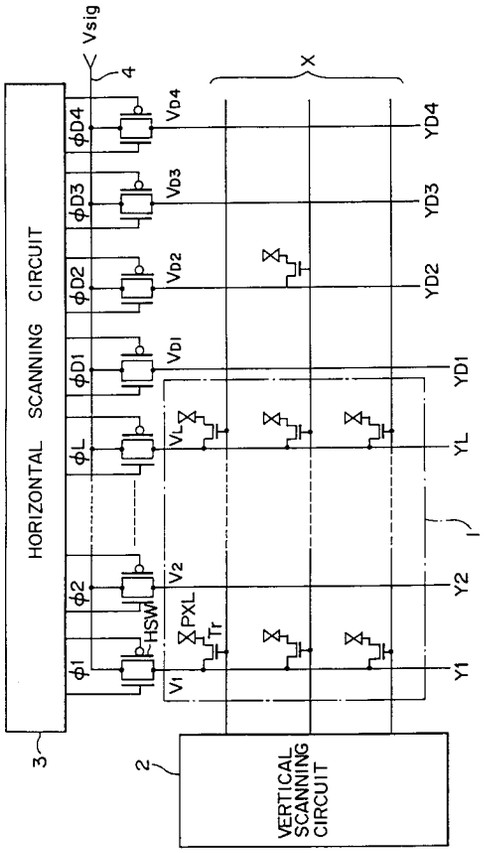

FIG. 1

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BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to an active matrix display device, more particularly to technology for eliminating band defect on the side ends of the screen of an active matrix display device driven by dot sequential scanning.

Description of Related Art

A typical schematic structure of a conventional active matrix display device is described briefly referring to Fig. 8. The active matrix display device has a plurality of gate lines X provided horizontally in parallel, a plurality of data lines Y provided vertically in parallel, and a plurality of picture elements PXL provided at each intersection of the gate and data lines. The picture element comprises, for example, a small liquid crystal cell, and the plurality of elements is provided so as to form a matrix which constitutes the display region. Thin film transistors Tr are integrated corresponding to each picture element PXL to drive the picture element. The display device is provided with a vertical scanning circuit 101 which vertically scans each gate line X sequentially and selects picture elements PXL on one horizontal line every one horizontal period. The device is provided also with a horizontal scanning circuit 102 which scans each data line Y sequentially in one horizontal period to sample image signal Vsig, and writes, by dot sequential scanning, the image signal Vsig on the picture elements on the selected one horizontal line. In detail, each data line Y is connected to the video line 103 through a respective horizontal switch HSW, and is supplied with the image signal Vsig from the outside. The horizontal scanning circuit 102 outputs sampling pulses ϕ_{H1}, ϕ_{H2}, ϕ_{H3},... ϕ_{HN} sequentially to make and break each horizontal switch HSW and sample image signal Vsig at each data line Y.

Fig. 9 shows waveforms of sampling pulses supplied sequentially from the horizontal scanning circuit 102 shown in Fig. 8. Sampling pulse duration τ_H is determined corresponding to the sampling period assigned to each data line Y. As active matrix display devices have been refined, the number of picture elements has been increased to cause shortening of writing time per one dot. For an active matrix display device for HDTV, writing time per one dot is shortened due to speed-up of line scanning. Correspondingly, sampling pulse duration τ_H is inevitably extremely shortened. For example, in the case of a half-line active matrix display device with 470 horizontal picture elements for NTSC, sampling pulse duration is of the order of τ_H = 50 μs/470/3(RGB) = 320 ns. In the case of 800 horizontal picture elements, τ_H = 188 ns. Furthermore, for a doubled driving speed of a full line system, the sampling pulse duration τ_H is shortened to 94 ns. Shortening of sampling pulse duration causes difficulty in wave shaping which results in use of a complex horizontal scanning circuit structure of the horizontal circuit and narrowed design options. Insufficient writing time causes a limitation on selectable design options of the liquid crystal panel.

For example, a method disclosed in Japanese Patent Publication No. 1989-37911 has been proposed to solve the shortening problem of sampling pulse duration τ_H. In this technique, the pulse durations of sampling pulses ϕ_{H1}, ϕ_{H2}, ϕ_{H3}, ϕ_{H4} ... are made longer and overlapped sampling pulses are output sequentially as illustrated in Fig. 10. This technique is a method in which a plurality of data lines are being selected simultaneously and the selected lines are being shifted sequentially. For example, in the case that four data lines are selected simultaneously as shown in Fig. 10, sampling pulse duration for 800 horizontal picture elements is of the order of τ_H = 4 x 188 ns = 750 ns. By applying this technique, the design limitation on the driving of the horizontal scanning circuit and also the design limitation on the liquid crystal panel are reduced.

However, this method, in which a plurality of data lines are selected simultaneously and the group of selected data lines is shifted sequentially, disadvantageously involves a band defect at the side of the display region 104 corresponding to the end of the horizontal scanning direction - see the screen shown in Fig. 11. For example, when the display is in normal white mode, the band defect 105 appears as a band darker than a normal region. The band defect 105 is attributed to the release of the sampling pulses from overlapping, at the side end of horizontal scanning, and to a driving condition different from that of a normal region.

OBJECTS AND SUMMARY OF THE INVENTION

It is the object of the present invention to eliminate the band defect on the side end of horizontal scanning in the dot sequential driving of an active matrix display device. The band defect is a disadvantage of the above-mentioned technique. To attain the object, a technique described hereinafter has been created. An active matrix display device of the invention has three basic components of a plurality of gate lines provided horizontally in parallel, a plurality of data lines provided vertically in parallel, and a plurality of picture elements provided at each intersection of both lines, which picture elements constitute the display region. In addition, the display device is provided with a vertical scanning circuit and horizontal scanning circuit as peripheral components. The vertical scanning circuit scans vertically each gate line sequentially to select picture elements on at least one horizontal line every respective horizontal period. On

the other hand, the horizontal scanning circuit scans each data line sequentially to sample image signals in one horizontal period, and writes by dot sequential scanning the image signals on picture elements of the respective selected horizontal line(s). The data lines of the present invention are defined characteristically into two sections, that is real data lines provided in the display region and additional dummy data lines provided outside the display region, which dummy lines intersect with the end sections of gate lines. The horizontal scanning circuit scans horizontally the real data lines with a sampling timing so that a plurality of pulses overlap, and subsequently the horizontal scanning circuit scans additionally the dummy data lines with the sampling timing in the same manner as scanned on the real data lines. In this case, it is required to provide at least as many dummy data lines as there are simultaneously-scanned lines in the horizontal scanning with the certain overlapped sampling timing.

According to the present invention, dummy data lines are provided additionally outside the display region adjacent to the ends of real data lines provided in the display region. The horizontal scanning circuit scans horizontally real data lines and then dummy data lines continuously. At the side of the display region, the overlapped sampling timing on a plurality of real data lines is maintained, therefore image display is normal at the side and no band defect is displayed. When the horizontal scanning reaches the dummy data lines, overlapped sampling timing is released and the quality of displaying could change depending on the case. However, this does not cause a problem because dummy data lines are provided outside the display region, and a band defect will not appear on the display.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a circuit diagram for illustrating the structure of an active matrix display device in accordance with the present invention.

Fig. 2 is a timing chart for description of the operation of the active matrix display device shown in Fig. 1.

Fig. 3 is a reference circuit diagram for description of the band defect in a conventional active matrix display device.

Fig. 4 is a timing chart for explaining effects occurring in the circuit of Fig. 3.

Fig. 5 is a reference equivalent circuit diagram to aid understanding of capacitive coupling effects in the Fig. 3 circuit.

Fig. 6 is a reference timing chart for explaining the operation of the Fig. 3 circuit.

Fig. 7 is a reference graph illustrating the occurrence of a band defect.

Fig. 8 is a circuit diagram for illustrating a typical structure of a conventional active matrix display device.

Fig. 9 is a timing chart for description of the operation of the active matrix display device shown in Fig. 8.

Fig. 10 is a timing chart for description of operation of a prior art active matrix display device.

Fig. 11 is a schematic diagram for illustrating a band defect on the display region.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

A preferred embodiment of the invention will be described in detail referring to the drawings. Fig. 1 is a circuit diagram for illustration of the preferred embodiment of an active matrix display device of the invention. As shown in the figure, the active matrix display device has a plurality of gate lines X provided horizontally in parallel and a plurality of data lines Y provided vertically in parallel. Picture elements PXL are provided at intersections of both lines to form a matrix, and the picture elements constitute the display region 1. The picture elements PXL comprise liquid crystal cells with fine structure. In this embodiment, thin film transistors Tr are provided to drive picture elements PXL comprising liquid crystal cells. Source electrodes of the thin film transistors Tr are connected individually to corresponding data lines Y, gate electrodes are connected to corresponding gate lines X, and drain electrodes are connected to corresponding picture elements PXL.

A vertical scanning circuit 2 and a horizontal scanning circuit 3 are provided around the display region 1. The vertical scanning circuit 2 scans vertically each gate line Y sequentially to make thin film transistors conductive, and picture elements PXL on a respective one horizontal line are selected every one horizontal period. On the other hand, the horizontal scanning circuit 3 scans each data line Y sequentially in one horizontal period to sample the image signal Vsig and writes, by dot sequential scanning, the image signal Vsig on picture elements PXL on the respective selected one horizontal line. In detail, each data line Y is connected to the video line 4 through a respective horizontal switch HSW and thereby receives the supply of image signal Vsig. The horizontal scanning circuit 3 outputs sampling pulses ϕ and inverted pulses sequentially to make and break controllably the horizontal switches HSW and thereby the above-mentioned image signal Vsig is sampled. Image signal Vsig sampled at each data line Y is written on picture elements PXL on one horizontal line through thin film transistors Tr which are ON. Afterwards, the thin film transistors Tr are switched OFF, and the written image signals Vsig are retained until next frame.

It is a feature of this invention that data lines are

defined in two sections, real data lines Y1, Y2, ..., YL provided in the display region 1 and dummy data lines YD1, YD2, YD3, and YD4 provided outside the display region 1. These dummy lines intersect with the end sections of gate lines X. In this embodiment, picture elements PXL and thin film transistors Tr are removed from the dummy data lines. The present invention is not limited to this embodiment, dummy picture elements and thin film transistors may be assigned to the dummy data lines for complete unification of the driving condition. On the other hand, the horizontal scanning circuit 3 scans not only the real data lines but also the dummy data lines. The horizontal scanning circuit 3 horizontally scans the real data lines Y1, Y2,...,YL with a sampling timing overlapping a plurality of data lines (in this embodiment, four lines). Subsequently, the horizontal scanning circuit 3 horizontally scans additionally the dummy data lines YD1, YD2, YD3, and YD4 with the same overlapped sampling timing as used in scanning the real data lines. In this case, it is required to provide at least so many dummy data lines as correspond to the simultaneously-scanned lines in the horizontal scanning. In this embodiment at least four dummy data lines are provided. The dummy data lines are described in detail hereinunder. The horizontal scanning circuit 3 outputs sampling pulses ϕ1, ϕ2, ... ϕL and inverted pulses sequentially to horizontal switches HSW connected to the real data lines Y1, Y2, ...,YL. Subsequently, the horizontal scanning circuit 3 outputs sampling pulses ϕD1, ϕD2, ϕD3, ϕD4 and inverted pulses sequentially to horizontal switches HSW connected to the dummy data lines YD1, YD2, YD3, and YD4. In this embodiment, inverted pulses are output because transmission gates comprising CMOS are used as the horizontal switches HSW.

Operation of the active matrix display device illustrated in Fig. 1 is described in detail referring of Fig. 2. As shown in the timing chart of Fig. 2, sampling pulses are output on the real data lines with a sampling timing overlapping four lines to scan horizontally the display region 1 (real scanning). For easy understanding of the timing chart, five real sampling pulses from the first pulse to the final pulse ϕL are shown. In this embodiment, the rising of a sampling pulse ϕL is followed by successive output of dummy sampling pulses ϕD1, ϕD2, ϕD3, ϕD4 with the same overlapped sampling timing on dummy data lines to scan horizontally outside the display region (dummy scanning). Output of successive sampling pulses ϕ with overlapped timing as described hereinabove generates voltage swinging of gate lines X due to capacitive coupling at intersections of gate lines X and data lines Y. For each rising edge of a sampling pulse ϕ, a corresponding disturbance is produced in the gate line voltage by capacitive coupling. Consequently, the voltage of the gate lines X continues to swing until the rising edge of the final dummy sampling pulse ϕD4. After the rising edge of the final dummy sampling pulse ϕD4, the voltage of the gate lines X decays gradually towards ground level because the gate lines are no longer subject to disturbance by capacitive coupling.

On the other hand, at the rising edge of each sampling pulse ϕ, horizontal switches HSW are changed from ON to OFF. Closed HSW causes jumping of the voltage swinging of gate lines to each signal line Y. As a result, when the voltage of the gate lines starts to decay after cessation of swinging, this decay affects the voltage of signal lines Y, through capacitive coupling, to cause decay thereof. As understood from the timing chart in Fig. 2, voltages of real data lines V_{L-4}, V_{L-3}, V_{L-3}, V_{L-1}, and V_L start to decay all at once after swinging of gate lines ceases, because the corresponding switches HSW are already off, and the decay finally causes voltage drop of ΔV_0. The voltage drop ΔV_0 is identical for all the real data lines, consequently no dark band appears on the display. On the other hand, for example for the first dummy data line YD1, after cessation of voltage swinging, the falling edge of the corresponding dummy sampling pulse ϕD1 occurs one clock period later. Because voltage VD1 starts to decay synchronously with the falling edge of pulse ϕD1, final voltage drop ΔV_1 is smaller than ΔV_0. Similarly, for the second dummy data line YD2, because VD2 starts to decay with a delay of one more clock period, the final voltage drop ΔV_2 is smaller than ΔV_1. As mentioned above, the voltage drops of the dummy data lines are different from each other, and the difference results in fluctuated display brightness. However, the dummy data lines are provided outside the display region 1, therefore the fluctuation does not affect an actual image on the display.

As described above, the horizontal scanning circuit 3 scans horizontally an extra four picture elements in addition to the effective display region 1. Four dummy data lines including HSW are provided on the area outside the display region 1 in the same arrangement as provided in the display region 1. By providing the four dummy data lines, swinging of gate lines continues similarly across the border between the effective display region 1 and the outside area covering four picture elements. Consequently, swinging of signal lines included in the display region 1 is limited to the side end, and does not change rapidly. In this embodiment, four signal lines are horizontally scanned simultaneously, and generally in the case of simultaneous scanning on n signal lines, at least n dummy data lines are required. Picture elements and transistors for driving them are not necessarily required in the dummy lines, and the degree of elimination of the band effect is sufficient without such picture elements and driving transistors.

Finally, the mechanism of band defect generation is described for better understanding, referring to Fig. 3 to Fig. 7. Fig. 3 shows the structure of a typical ac-

tive matrix display device, and is the same device as shown in Fig. 8 (on the corresponding components, corresponding reference numerals are indicated for easy understanding). Reference symbols which are used for the first time in the following description are explained below. The voltage of video line 103 supplied with image signal Vsig is represented by VA. Voltage of individual data lines Y is represented by VB. Voltage of each gate line X is represented by VC. Parasitic capacitance Ch interposes at the intersections of each gate line X and data line Y, and the parasitic capacitance Ch causes the above-mentioned capacitive coupling. A resistance component is included in each gate line X.

Fig. 4 illustrates how voltage VA, VB, and VC of each line change with time. As illustrated, a sampling pulse ϕ_H is output from the horizontal scanning circuit 102, and image signal Vsig is sample-held on the corresponding data line. The voltage VB of a sample-held data line and the voltage VC of the gate line are apparently flat, but the enlarging of the scale representing VB and VC, around the sampling timing, reveals fluctuation due to the above-mentioned capacitive coupling. Signals of differential waveform are superposed continuously on the gate voltage VC. Data voltage VB decays from the sample-hold level.

Fig. 5 shows a circuit equivalent with this part. Individual data lines intersect with all gate lines behind the corresponding HSW. Therefore, the equivalent circuit includes a capacitive C_H equivalent to the total parasitic capacitance shown in Fig. 3. C_G in the equivalent circuit represents the total capacitance of the gate lines themselves, and R_G represents the equivalent gate line resistance. In this circuit, when data voltage VB rises, gate voltage VC also rises correspondingly. When HSW is closed, decay of the gate voltage VC is reflected on the data voltage VB analogously.

Corresponding behavior during simultaneous four line scanning is illustrated referring to the timing chart in Fig. 6. For easy description, five sampling pulses from the final sampling pulse $\phi_{H,LAST}$ to $\phi_{H,LAST-4}$ are shown. Charging and discharging of signal lines are repeated until the final sampling pulse $\phi_{H,LAST}$ rises. Due to the repeated charge and discharge, gate voltage VC is sequentially disturbed, via capacitive coupling, at each ϕ_H rise. After the rise of $\phi_{H,LAST}$, the gate voltage VC decays toward the ground level because the gate voltage VC no longer receives disturbance via capacitive coupling. On the other hand, after closing of the corresponding HSW, swinging of the gate voltage produces an effect in each signal line through the capacitive component C_H of the equivalent circuit illustrated in Fig. 5.

For the signal lines horizontally scanned before the timing of $\phi_{H,LAST-4}$, the voltage level of the signal lines changes by ΔV_0 as shown on the VB_{LAST-4}. The level of disturbance of signal line voltage decreases step by step as one passes from the signal line scanned by $\phi_{H,Last-3}$, to the signal lines scanned by $\phi_{H,LST-2}$, and $\phi_{H,LST-1}$, ..., due to gate voltage VC decay. Voltage drop ΔV_1, ... ΔV_4 for the final four signal line voltages VB_{LAST-3}, ..., VB_{LAST} decreases in the order from LAST-3 to LAST.

The ΔV is illustrated schematically in Fig. 7. ΔV of the final four signal lines is smaller than that of all previous signal lines. The decrement increases as the signal line approaches the final signal line. Accordingly, a band defect in the final four lines results.

As described hereinbefore, according to the present invention, dummy data lines are provided outside the display region in addition to real data lines provided in the display region. The real data lines are scanned horizontally with a sampling timing overlapping on a plurality of data lines, and then additionally the dummy data lines are scanned horizontally with the same sampling timing as scanned on the real data lines, thereby the band defect is eliminated and image quality is improved. Especially, this invention is effective for large size active matrix display devices which utilize increased numbers of picture elements with dot sequence driving.

Although the present invention has been described with reference to "horizontal" gate lines, "vertical" signal lines and a left-to-right "horizontal scanning direction" these directions merely correspond to the directions in a conventionally-scanned image (scanning left-to-right line-by-line, starting at the top of the image). It is to be understood that the present invention includes the case where the specific preferred embodiment is modified to take into account a non-standard scanned image signal (e.g. one in which the horizontal scanning is right-to-left, or the image is scanned top-to-bottom, column-by-column, starting at the left).

Claims

1. An active matrix display device comprising :

a plurality of gate lines (X) provided on horizontal lines,

a plurality of data lines (Y) provided vertically,

a plurality of picture elements (PXL) provided at each intersection of said gate lines and data lines which constitute the display region (1),

a vertical scanning circuit (2) for scanning vertically each gate line sequentially to select picture elements for each horizontal line, and

a horizontal scanning circuit (3) to sample image signals and subsequently write the image signals on picture elements on a selected horizontal line by dot sequential scanning, wherein

said data lines are defined in two sections, real data lines (Y) provided in said display region,

and dummy data lines (YD) provided outside said display region, which dummy data lines intersect with the end section of the gate lines,and

said horizontal scanning circuit (3) is adapted to operate a first scanning horizontally on said real data lines with a sampling timing overlapping a plurality of real data lines, and, subsequently to said first scanning, to operate a second scanning horizontally on said dummy data lines with the overlapped sampling timing.

2. An active matrix display device as claimed in claim 1, wherein at least as many dummy data lines are provided as there are simultaneously-scanned lines in the horizontal scanning with the overlapped sampling timing.

3. An active matrix display device as claimed in claim 1, wherein dummy picture elements corresponding to said dummy data lines are provided.

4. An active matrix display device as claimed in claim 1, wherein picture elements are provided on only said data lines.

FIG. 1

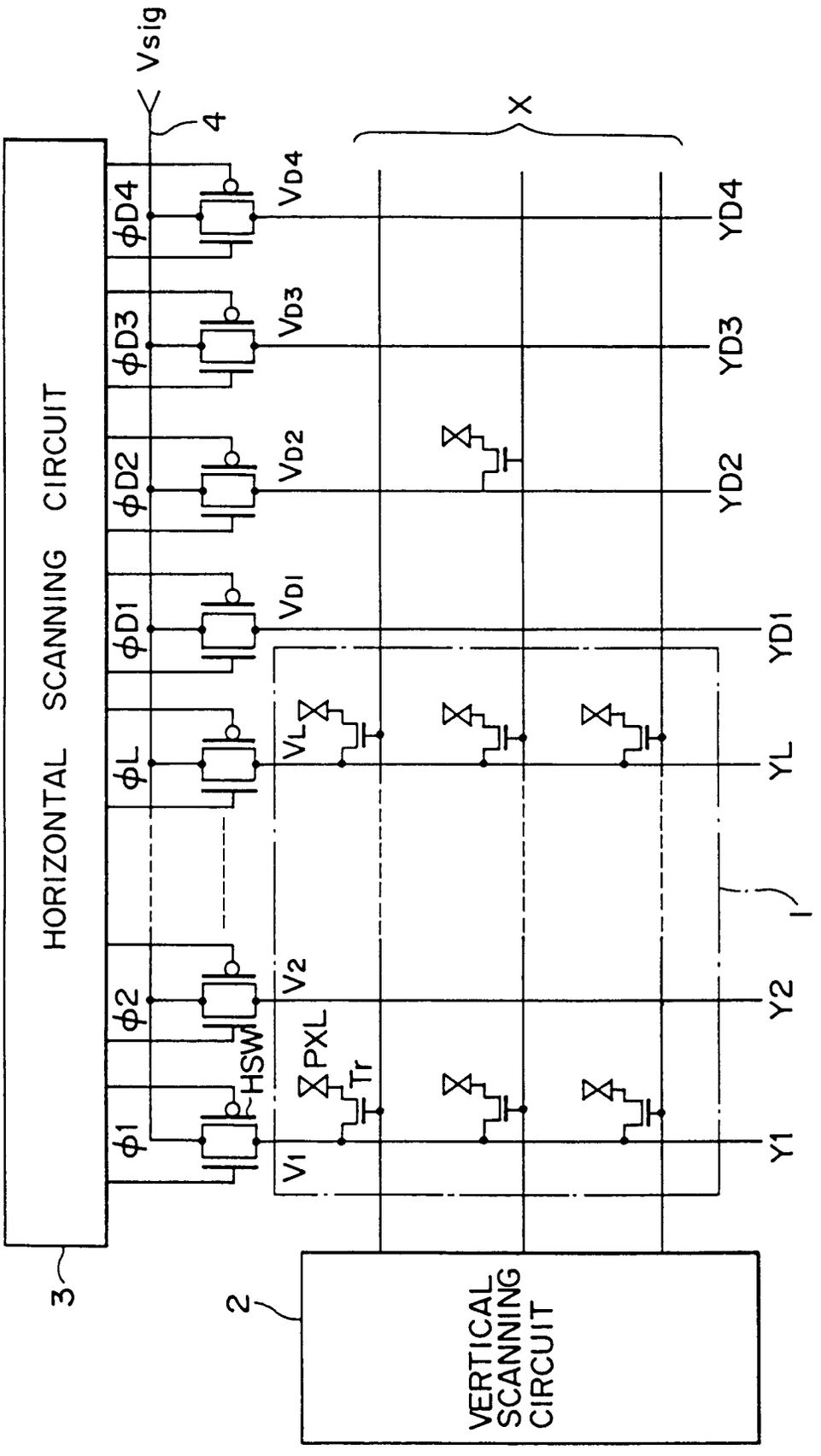

HORIZONTAL SCANNING CIRCUIT
3
Vsig
4
X
φD4
φD3
φD2
φD1
φL
φ2
φ1
HSW
VD4
VD3
VD2
VD1
VL
V2
V1
PXL
Tr
YD4
YD3
YD2
YD1
YL
Y2
Y1
1
2
VERTICAL SCANNING CIRCUIT

FIG. 2

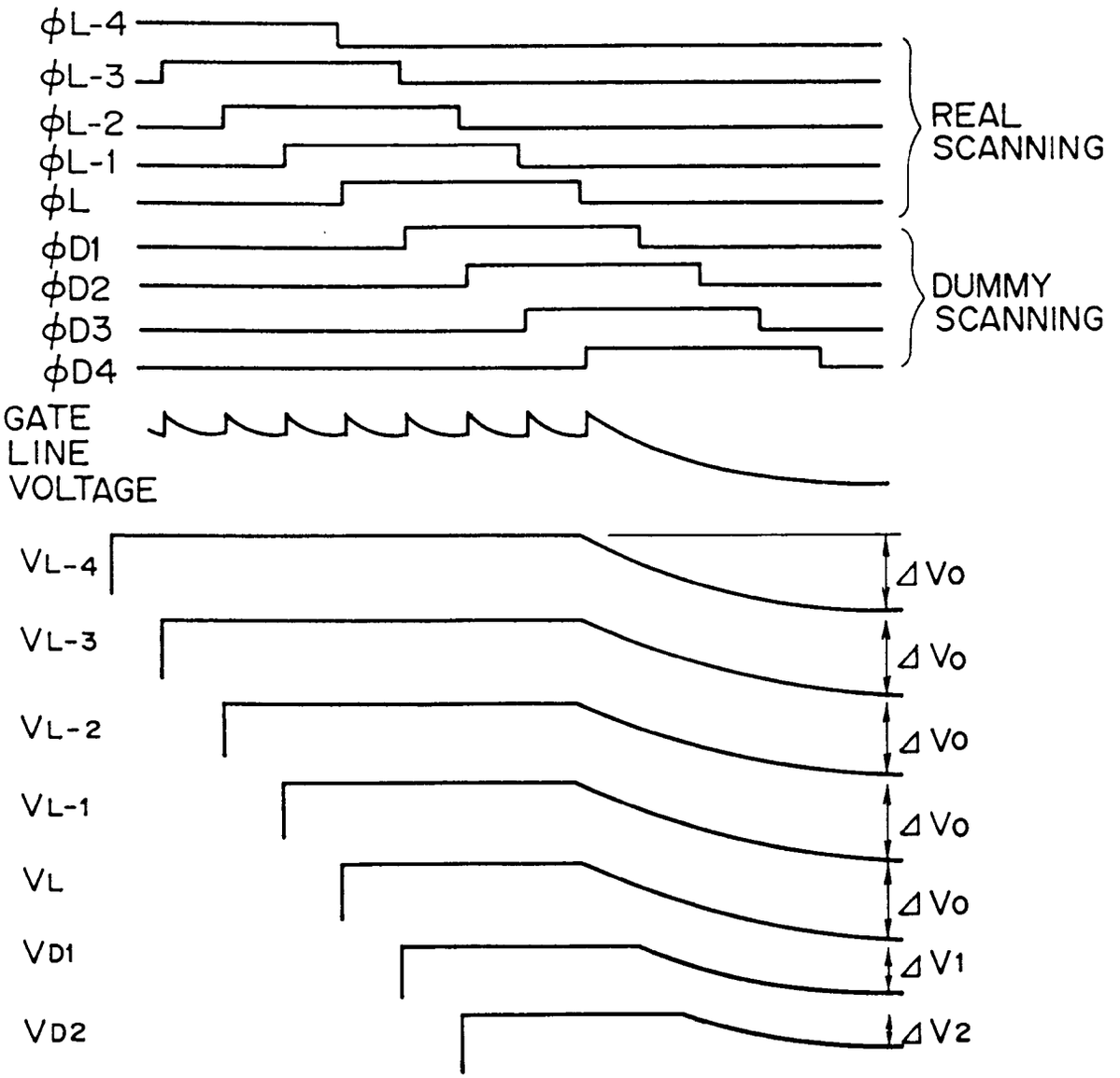

φL-4
φL-3
φL-2
φL-1
φL
REAL SCANNING
φD1
φD2
φD3
φD4
DUMMY SCANNING
GATE LINE VOLTAGE
VL-4
VL-3
VL-2
VL-1
VL
VD1
VD2
ΔVo
ΔVo
ΔVo
ΔVo
ΔVo
ΔV1
ΔV2

FIG. 3

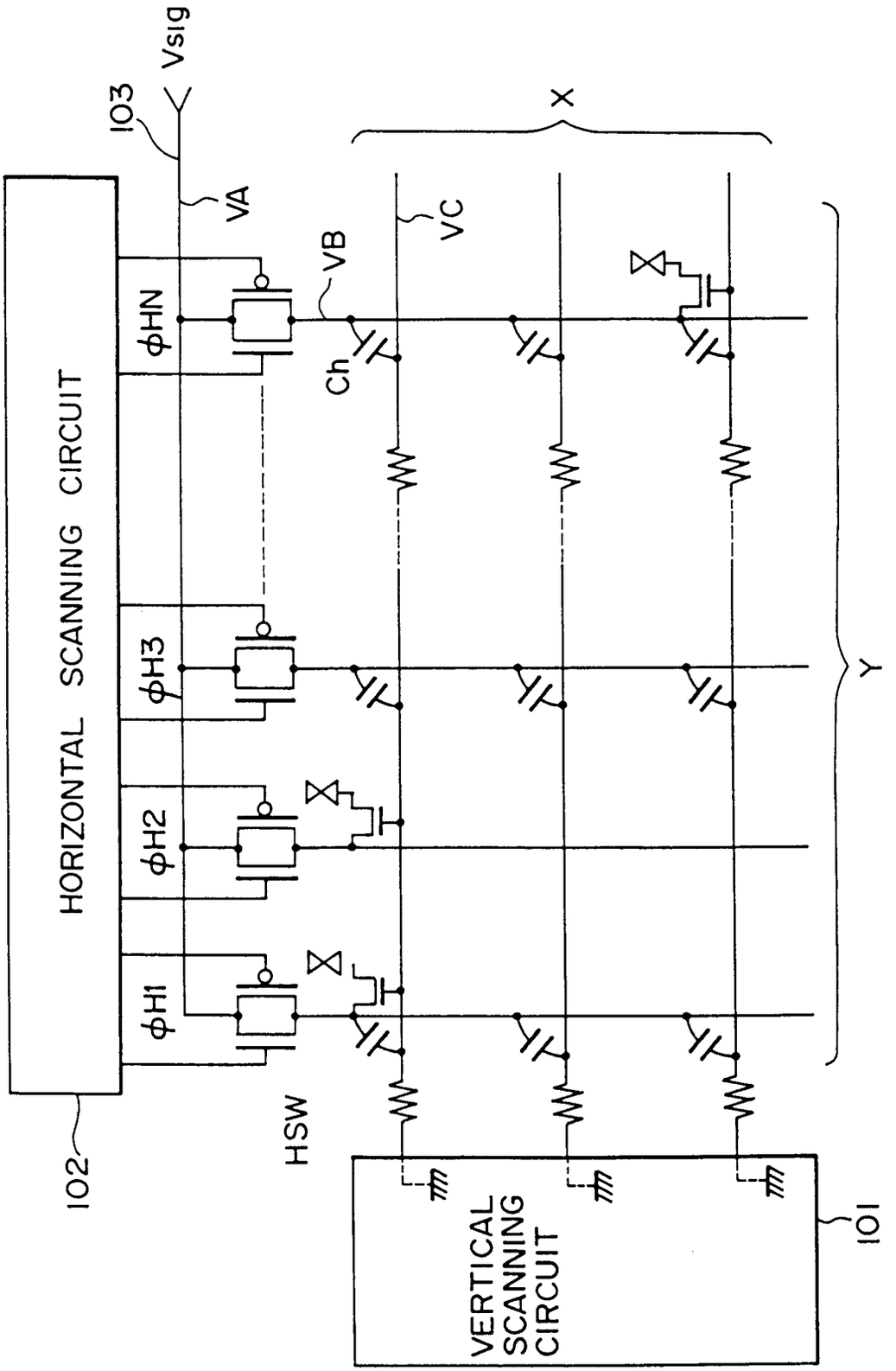

HORIZONTAL SCANNING CIRCUIT
VERTICAL SCANNING CIRCUIT
Vsig
103
VA
VB
VC
Ch
HSW
ϕHN
ϕH3
ϕH2
ϕH1
X
Y
101
102

FIG. 4

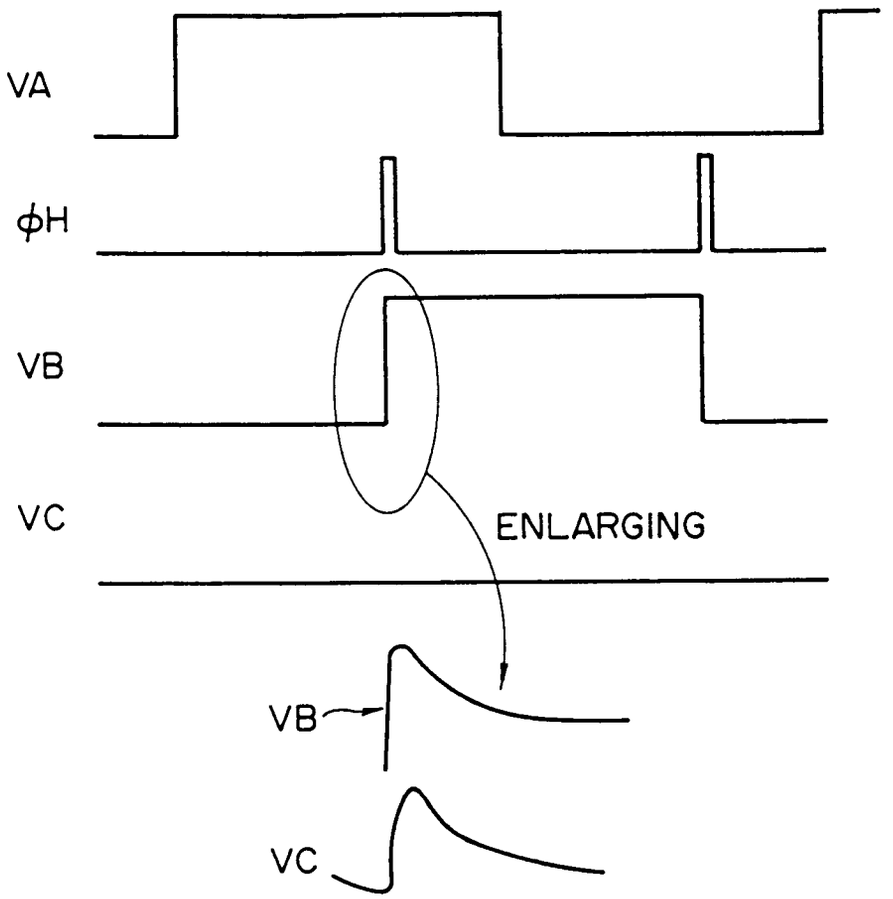


FIG. 5

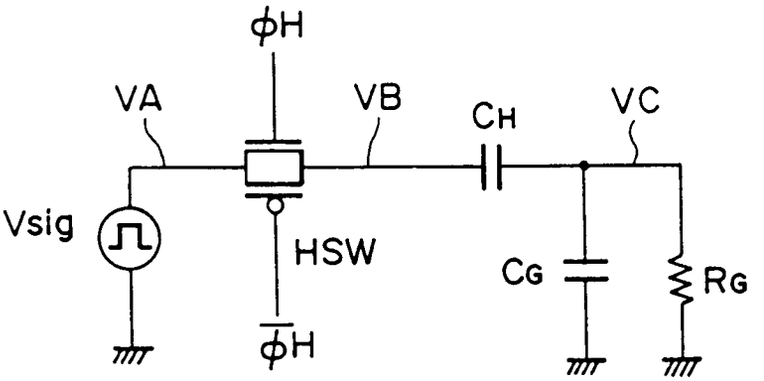


FIG. 6

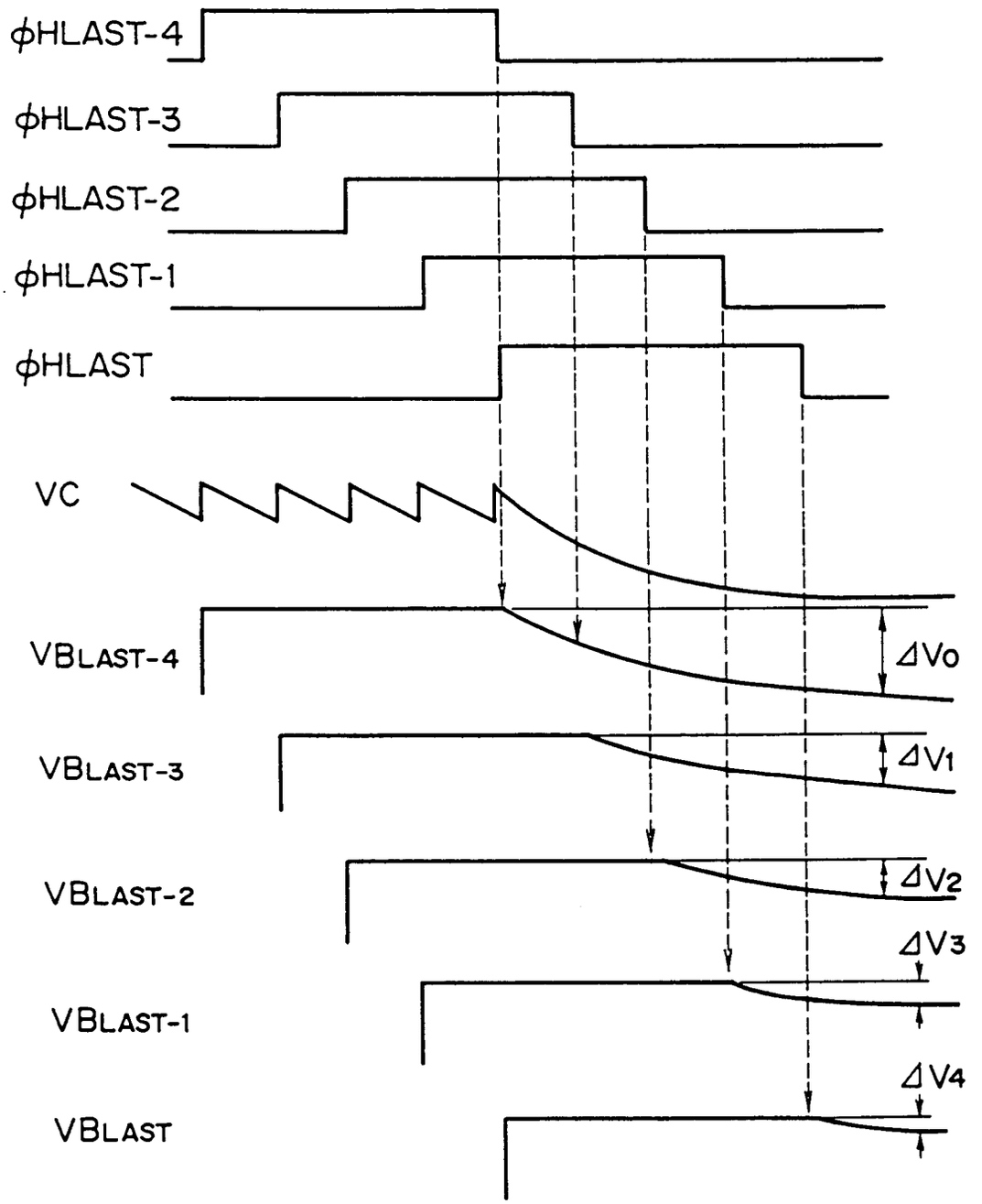

φHLAST-4
φHLAST-3
φHLAST-2
φHLAST-1
φHLAST
VC
VBLAST-4
VBLAST-3
VBLAST-2
VBLAST-1
VBLAST
ΔV0
ΔV1
ΔV2
ΔV3
ΔV4

FIG. 7

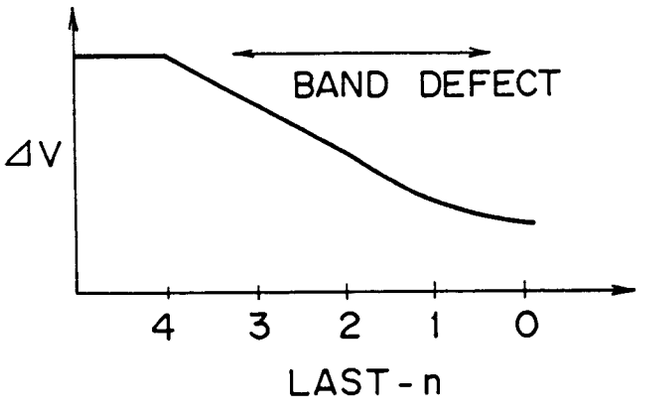

BAND DEFECT
ΔV
4
3
2
1
0
LAST - n

FIG. 8

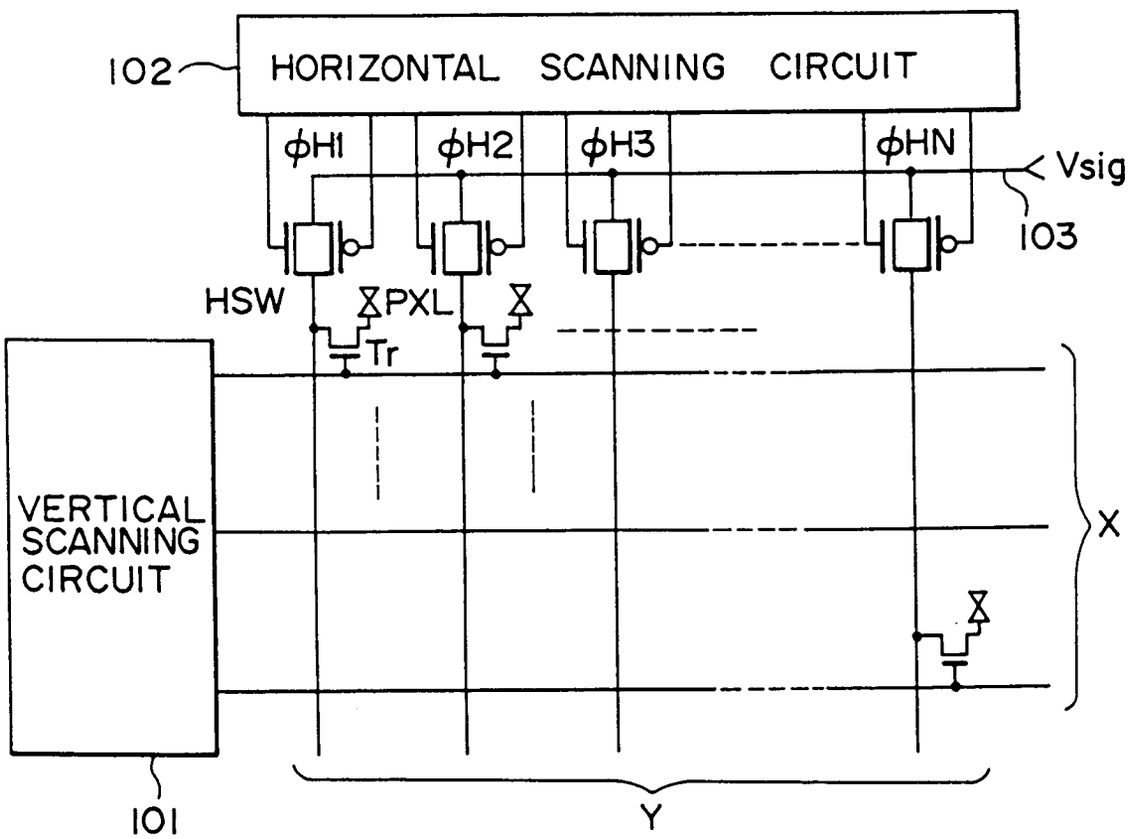

102
HORIZONTAL SCANNING CIRCUIT
φH1
φH2
φH3
φHN
Vsig
103
HSW
PXL
Tr
VERTICAL SCANNING CIRCUIT
X
101
Y

FIG. 9

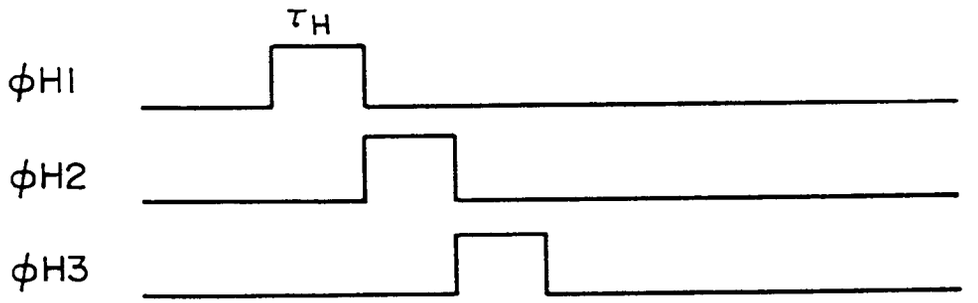


FIG. 10

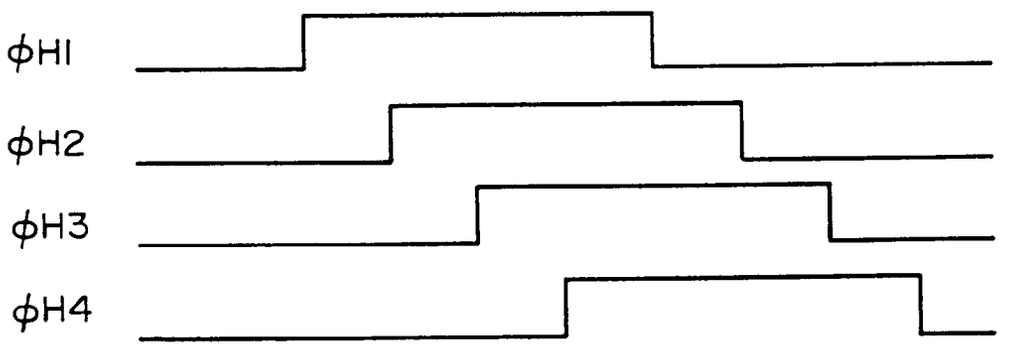
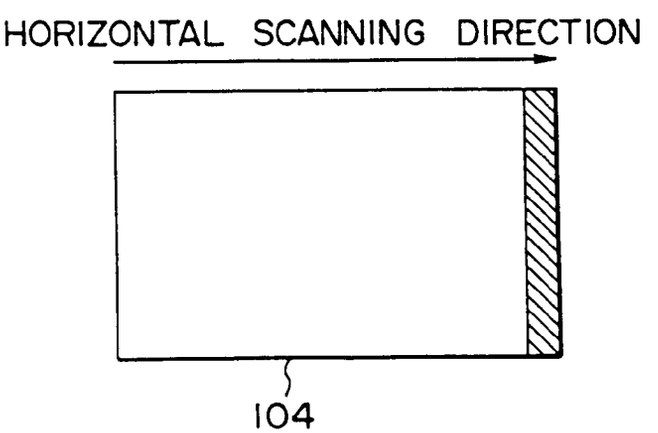


FIG. 11



European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 95 40 0895

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	PATENT ABSTRACTS OF JAPAN vol. 4 no. 71 (E-012) ,24 May 1980 & JP-A-55 041037 (SEIKO EPSON CO.) 22 March 1980, * abstract * ---	1,2	G09G3/36 G09G3/30
A	US-A-4 724 433 (INOUE ET AL.) * Abstract * * column 2, line 47 - column 3, line 30; figures 3A-5 * -----	1,2	
			TECHNICAL FIELDS SEARCHED (Int.Cl.6) G09G

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	3 August 1995	Corsi, F

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

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E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)