

(19)



Europäisches Patentamt
European Patent Office
Office européen des brevets



(11)

EP 0 678 850 B1

(12)

EUROPEAN PATENT SPECIFICATION

(45) Date of publication and mention
of the grant of the patent:
21.06.2000 Bulletin 2000/25

(51) Int Cl.7: **G09G 3/36**, G09G 3/30

(21) Application number: **95400895.9**

(22) Date of filing: **21.04.1995**

(54) **Active matrix display device with additional dummy datalines**

Anzeigeeinrichtung mit aktiver Matrix mit zusätzlichen Dummy-Datenleitungen

Appareil d'affichage à matrice active avec lignes de données factices additionnelles

(84) Designated Contracting States:
DE FR GB

(30) Priority: **22.04.1994 JP 10760294**

(43) Date of publication of application:
25.10.1995 Bulletin 1995/43

(73) Proprietor: **SONY CORPORATION**
Tokyo 141 (JP)

(72) Inventor: **Maekawa, Toshikazu**
Shinagawa-ku, Tokyo (JP)

(74) Representative: **Thévenet, Jean-Bruno et al**
Cabinet Beau de Loménie
158, rue de l'Université
75340 Paris Cédex 07 (FR)

(56) References cited:
US-A- 4 724 433

- **PATENT ABSTRACTS OF JAPAN vol. 4 no. 71**
(E-012) ,24 May 1980 & JP-A-55 041037 (SEIKO
EPSON CO.) 22 March 1980,

Note: Within nine months from the publication of the mention of the grant of the European patent, any person may give notice to the European Patent Office of opposition to the European patent granted. Notice of opposition shall be filed in a written reasoned statement. It shall not be deemed to have been filed until the opposition fee has been paid. (Art. 99(1) European Patent Convention).

EP 0 678 850 B1

Description

Field of the Invention

[0001] This invention relates to an active matrix display device, more particularly to technology for eliminating band defect on the side ends of the screen of an active matrix display device driven by dot sequential scanning.

Description of Related Art

[0002] A typical schematic structure of a conventional active matrix display device is described briefly referring to Fig. 8. The active matrix display device has a plurality of gate lines X provided horizontally in parallel, a plurality of data lines Y provided vertically in parallel, and a plurality of picture elements PXL provided at each intersection of the gate and data lines. The picture element comprises, for example, a small liquid crystal cell, and the plurality of elements is provided so as to form a matrix which constitutes the display region. Thin film transistors Tr are integrated corresponding to each picture element PXL to drive the picture element. The display device is provided with a vertical scanning circuit 101 which vertically scans each gate line X sequentially and selects picture elements PXL on one horizontal line every one horizontal period. The device is provided also with a horizontal scanning circuit 102 which scans each data line Y sequentially in one horizontal period to sample image signal Vs_{ig}, and writes, by dot sequential scanning, the image signal Vs_{ig} on the picture elements on the selected one horizontal line. In detail, each data line Y is connected to the video line 103 through a respective horizontal switch HSW, and is supplied with the image signal Vs_{ig} from the outside. The horizontal scanning circuit 102 outputs sampling pulses ϕ_{H1} , ϕ_{H2} , ϕ_{H3} , ..., ϕ_{HN} sequentially to make and break each horizontal switch HSW and sample image signal Vs_{ig} at each data line Y.

[0003] Fig. 9 shows waveforms of sampling pulses supplied sequentially from the horizontal scanning circuit 102 shown in Fig. 8. Sampling pulse duration τ_H is determined corresponding to the sampling period assigned to each data line Y. As active matrix display devices have been refined, the number of picture elements has been increased to cause shortening of writing time per one dot. For an active matrix display device for HDTV, writing time per one dot is shortened due to speed-up of line scanning. Correspondingly, sampling pulse duration τ_H is inevitably extremely shortened. For example, in the case of a half-line active matrix display device with 470 horizontal picture elements for NTSC, sampling pulse duration is of the order of $\tau_H = 50 \mu s / 470 / 3 (RGB) = 320 \text{ ns}$. In the case of 800 horizontal picture elements, $\tau_H = 188 \text{ ns}$. Furthermore, for a doubled driving speed of a full line system, the sampling pulse duration τ_H is shortened to 94 ns. Shortening of sam-

pling pulse duration causes difficulty in wave shaping which results in use of a complex horizontal scanning circuit structure of the horizontal circuit and narrowed design options. Insufficient writing time causes a limitation on selectable design options of the liquid crystal panel.

[0004] For example, a method disclosed in Japanese Patent Publication No. 1989-37911 has been proposed to solve the shortening problem of sampling pulse duration τ_H . In this technique, the pulse durations of sampling pulses ϕ_{H1} , ϕ_{H2} , ϕ_{H3} , ϕ_{H4} ... are made longer and overlapped sampling pulses are output sequentially as illustrated in Fig. 10. This technique is a method in which a plurality of data lines are being selected simultaneously and the selected lines are being shifted sequentially. For example, in the case that four data lines are selected simultaneously as shown in Fig. 10, sampling pulse duration for 800 horizontal picture elements is of the order of $\tau_H = 4 \times 188 \text{ ns} = 750 \text{ ns}$. By applying this technique, the design limitation on the driving of the horizontal scanning circuit and also the design limitation on the liquid crystal panel are reduced.

[0005] However, this method, in which a plurality of data lines are selected simultaneously and the group of selected data lines is shifted sequentially, disadvantageously involves a band defect at the side of the display region 104 corresponding to the end of the horizontal scanning direction - see the screen shown in Fig. 11. For example, when the display is in normal white mode, the band defect 105 appears as a band darker than a normal region. The band defect 105 is attributed to the release of the sampling pulses from overlapping, at the side end of horizontal scanning, and to a driving condition different from that of a normal region.

[0006] Document US A 4 724 433 further discloses a matrix type display panel comprising a display panel having a plurality of scanning lines, a plurality of data lines and a plurality of picture elements disposed at each intersection of the scanning lines and data lines, analog switching elements for sampling-and-holding information signals which are applied to the data lines in synchronisation with scanning signals applied to the scanning lines, and a horizontal scanning circuit adapted to operate a scanning horizontally on said data lines with a sampling timing of one data line overlapping the corresponding respective sampling timings of a plurality of data lines.

OBJECTS AND SUMMARY OF THE INVENTION

[0007] It is the object of the present invention to eliminate the band defect on the side end of horizontal scanning in the dot sequential driving of an active matrix display device. The band defect is a disadvantage of the above-mentioned technique. To attain the object, the invention provides an active matrix display device as defined in claim 1. The active matrix display device of the invention has three basic components of a plurality of

gate lines provided horizontally in parallel, a plurality of data lines provided vertically in parallel, and a plurality of picture elements provided at each intersection of both lines, which picture elements constitute the display region. In addition, the display device is provided with a vertical scanning circuit and horizontal scanning circuit as peripheral components. The vertical scanning circuit scans vertically each gate line sequentially to select picture elements on at least one horizontal line every respective horizontal period. On the other hand, the horizontal scanning circuit scans each data line sequentially to sample image signals in one horizontal period, and writes by dot sequential scanning the image signals on picture elements of the respective selected horizontal line(s). The data lines of the present invention are defined characteristically into two sections, that is real data lines provided in the display region and additional dummy data lines provided outside the display region, which dummy lines intersect with the end sections of gate lines. The horizontal scanning circuit scans horizontally the real data lines with a sampling timing so that a plurality of pulses overlap, and subsequently the horizontal scanning circuit scans additionally the dummy data lines with the sampling timing in the same manner as scanned on the real data lines. It is required to provide at least as many dummy data lines as there are simultaneously-scanned lines in the horizontal scanning with the certain overlapped sampling timing.

[0008] According to the present invention, dummy data lines are provided additionally outside the display region adjacent to the ends of real data lines provided in the display region. The horizontal scanning circuit scans horizontally real data lines and then dummy data lines continuously. At the side of the display region, the overlapped sampling timing on a plurality of real data lines is maintained, therefore image display is normal at the side and no band defect is displayed. When the horizontal scanning reaches the dummy data lines, overlapped sampling timing is released and the quality of displaying could change depending on the case. However, this does not cause a problem because dummy data lines are provided outside the display region, and a band defect will not appear on the display.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] Fig. 1 is a circuit diagram for illustrating the structure of an active matrix display device in accordance with the present invention.

[0010] Fig. 2 is a timing chart for description of the operation of the active matrix display device shown in Fig. 1.

[0011] Fig. 3 is a reference circuit diagram for description of the band defect in a conventional active matrix display device.

[0012] Fig. 4 is a timing chart for explaining effects occurring in the circuit of Fig. 3.

[0013] Fig. 5 is a reference equivalent circuit diagram

to aid understanding of capacitive coupling effects in the Fig. 3 circuit.

[0014] Fig. 6 is a reference timing chart for explaining the operation of the Fig. 3 circuit.

[0015] Fig. 7 is a reference graph illustrating the occurrence of a band defect.

[0016] Fig. 8 is a circuit diagram for illustrating a typical structure of a conventional active matrix display device.

[0017] Fig. 9 is a timing chart for description of the operation of the active matrix display device shown in Fig. 8.

[0018] Fig. 10 is a timing chart for description of operation of a prior art active matrix display device.

[0019] Fig. 11 is a schematic diagram for illustrating a band defect on the display region.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0020] A preferred embodiment of the invention will be described in detail referring to the drawings. Fig. 1 is a circuit diagram for illustration of the preferred embodiment of an active matrix display device of the invention. As shown in the figure, the active matrix display device has a plurality of gate lines X provided horizontally in parallel and a plurality of data lines Y provided vertically in parallel. Picture elements PXL are provided at intersections of both lines to form a matrix, and the picture elements constitute the display region 1. The picture elements PXL comprise liquid crystal cells with fine structure. In this embodiment, thin film transistors Tr are provided to drive picture elements PXL comprising liquid crystal cells. Source electrodes of the thin film transistors Tr are connected individually to corresponding data lines Y, gate electrodes are connected to corresponding gate lines X, and drain electrodes are connected to corresponding picture elements PXL.

[0021] A vertical scanning circuit 2 and a horizontal scanning circuit 3 are provided around the display region 1. The vertical scanning circuit 2 scans vertically each gate line Y sequentially to make thin film transistors conductive, and picture elements PXL on a respective one horizontal line are selected every one horizontal period. On the other hand, the horizontal scanning circuit 3 scans each data line Y sequentially in one horizontal period to sample the image signal Vsig and writes, by dot sequential scanning, the image signal Vsig on picture elements PXL on the respective selected one horizontal line. In detail, each data line Y is connected to the video line 4 through a respective horizontal switch HSW and thereby receives the supply of image signal Vsig. The horizontal scanning circuit 3 outputs sampling pulses ϕ and inverted pulses sequentially to make and break controllably the horizontal switches HSW and thereby the above-mentioned image signal Vsig is sampled. Image signal Vsig sampled at each data line Y is written on picture elements PXL on one hor-

horizontal line through thin film transistors T_r which are ON. Afterwards, the thin film transistors T_r are switched OFF, and the written image signals V_{sig} are retained until next frame.

[0022] It is a feature of this invention that data lines are defined in two sections, real data lines Y_1, Y_2, \dots, Y_L provided in the display region 1 and dummy data lines YD_1, YD_2, YD_3 , and YD_4 provided outside the display region 1. These dummy lines intersect with the end sections of gate lines X . In this embodiment, picture elements PXL and thin film transistors T_r are removed from the dummy data lines. The present invention is not limited to this embodiment, dummy picture elements and thin film transistors may be assigned to the dummy data lines for complete unification of the driving condition. On the other hand, the horizontal scanning circuit 3 scans not only the real data lines but also the dummy data lines. The horizontal scanning circuit 3 horizontally scans the real data lines Y_1, Y_2, \dots, Y_L with a sampling timing overlapping a plurality of data lines (in this embodiment, four lines). Subsequently, the horizontal scanning circuit 3 horizontally scans additionally the dummy data lines YD_1, YD_2, YD_3 , and YD_4 with the same overlapped sampling timing as used in scanning the real data lines. In this case, it is required to provide at least so many dummy data lines as correspond to the simultaneously-scanned lines in the horizontal scanning. In this embodiment at least four dummy data lines are provided. The dummy data lines are described in detail hereinafter. The horizontal scanning circuit 3 outputs sampling pulses $\phi_1, \phi_2, \dots, \phi_L$ and inverted pulses sequentially to horizontal switches HSW connected to the real data lines Y_1, Y_2, \dots, Y_L . Subsequently, the horizontal scanning circuit 3 outputs sampling pulses $\phi D_1, \phi D_2, \phi D_3, \phi D_4$ and inverted pulses sequentially to horizontal switches HSW connected to the dummy data lines YD_1, YD_2, YD_3 , and YD_4 . In this embodiment, inverted pulses are output because transmission gates comprising CMOS are used as the horizontal switches HSW .

[0023] Operation of the active matrix display device illustrated in Fig. 1 is described in detail referring to Fig. 2. As shown in the timing chart of Fig. 2, sampling pulses are output on the real data lines with a sampling timing overlapping four lines to scan horizontally the display region 1 (real scanning). For easy understanding of the timing chart, five real sampling pulses from the first pulse to the final pulse ϕ_L are shown. In this embodiment, the rising of a sampling pulse ϕ_L is followed by successive output of dummy sampling pulses $\phi D_1, \phi D_2, \phi D_3, \phi D_4$ with the same overlapped sampling timing on dummy data lines to scan horizontally outside the display region (dummy scanning). Output of successive sampling pulses ϕ with overlapped timing as described hereinabove generates voltage swinging of gate lines X due to capacitive coupling at intersections of gate lines X and data lines Y . For each rising edge of a sampling pulse ϕ , a corresponding disturbance is produced in the

gate line voltage by capacitive coupling. Consequently, the voltage of the gate lines X continues to swing until the rising edge of the final dummy sampling pulse ϕD_4 . After the rising edge of the final dummy sampling pulse ϕD_4 , the voltage of the gate lines X decays gradually towards ground level because the gate lines are no longer subject to disturbance by capacitive coupling.

[0024] On the other hand, at the rising edge of each sampling pulse ϕ , horizontal switches HSW are changed from ON to OFF. Closed HSW causes jumping of the voltage swinging of gate lines to each signal line Y . As a result, when the voltage of the gate lines starts to decay after cessation of swinging, this decay affects the voltage of signal lines Y , through capacitive coupling, to cause decay thereof. As understood from the timing chart in Fig. 2, voltages of real data lines $V_{L-4}, V_{L-3}, V_{L-2}, V_{L-1}$, and V_L start to decay all at once after swinging of gate lines ceases, because the corresponding switches HSW are already off, and the decay finally causes voltage drop of ΔV_0 . The voltage drop ΔV_0 is identical for all the real data lines, consequently no dark band appears on the display. On the other hand, for example for the first dummy data line YD_1 , after cessation of voltage swinging, the falling edge of the corresponding dummy sampling pulse ϕD_1 occurs one clock period later. Because voltage VD_1 starts to decay synchronously with the falling edge of pulse ϕD_1 , final voltage drop ΔV_1 is smaller than ΔV_0 . Similarly, for the second dummy data line YD_2 , because VD_2 starts to decay with a delay of one more clock period, the final voltage drop ΔV_2 is smaller than ΔV_1 . As mentioned above, the voltage drops of the dummy data lines are different from each other, and the difference results in fluctuated display brightness. However, the dummy data lines are provided outside the display region 1, therefore the fluctuation does not affect an actual image on the display.

[0025] As described above, the horizontal scanning circuit 3 scans horizontally an extra four picture elements in addition to the effective display region 1. Four dummy data lines including HSW are provided on the area outside the display region 1 in the same arrangement as provided in the display region 1. By providing the four dummy data lines, swinging of gate lines continues similarly across the border between the effective display region 1 and the outside area covering four picture elements. Consequently, swinging of signal lines included in the display region 1 is limited to the side end, and does not change rapidly. In this embodiment, four signal lines are horizontally scanned simultaneously, and generally in the case of simultaneous scanning on n signal lines, at least n dummy data lines are required. Picture elements and transistors for driving them are not necessarily required in the dummy lines, and the degree of elimination of the band effect is sufficient without such picture elements and driving transistors.

[0026] Finally, the mechanism of band defect generation is described for better understanding, referring to Fig. 3 to Fig. 7. Fig. 3 shows the structure of a typical

active matrix display device, and is the same device as shown in Fig. 8 (on the corresponding components, corresponding reference numerals are indicated for easy understanding). Reference symbols which are used for the first time in the following description are explained below. The voltage of video line 103 supplied with image signal Vsig is represented by VA. Voltage of individual data lines Y is represented by VB. Voltage of each gate line X is represented by VC. Parasitic capacitance Ch interposes at the intersections of each gate line X and data line Y, and the parasitic capacitance Ch causes the above-mentioned capacitive coupling. A resistance component is included in each gate line X.

[0027] Fig. 4 illustrates how voltage VA, VB, and VC of each line change with time. As illustrated, a sampling pulse ϕ_H is output from the horizontal scanning circuit 102, and image signal Vsig is sample-held on the corresponding data line. The voltage VB of a sample-held data line and the voltage VC of the gate line are apparently flat, but the enlarging of the scale representing VB and VC, around the sampling timing, reveals fluctuation due to the above-mentioned capacitive coupling. Signals of differential waveform are superposed continuously on the gate voltage VC. Data voltage VB decays from the sample-hold level.

[0028] Fig. 5 shows a circuit equivalent with this part. Individual data lines intersect with all gate lines behind the corresponding HSW. Therefore, the equivalent circuit includes a capacitive C_H equivalent to the total parasitic capacitance shown in Fig. 3. C_G in the equivalent circuit represents the total capacitance of the gate lines themselves, and R_G represents the equivalent gate line resistance. In this circuit, when data voltage VB rises, gate voltage VC also rises correspondingly. When HSW is closed, decay of the gate voltage VC is reflected on the data voltage VB analogously.

[0029] Corresponding behavior during simultaneous four line scanning is illustrated referring to the timing chart in Fig. 6. For easy description, five sampling pulses from the final sampling pulse $\phi_{H, \text{LAST}}$ to $\phi_{H, \text{LAST}-4}$ are shown. Charging and discharging of signal lines are repeated until the final sampling pulse $\phi_{H, \text{LAST}}$ rises. Due to the repeated charge and discharge, gate voltage VC is sequentially disturbed, via capacitive coupling, at each ϕ_H rise. After the rise of $\phi_{H, \text{LAST}}$, the gate voltage VC decays toward the ground level because the gate voltage VC no longer receives disturbance via capacitive coupling. On the other hand, after closing of the corresponding HSW, swinging of the gate voltage produces an effect in each signal line through the capacitive component C_H of the equivalent circuit illustrated in Fig. 5.

[0030] For the signal lines horizontally scanned before the timing of $\phi_{H, \text{LAST}-4}$, the voltage level of the signal lines changes by ΔV_0 as shown on the $\text{VB}_{\text{LAST}-4}$. The level of disturbance of signal line voltage decreases step by step as one passes from the signal line scanned by $\phi_{H, \text{LAST}-3}$, to the signal lines scanned by $\phi_{H, \text{LAST}-2}$, and $\phi_{H, \text{LAST}-1}$, ..., due to gate voltage VC decay. Voltage drop

$\Delta V_1, \dots, \Delta V_4$ for the final four signal line voltages $\text{VB}_{\text{LAST}-3}, \dots, \text{VB}_{\text{LAST}}$ decreases in the order from LAST-3 to LAST.

[0031] The ΔV is illustrated schematically in Fig. 7. ΔV of the final four signal lines is smaller than that of all previous signal lines. The decrement increases as the signal line approaches the final signal line. Accordingly, a band defect in the final four lines results.

[0032] As described hereinbefore, according to the present invention, dummy data lines are provided outside the display region in addition to real data lines provided in the display region. The real data lines are scanned horizontally with a sampling timing overlapping on a plurality of data lines, and then additionally the dummy data lines are scanned horizontally with the same sampling timing as scanned on the real data lines, thereby the band defect is eliminated and image quality is improved. Especially, this invention is effective for large size active matrix display devices which utilize increased numbers of picture elements with dot sequence driving.

[0033] Although the present invention has been described with reference to "horizontal" gate lines, "vertical" signal lines and a left-to-right "horizontal scanning direction" these directions merely correspond to the directions in a conventionally-scanned image (scanning left-to-right line-by-line, starting at the top of the image). It is to be understood that the present invention includes the case where the specific preferred embodiment is modified to take into account a non-standard scanned image signal (e.g. one in which the horizontal scanning is right-to-left, or the image is scanned top-to-bottom, column-by-column, starting at the left).

Claims

1. An active matrix display device comprising :

- a plurality of gate lines (X) provided on horizontal lines,
- a plurality of data lines (Y) provided vertically,
- a plurality of picture elements (PXL) provided at each intersection of said gate lines and data lines which constitute the display region (1),
- a vertical scanning circuit (2) for scanning vertically each gate line sequentially to select picture elements for each horizontal line, and
- a horizontal scanning circuit (3) to sample image signals and subsequently write the image signals on picture elements on a selected horizontal line by dot sequential scanning, characterised in that
- said data lines are defined in two sections, real data lines (Y) provided in said display region, and dummy data lines (YD) provided outside said display region, said dummy data lines intersecting with the end section of the gate lines

in accordance with the direction of scanning of the horizontal scanning circuit, said horizontal scanning circuit (3) is adapted to operate a first scanning horizontally on each said real data line, with a sampling timing of one 5
real data line overlapping the respective sampling timings of a plurality of real data lines, and, subsequent to each said first scanning, to operate a second scanning horizontally on said dummy data lines with the same overlapped 10
sampling timing as used in scanning the real data lines, and
at least as many dummy data lines are provided as there are simultaneously-scanned lines in the horizontal scanning resulting from the overlapping of the plurality of sampling timings. 15

2. An active matrix display device as claimed in claim 1, wherein dummy picture elements corresponding to said dummy data lines are provided. 20
3. An active matrix display device as claimed in claim 1, wherein picture elements are provided on only said data lines. 25

Patentansprüche

1. Aktivmatrix-Anzeigeeinrichtung, die umfasst:

eine Vielzahl von Gateleitungen (X), die in horizontalen Zeilen vorgesehen sind,
eine Vielzahl von Datenleitungen (Y), die vertikal angeordnet vorgesehen sind,
eine Vielzahl von Bildelementen (PXL), die an jedem Durchschneidungspunkt der Gateleitungen und der Datenleitungen, die einen Anzeigebereich (1) bilden, vorgesehen sind,
eine Vertikal-Abtastschaltung (2) zum sequentiellen Vertikal-Abtasten jeder Gateleitung, um Bildelemente für jede horizontale Zeile auszuwählen, und
eine Horizontal-Abtastschaltung (3) zum Abtasten von Bildsignalen und nachfolgenden Einschreiben der Bildsignale in Bildelemente in einer ausgewählten horizontalen Zeile durch punktsequentielles Abtasten, 35
40
45

dadurch **gekennzeichnet**, dass

die Datenleitungen in zwei Abschnitten definiert sind, Wirkdatenleitungen (Y), die in dem Anzeigebereich vorgesehen sind, und Blinddatenleitungen (YD), die ausserhalb des Anzeigebereichs vorgesehen sind, wobei sich die Blinddatenleitungen mit dem Endabschnitt der Gateleitungen in Übereinstimmung mit der Richtung des Abtastens der Horizontal-Abtast-

schaltung durchschneiden,
die Horizontal-Abtastschaltung (3) dazu bestimmt ist, ein erstes Abtasten horizontal in jeder der Wirkdatenleitungen mit einer Abtastzeit einer Wirkdatenleitung durchzuführen, die sich mit den jeweiligen Abtastzeiten einer Vielzahl von Wirkdatenleitungen überlappt, und jedem ersten Abtasten nachfolgend ein zweites Abtasten horizontal in den Blinddatenleitungen mit der gleichen überlappten Abtastzeit, wie sie beim Abtasten der Wirkdatenleitungen benutzt wird, durchzuführen, und
zumindest so viele Blinddatenleitungen vorgesehen sind, wie es gleichzeitig abgetastete Leitungen bei dem horizontalen Abtasten gibt, die sich aus der Überlappung der Vielzahl von Abtastzeiten ergeben.

2. Aktivmatrix-Anzeigeeinrichtung nach Anspruch 1, wobei Blindbildelemente, die den Blinddatenleitungen entsprechen, vorgesehen sind.
3. Aktivmatrix-Anzeigeeinrichtung nach Anspruch 1, wobei nur in den Datenleitungen Bildelemente vorgesehen sind.

Revendications

1. Dispositif d'affichage à matrice active, comprenant :

une pluralité de lignes de grille (X) disposées sur des lignes horizontales.
une pluralité de lignes de données (Y) disposées verticalement,
une pluralité d'éléments d'image (PXL), disposés à chaque intersection desdites lignes de grille et desdites lignes de données, qui constituent la région d'affichage (1),
un circuit de balayage vertical (2) servant à balayer verticalement chaque ligne de grille en séquence afin de sélectionner des éléments d'image sur chaque ligne horizontale, et
un circuit de balayage horizontal (3) servant à échantillonner des signaux d'image et à écrire ensuite les signaux d'image sur des éléments d'image se trouvant sur une ligne horizontale sélectionnée, par balayage à séquence de points, 30
35
40
45

le dispositif étant caractérisé en ce que :

lesdites lignes de données sont définies en deux parties, des lignes de données réelles (Y) disposées dans ladite région d'affichage et des lignes de données fictives (YD) disposées à l'extérieur de ladite région d'affichage, lesdites lignes de données fictives croisant la partie ter-

minale des lignes de grille suivant la direction de balayage du circuit de balayage horizontal, ledit circuit de balayage horizontal (3) est conçu pour effectuer un premier balayage horizontalement sur chaque dite ligne de données réelle, 5
suivant un positionnement temporel d'échantillonnage d'une ligne de données réelle se chevauchant avec les positionnements temporels d'échantillonnage respectifs d'une pluralité de lignes de données réelles, et pour, à la suite de 10
chaque dit premier balayage, effectuer un deuxième balayage horizontalement sur lesdites lignes de données fictives suivant le même positionnement temporel d'échantillonnage chevauché que celui utilisé dans le balayage 15
des lignes de données réelles, et
les lignes de données fictives sont prévues en un nombre au moins égal à celui des lignes simultanément balayées dans le balayage horizontal du fait du chevauchement de la pluralité 20
de positionnements temporels d'échantillonnage.

2. Dispositif d'affichage à matrice active selon la revendication 1, où des éléments d'image fictifs correspondant auxdites lignes de données fictives sont prévus. 25
3. Dispositif d'affichage à matrice active selon la revendication 1, où des éléments d'image ne sont prévus que sur lesdites lignes de données. 30

35

40

45

50

55

FIG. 1

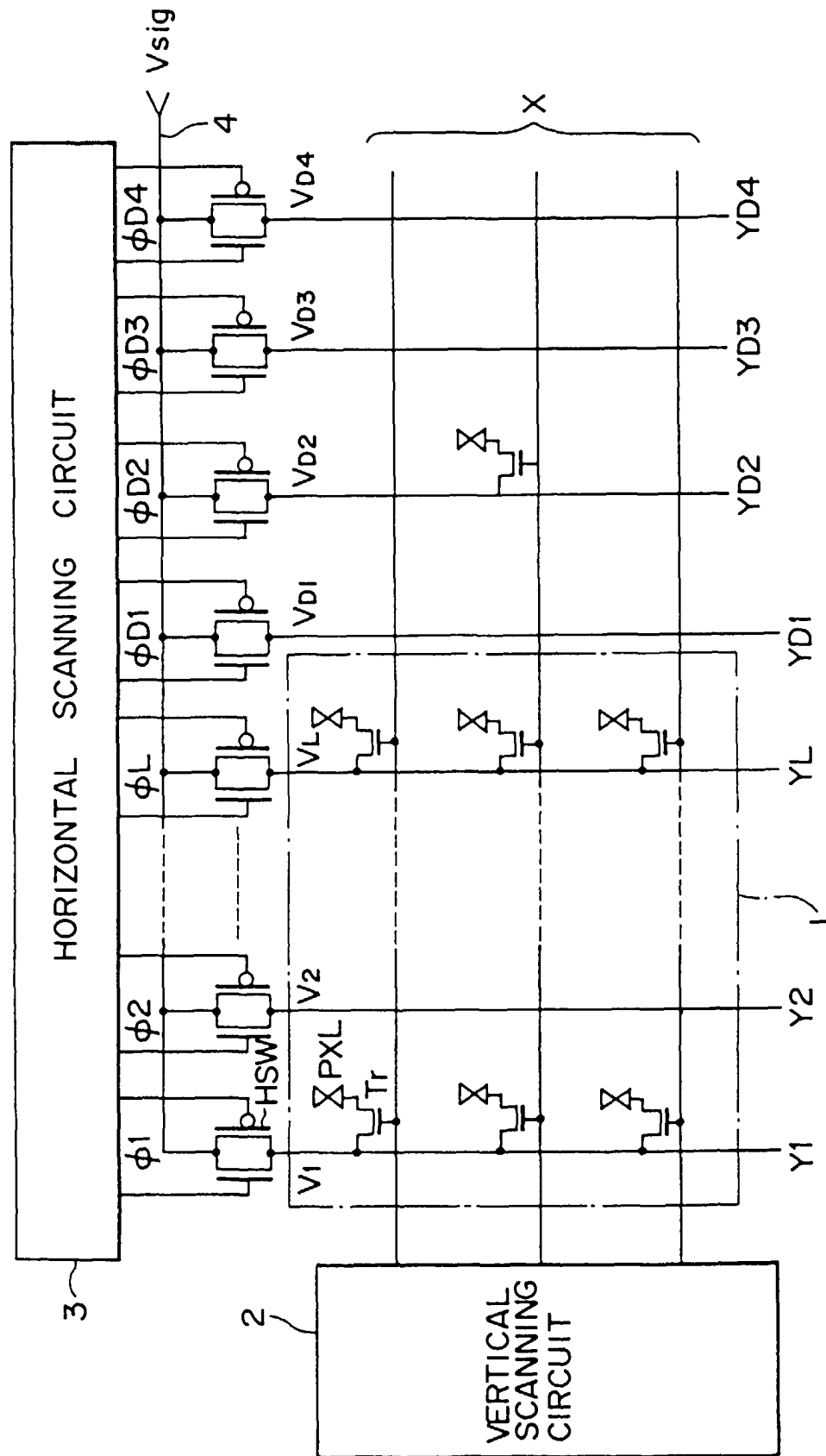


FIG. 2

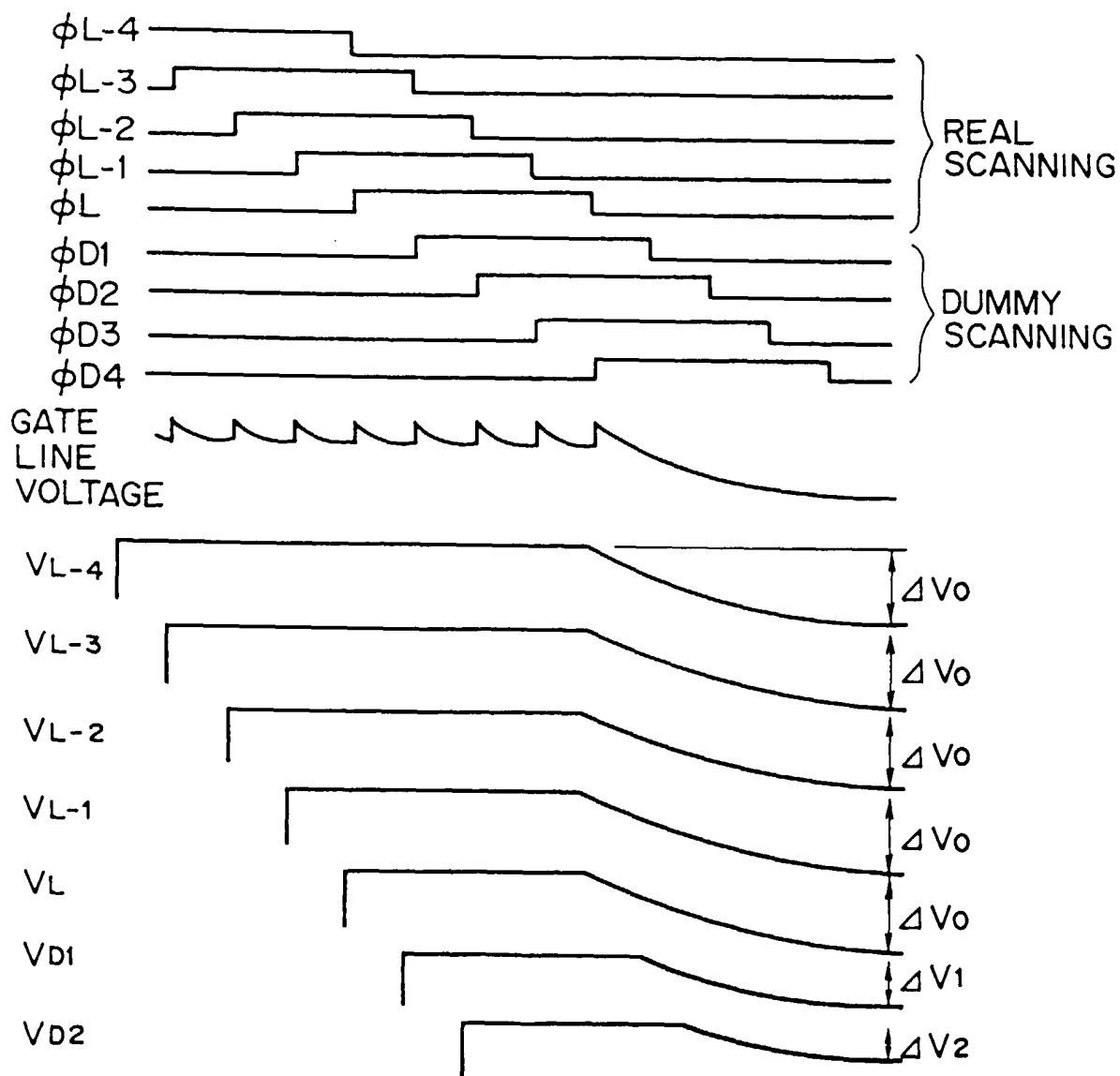


FIG. 3

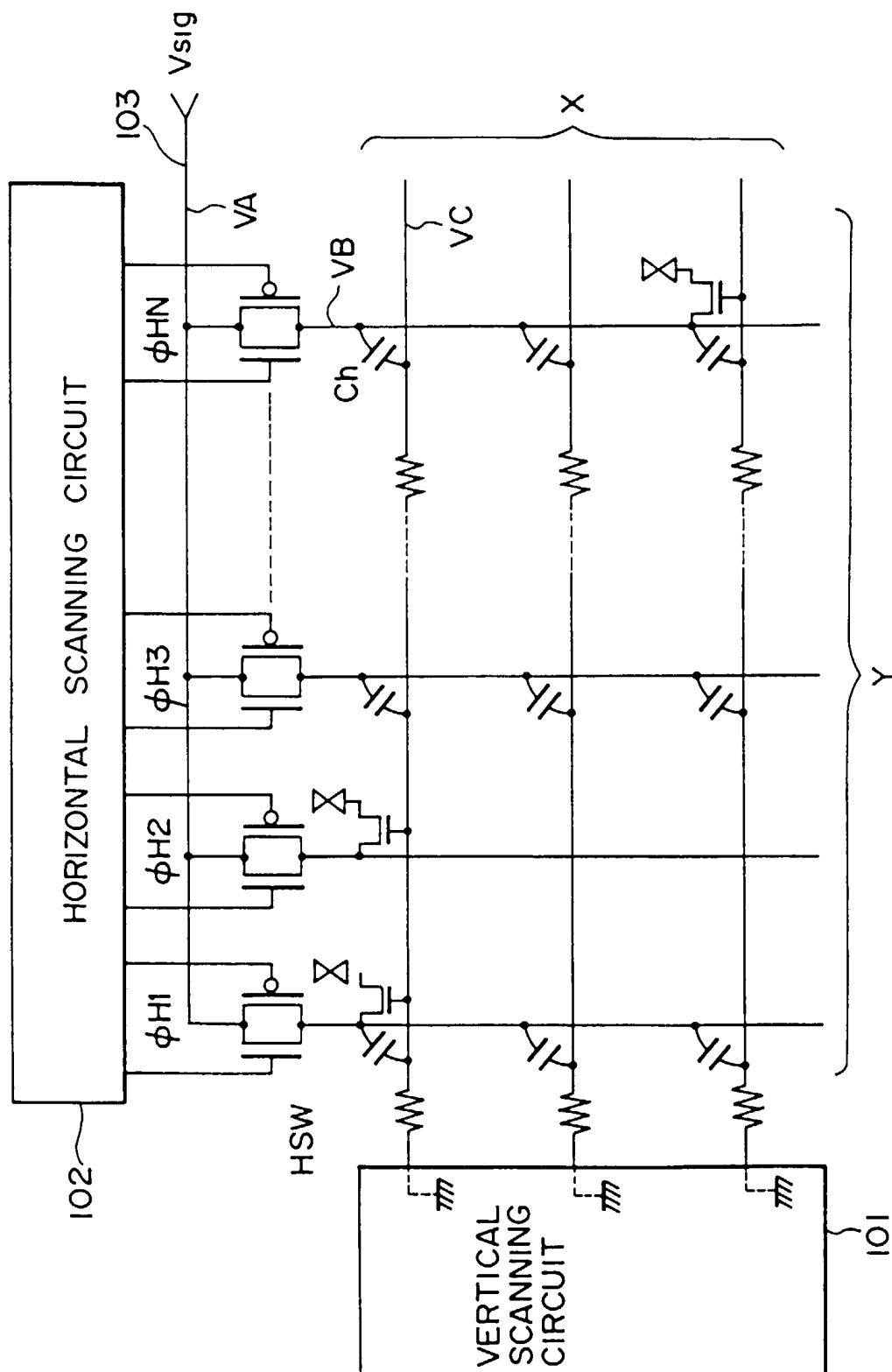


FIG. 4

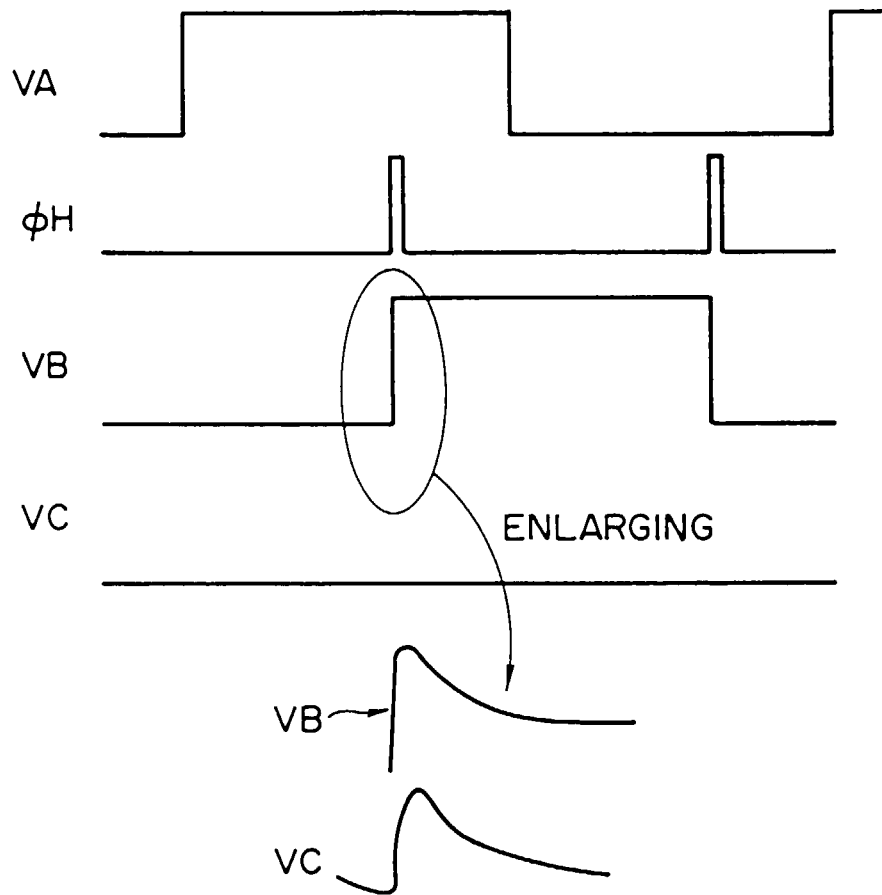


FIG. 5

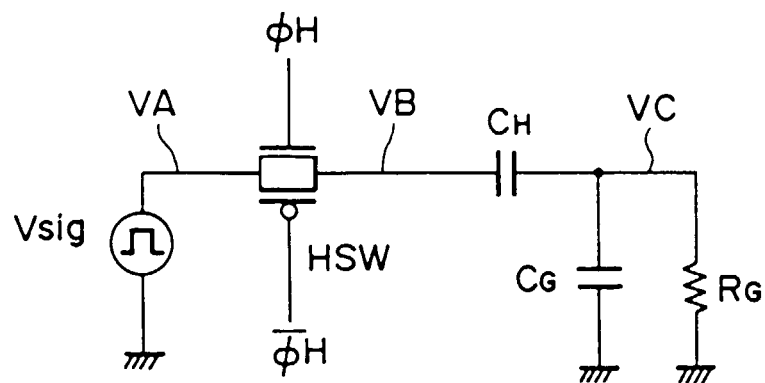


FIG. 6

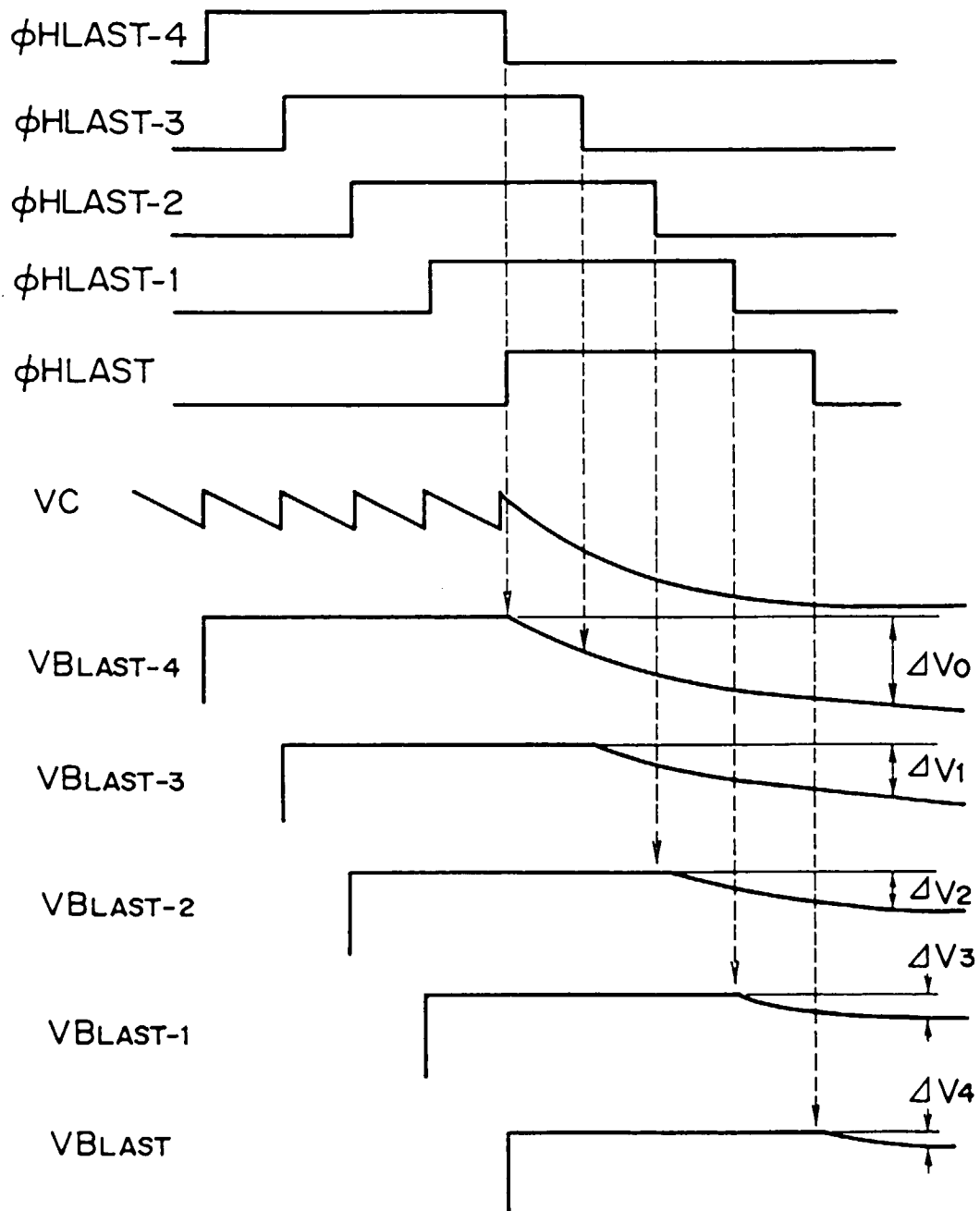


FIG. 7

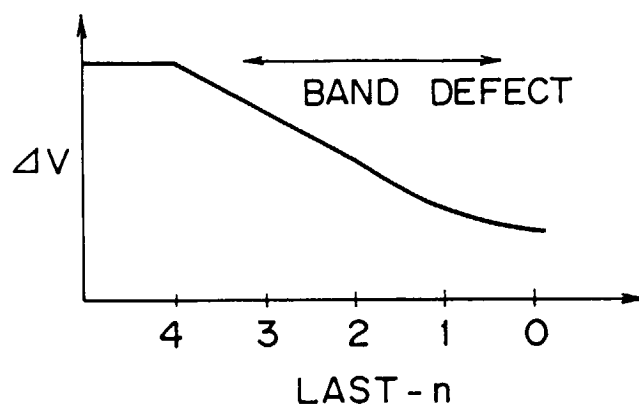


FIG. 8

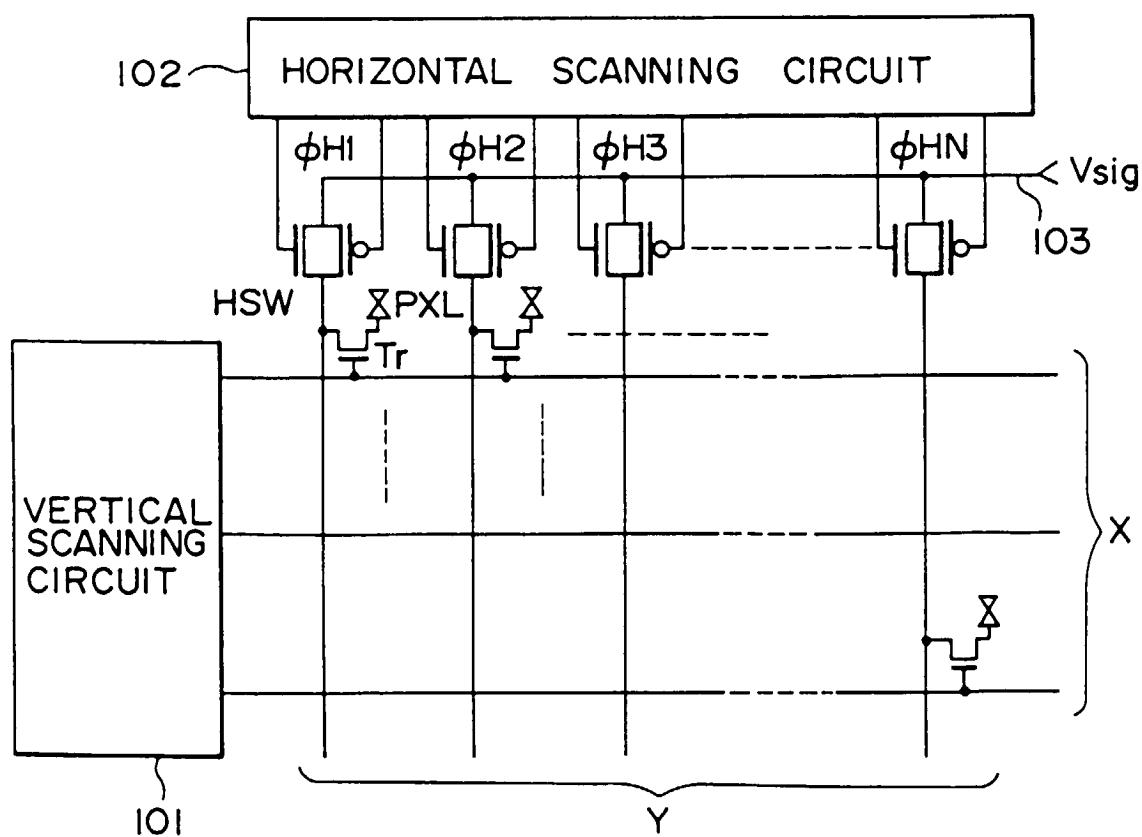


FIG. 9

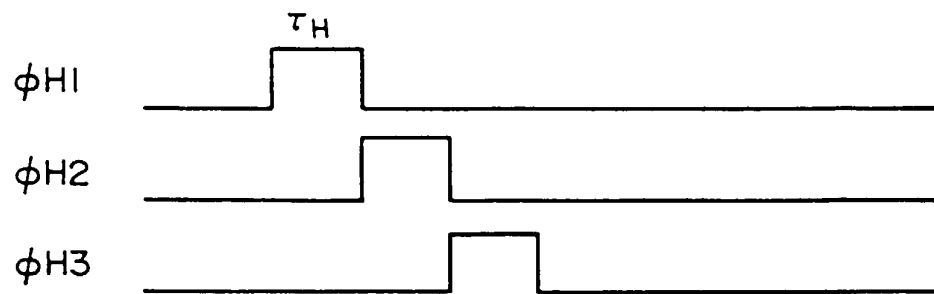


FIG. 10

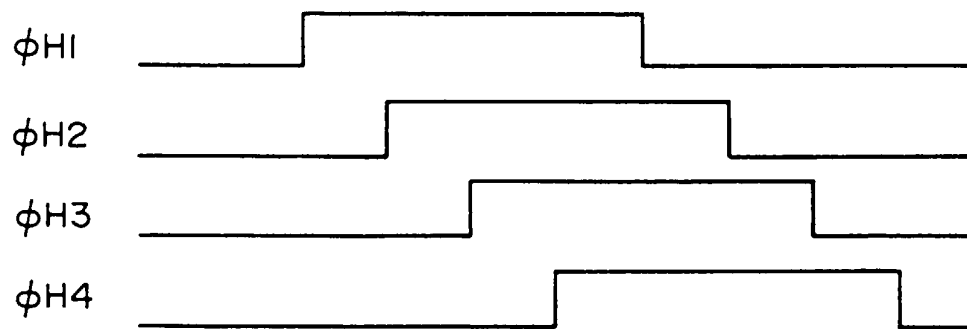
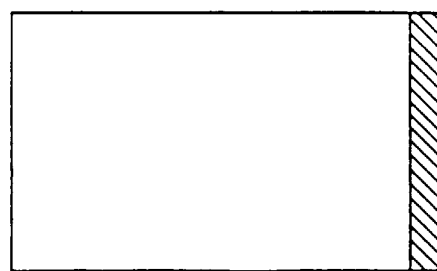


FIG. 11

HORIZONTAL SCANNING DIRECTION



104