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## (54) Method and apparatus for controlling the power consumption of an electronic device.

(57) The invention relates to a method for reducing power consumption of an electronic device comprising at least one voltage regulator. The regulating loop of at least one voltage regulator of the electronic device is controlled into a slower mode during periods when normal voltage regulator accuracy is not required, this period being known by the electronic device. The voltage regulator loop is controlled into a slower mode by switching the slew rate into a slower mode with the aid of an auxiliary input (SLEEP) arranged in the voltage regulator's differential amplifier (2) and by decreasing the current flowing through the differential amplifier. The invention is applicable in different electronic devices, particularly in battery powered devices in order to increase the operational time of the battery. For instance, in order to reduce the power consumption the voltage regulator of a mobile telephone can be switched into a slower mode between the control channel messages received from a base station.

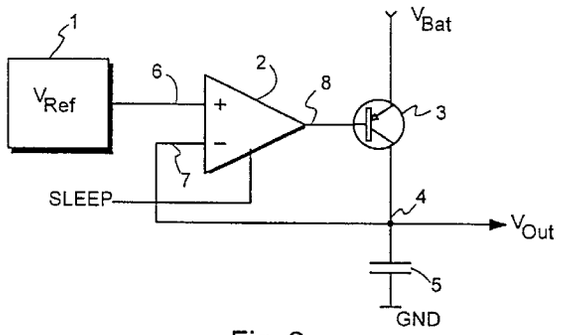


Fig. 2

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The present invention relates to a method and apparatus for controlling the power consumption of an electronic device comprising an improved voltage regulator.

Today a multitude of different battery powered devices are available to the consumer. These devices include, for example, mobile telephones, portable computers, portable telefax terminals, portable copying machines, portable oscilloscopes, portable hospital equipment, and so on. Here, a battery refers to any component which stores electrical energy, for example a rechargeable battery, a disposable battery, or an accumulator.

In order to illustrate an application area and advantages of the invention relative to the prior art, consideration will now be given to a mobile telephone as an example of an electronic device,

A cellular telephone system, such as the GSM (Groupe Speciale Mobile) system, usually comprises a number of base stations, each providing service in a predefined geographical area or cell. Each base station broadcasts messages to the mobile telephones situated within the cell area. The mobile telephones comprise a microprocessor, a transceiver, and a decoder controlled by the microprocessor. In battery powered mobile telephones the battery will usually last, between charging, approximately eight hours when the telephone is in idle mode and approximately one to two hours in talk mode, in which the telephone transmits and receives data and/or speech.

The mobile telephone and the base station communicate via a radio path assigned to the mobile telephone network. The radio path conveys both speech and signalling information used to control the operation of the mobile telephones and their allocation to the radio path. In the GSM system for example, two frequency bands of 25 MHz each are reserved for the radio path on the 900 MHz band; the band 890 - 915 MHz is reserved for uplink communication in the direction from the mobile telephone to the base station (transmit frequency band), and 935 - 960 MHz is reserved for the downlink direction from the base station to the telephone (receive frequency band). These frequency bands are divided in 124 frequency channels at intervals of 200 kHz. Each frequency channel is further divided in eight time slots, i.e. the GSM system utilises time division multiple access (TDMA), where each mobile telephone is allocated one time slot for the transmission and reception, so that each frequency channel of 200 kHz can simultaneously serve eight telephones. Thus the GSM system has a total of 992 channels.

The GSM system, which is based on time division multiple access (TDMA) will not be described in greater detail here, because it is well known by a person skilled in the art, and the system is exactly specified in the GSM specifications and presented , for example, in the article M.R.L. Hodges: "The GSM radio interface", British Telecom Technological Journal, Vol. 8, No 1, 1990, p. 31 - 43, the contents of which is incorporated herein by reference.

In the GSM mobile system there is specified the concept of an idle mode, in which a mobile telephone listens to and reconstructs system information messages sent by the base station as well as listening for paging messages which prompts the telephone that a call is waiting. The paging message is a common concept in cellular mobile telephone systems, and is transmitted as an impulse by the base station indicating to the mobile telephone that there is a call waiting. In reply the mobile telephone responds to the base station in order to establish a communication link between the mobile telephone and the base station.

In mobile telephones there is known a power saving mode, whereby certain circuits, such as the microprocessor circuits controlling the operation of the mobile telephone, are switched into a mode in which their power consumption is reduced. In this power saving mode clock frequencies are lowered, and some of the clocks are even stopped. European patent publication EP 473 465 presents a way to implement such a power saving mode.

Since in cellular mobile systems most messages transmitted by a base station to the mobile station are intended for a single mobile station, only a small number of all messages transmitted by the base station are intended for a specific mobile station. So as not to have the mobile stations continuously receive and decode all messages broadcast by the base station, the European patent publication EP 473 465 suggests, in order to save power, that the messages received by the mobile station are detected to find out whether a received message is intended for another mobile station, and in this case the battery power is lowered (the power saving state is activated) until the next message broadcast by the base station is expected to arrive. Battery saving according to the publication EP 473 465 is based on the receiving of a two-part message, the first part indicating that this message is intended for another mobile station, and that the message for this other mobile station contains a second part which, according to the publication EP 473 465, it is not necessary to receive if the message is addressed to another mobile station. Thus the mobile station can switch a considerable part of its receiving circuits into the power saving mode until the next message possibly directed to this mobile station is expected to arrive. This power saving mode is controlled by a timing circuit, which may be programmed to contain the start time of an expected next message.

Most electronic devices require different supply voltages for different sections of the circuitry, and as a result voltage regulators are usually used to generate these different supply voltages. A voltage regulator usually operates using a supply voltage from a voltage source, such as a battery. The voltage regulator

comprises typically three sections: (i) a reference voltage source generating a reference voltage, (ii) a differential or error amplifier, and (iii) an admitting or output element, usually a transistor. A simplified diagram of a voltage regulator is shown in Figure 1, where the reference voltage $V_{Ref}$ generated by the reference voltage source 1 is connected to the first input 6 (non-inverting input) of the error amplifier 2. The output 8 of the error amplifier is connected the base of the output transistor 3, and the emitter of the output transistor 3 is connected as feedback to the second input 7 (inverting input) of the error amplifier 2. The emitter of the output transistor is connected to the supply voltage $V_{Bat}$, which may be, for example, a battery, and the output $V_{out}$ of the voltage regulator is tapped from a junction 4 of part of the feedback loop between the transistor collector and the error amplifier feedback, whereby a load 5, in Figure 1 represented by a capacitor 5, is connected between this junction 4 and ground (GND).

The power consumption of a voltage regulator is the sum of the power consumed by each voltage regulator section:

- The power consumption of the reference voltage source is usually 10 - 500 μA. If there is more than one voltage regulator, then all voltage regulators usually use a common reference voltage source.
- The base current of the output transistor, which is usually of the order of the output current of the voltage regulator divided by the transistor gain. Thus this current mainly depends on the current consumed by the load connected to the voltage regulator output.
- The power consumption of the error amplifier.

The output current in the output line $V_{Out}$ also depends on the power consumption of the buffer stage of the error amplifier.

A single voltage regulator may consume a significant amount of power during operation. However, as electronic devices usually have several voltage regulators, to generate several different voltages, the combined power consumption of these voltage regulators form an increasingly significant contribution to the overall power consumption of the electronic device. This is particularly exemplified in mobile telephones operating in idle mode where the remainder of circuit functions within the telephone operate in a power saving mode. With the majority of circuits within the telephone becoming more efficient there exists a requirement for power saving modes in increasingly diverse components.

According to a first aspect of the invention there is provided a voltage regulator for providing a regulated output voltage from a voltage source, comprising an input for the voltage source, an output for providing the regulated output voltage, and a feedback loop for controlling the input voltage in response to the regulated output voltage, characterised in that the voltage regulator further comprises an auxiliary input and means for controlling the response time of the feedback loop in accordance with a signal input to the auxiliary input, and according to a second aspect of the present invention there is provided a method for controlling a voltage regulator having a feedback loop by controlling the response time of the feedback loop in accordance with a signal input to an auxiliary input of the feedback loop.

A method and apparatus in accordance with the invention has the advantage that greater control is achieved over the voltage regulator such that the power consumption of an electronic device, preferably a battery powered device, can be reduced in order to increase the operational time of the battery. The method and apparatus in accordance with the invention is based on the idea of reducing the power consumption of the voltage regulator by switching the voltage regulator feedback loop into a slower or lower accuracy mode when the device comprising the voltage regulator is on and operating in a passive mode. The advantage of being able to operate at a lower accuracy rather than switching the voltage regulator off is that it is be possible to rapidly restore the active operating state of the circuits to which the voltage regulator supplies voltages. If the supply voltage were removed from these circuits, it would be necessary to reset them before use and RAM memories would lose their stored data.

In a preferred embodiment an operating current is provided to the feedback loop, and the means for controlling the response time comprises means for controlling the operating current.

An advantage of this embodiment and the associated method is that by reducing the operating current at certain times, less power is consumed by the device incorporating the voltage regulator.

Suitably a reduction in the operating current results in a reduction of the response time of the feedback loop and an increase in the operating current results in an increase in the response time of the feedback loop.

In a preferred embodiment the feedback loop comprises a differential amplifier and the operating current is the operating current of the differential amplifier

Suitably a slew rate associated with the differential amplifier is dependent upon the magnitude of the operating current, and consequently the response time of the feedback loop is correspondingly dependant

The slew rate of the differential amplifier depends on the power supply current of the differential stage, whereby the slew rate decreases when this current is reduced. The control loop speed of the voltage regulator accordingly depends on the slew rate of the error amplifier, so that when the current of the

differential amplifier in the power supply differential stage is reduced, then the speed of the voltage regulator's control loop is reduced, so that the accuracy of the voltage regulator's output voltage is reduced.

The inactive state, the sleep mode, is an example of a mode in which the electronic device is on, but operationally in a passive state. The above described power saving mode is an example of an inactive state, in which the aim is to reduce the power consumption without switching off the circuits. The mobile telephone can be switched into the inactive state , for example, between the receiving of control channel messages in the GSM system. These messages from the base station arrive at the mobile telephone at certain intervals (about 2 to 10 seconds), whereby the mobile telephone knows that between them it can be switched into the inactive state, and excited to receive a control channel message (on a control channel BCCH, Broadcast Control Channel, reserved for this purpose), respectively. Another corresponding situation arises when the mobile telephone gets in a bad field and cannot contact the base station. Then the mobile telephone is temporarily switched into the inactive state in order to save power, and at intervals the mobile telephone is excited to test whether a connection to the base station can be established. In the analogue NMT mobile telephone system the corresponding state is the Battery Save mode, in which the mobile telephone Knows, according to information received from the base station, that it can switch into the inactive state for a certain period.

Generally we can switch the voltage regulator into a slower mode (i.e. to lesser accuracy) when the device (the mobile telephone, computer, measuring equipment, etc.) is on, but operationally in a passive state (or is not performing the actual functions of the device), but when we do not wish to switch off the supply voltages of the circuits.

Embodiments of the invention will now be described, by way of example, with reference to the accompanying drawings, in which:

Figure 1 is a block diagram of a known voltage regulator;

Figure 2 is a block diagram of a voltage regulator in accordance with the invention;

Figure 3 is a circuit diagram of a differential amplifier used in voltage regulators;

Figure 4 is a control circuit for use with the differential amplifier of Figure 3 in accordance with the invention;

Figure 5 is a modified version of the control circuit of Figure 4 in accordance with the invention;

Figure 6 is another embodiment of the voltage regulator control circuit in accordance with the invention;

Figure 7a is a block diagram of a first arrangement used to generate a control signal in accordance with the invention;

Figure 7b is a block diagram of a second arrangement used to generate a control signal in accordance with the invention; and

Figure 7c is a block diagram of a third arrangement used to generate a control signal in accordance with the invention.

Figure 1 has already been described in connection with the description of the prior art.

Figure 2 shows a block diagram of a voltage regulator in accordance with the invention. A reference voltage $V_{Ref}$ generated by the reference voltage source 1 is connected to the first input 6 (non-inverting input) of the error amplifier 2. The output 8 of the error amplifier is connected the base of the output transistor 3 (here a PNP transistor), and the collector of the output transistor 3 is connected as part of a feedback loop to the second input 7 (inverting input) of the error amplifier 2. The supply voltage $V_{Bat}$ which requires regulating, is supplied by a battery to the emitter of the output transistor. The output $V_{Out}$ of the voltage regulator is obtained at the junction 4 of the output from the transistor collector and the error amplifier feedback, whereby between the junction 4 and ground GND there is usually connected a load 5, represented in Figure 2 by the capacitor 5, for stabilising the output coupling so that it will not oscillate. In a voltage regulator in accordance with the invention the error amplifier 2 is provided with an auxiliary intermediate input SLEEP, for receiving a control signal with which the voltage regulator feedback loop can be controlled into having a slower response time, resulting in a reduction of its power consumption. Response time refers to the maximum speed at which the system can respond to an input. With a separate control signal received at the auxiliary intermediate input SLEEP, the voltage regulator can be switched back to the original speed, in which the voltage regulator will have a normal power consumption.

In Figure 2 the error amplifier (differential amplifier) is an operational amplifier, which drives an external bipolar transistor, for example, a PNP transistor, which in Figure 2 functions as the output transistor 3 of the voltage regulator. Hence the voltage source provides a current through the output transistor 3 which is regulated by the output of the operational amplifier and proceeds to supply a regulated voltage.

Figure 3 shows a circuit diagram of a differential amplifier, normally an operational amplifier. It comprises a differential amplifier stage, in which MOS transistors form a differential pair M1, M2 and a current mirror M3, M4 a current source transistor M5. A current source IBIAS produces a transistor M6 which forms a current mirror in combination with the transistor M5 mirroring to the differential stage the bias current $I_{bias}$ generated by the bias current supply, and a compensating capacitor $C_c$. The circuit of the operational amplifier shown in Figure 3 is known to a per-

son skilled in the art. The operational amplifier can as the output stage further comprise in a known way , for example, an inverter of the push-pull type.

The slew rate (SR) of the differential amplifier depends on the current $I_{ss}$ flowing into the current source transistor M5 and the capacitance $C_c$ of the compensating capacitor according to the equation SR = $I_{SS}/C_C$, the units of SR usually quoted as V/µs. The slew rate (SR) of the differential amplifier determines the speed of the voltage regulator's feedback loop and consequently the accuracy of the voltage regulator output voltage $V_{Out}$. As can be seen in the formula above, the slew rate (SR) of the differential amplifier is decreased when the current $I_{SS}$ flowing in the current source transistor M5 is reduced, and thus the speed of the voltage regulator's feedback loop will be less when the current $I_{SS}$ is reduced.

The slew rate SR or the current $I_{SS}$ can be controlled in at least two different ways in accordance with the invention, firstly by controlling the bias current $I_{bias}$ shown in Figure 3, or secondly by changing the ratio of the currents $I_{bias}$ and $I_{SS}$. An example of an embodiment of the first control method is shown in Figures 4 and 5, and an example of an embodiment of the second control method is shown in Figure 6.

Figure 4 shows a circuit diagram of a voltage regulator control circuit in accordance with the invention, in which the voltage regulator's differential amplifier bias current ($I_{bias}$ shown in Figure 3) is controlled. (The width/length ratio (or the W/L-ratio) of the transistors M5 and M6 shown in Figure 3 is not changed). The bias current $I_{bias}$ of the operational amplifier controls, by virtue of the current mirror formed by transistors M5 and M6, the current $I_{SS}$ flowing into the differential amplifier stage. The current generator of Figure 4 is situated in place of the current source IBIAS shown in Figure 3, i.e. the current generator according to Figure 4 is connected to the point 9 in Figure 3. The current generator in Figure 4 consists of a transistor M7 operating as a controlled switch, two resistors R1 and R1S, these resistors being connected to the supply voltage $V_{DD}$ as shown (e.g. +5 V, which may be directly the battery voltage). Depending on whether the transistor M7 is conducting or not, either one resistor R1 or two parallel resistors R1 and R1S are connected in series with the transistor M6. The circuit of Figure 4 can be implemented in an integrated circuit using MOS technology (as is shown in Figure 5) by using two MOS transistors MR1 and MR1S to act as the two resistors R1 and R1S. In Figures 4 and 5 the SLEEP control is connected to the gate of the transistor M7. When the electronic device is in normal operation the SLEEP input receives a supply voltage $V_{DD}$, whereby the NMOS transistor M7 is switched to a conducting mode and the bias current $I_{bias}$ is then determined by the parallel connection of the resistors R1 (MR1) and R1S (MR1S), giving the result $I_{bias} = (V_{DD}/R1S) + (V_{DD}/R1) = \{(1/R1S) + (1/R1)\} V_{DD}$. When it is desired to control the voltage regulator into a slower state, then a supply voltage lower than $V_{DD}$, or in this case the ground potential GND, is connected to the SLEEP input, such that the NMOS transistor M7 is switched to a cut-off state and the bias current $I_{bias}$ is determined solely by the resistor R1 (MR1), i.e. we obtain a bias current $I_{bias} = V_{DD}/R1 = (1/R1)V_{DD}$, lower than in the normal operation.

Figure 6 shows a circuit diagram of the second voltage regulator control circuit in accordance with the invention, in which is controlled the ratio of the bias current $I_{bias}$ of the voltage regulator's differential amplifier and the current $I_{SS}$ flowing in the differential stage. The current mirror formed by the transistors M5 and M6 shown in Figure 3 provide the differential stage current $I_{SS}$ as a mirror image of the bias current $I_{bias}$ according to the W/L-ratio (width/length ratio) of the transistors M5 and M6 in the following way: $I_{SS}/I_{bias} = (W_{M5}/L_{M5})/(W_{M6}/L_{M6}) = (L_{M6}W_{M5})/(W_{M6}L_{M5})$, or the current of the differential stage will be $I_{SS} = \{(L_{M6}W_{M5})/(W_{M6}L_{M5})\}I_{bias}$. Here we can see that a reduction of the W/L-ratio of the gate of transistor M5 will reduce the current $I_{SS}$ of the differential stage. The W/L-ratio can be changed by connecting another transistor M5S in parallel with the transistor M5, as is shown in Figure 6. The points 10 and 11 drawn in Figure 6 correspond to the points 10 and 11 drawn in Figure 3. When the transistor M5S is connected in parallel with the transistor M5 their combination corresponds to a single transistor M5', having gate dimensions formed by the sum of the gate dimensions of the transistors M5 and M5S, whereby $(W_{M5'}/L_{M5'}) = (W_{M5}/L_{M5}) + (W_{M5S}/L_{M5S})$. A transistor, such as the NMOS transistor in Figures 4 and 5, can be used as the switch S1 in Figure 6, and when the electronic device is in normal operation the SLEEP input receives the supply voltage $V_{DD}$, resulting in the switch S1 being closed or conducting. Here there is a parallel connection of resistors M5 and M5S, and thus a higher W/L-ratio results. When controlling the voltage regulator into a slower state or a state consuming less power, a supply voltage lower than $V_{DD}$, or in this case the ground potential GND, is connected to the SLEEP input, whereby the switch S1 is opened and the current $I_{SS}$ flows only through the transistor M5. A lower W/L-ratio is obtained and thus a lower current $I_{SS}$ flows through the differential stage than in the normal operation.

If the electronic device has several voltage regulators, then a common current generator, for example the current generator in Figures 4 or 5, can be arranged for all the voltage regulators, particularly for their differential stages. All voltage regulators can then be controlled either into the normal operation or into the lower speed state by simply using a single common control and a single common resistor R1S or transistor MR1S with the solution in Figures 4 and 5. If the solution in Figure 6 is used, then a transistor

M5S must be connected in parallel with the current source transistor M5 in the differential stage of each voltage regulator. However, if all transistors M5S are of the same type, their control can be combined as a single common SLEEP input line. An advantage of the solution in Figures 4 and 5 is that, because the bias current $I_{bias}$ is controlled, then in addition to a lower differential stage current $I_{SS}$, a lower bias current $I_{bias}$ is supplied by the current generator.

The SLEEP signal can be supplied in two different ways to the voltage regulator. In the first alternative the SLEEP signal can be supplied from an external source as a digital signal to the circuit containing the voltage regulator. The signal can be supplied from, e.g. the microcontroller 12 of the electronic device or from any corresponding circuit 13 controlling the functions of the device, as shown in Figures 7a and 7b. Other circuits (19) of the electronic device, (which may be a mobile telephone), to which the voltage regulator supplies the regulated supply voltages may also be controlled by microcontroller 12 or circuit 13. Within the integrated circuit containing the voltage regulator the SLEEP signal can be buffered in a buffer 14, if required, so that it is provided at a suitable level for the switch M7 or S1.

As a second alternative the SLEEP signal can be generated within the circuit IC containing the voltage regulator. If the voltage regulator has to supply current in accordance with some regular event, for example, in a digital mobile telephone in synchronism with the transmitter pulse sequence 16 (which can be for example, 50 Hz or 200 Hz), or in synchronism with the battery charger pulse sequence 15 during the trickle-charge (having , for example, a frequency of 1 Hz), then the SLEEP signal can be generated by the state machine 1 7 with the aid of the above mentioned pulses or any corresponding pulses. Such a state machine 17 needs information, for example, about the transmission starting point 18, after which it can itself synchronise the SLEEP signal with the aid of said pulse sequences or any corresponding signals. Figure 7c shows how a state machine is used as a part of the circuit IC containing the voltage regulator, and to generate the SLEEP signal for the voltage regulator. As in the case of the external connection, the state machine 17 supplies an output signal which may be buffered to a suitable level.

The power consumption of an electronic device containing at least one voltage regulator can be simply reduced by switching the voltage regulator's control loop to a slower state during periods when a normal voltage regulator accuracy is not required. A situation like this may occur when the device is generally operational in the passive state, but also when a circuit receiving its supply voltage from a certain voltage regulator is in such a state where its supply voltage is not required to have the normal accuracy. One such circuit is for instance the oscillator, whereby the voltage regulator supplying the supply voltage to the oscillator can be switched to a lower accuracy, for instance in a radiotelephone which does not transmit or receive, about which there is then information available to the microcontroller 12 or other circuit 13 controlling the functions of the radiotelephone.

In view of the foregoing description it will be evident to a person skilled in the art that various modifications may be made within the scope of the invention. For example a device with similar charcteristics could be used in place of the operational amplifier of figures 1 and 2.

The scope of the present disclosure includes any novel feature or combination of features disclosed therein either explicitly or implicitly or any generalisation thereof irrespective of whether or not it relates to the claimed invention or mitigates any or all of the problems addressed by the present invention. The applicant hereby gives notice that new claims may be formulated to such features during prosecution of this application or of any such further application derived therefrom.

## Claims

1. A voltage regulator for providing a regulated output voltage from a voltage source, comprising an input for the voltage source, an output for providing the regulated output voltage, and a feedback loop for controlling the input voltage in response to the regulated output voltage, characterised in that the voltage regulator further comprises an auxiliary input and means for controlling the response time of the feedback loop in accordance with a signal input to the auxiliary input.

2. A voltage regulator as claimed in claim 1, wherein an operating current is provided to the feedback loop, and the means for controlling the response time comprises means for controlling the operating current.

3. A voltage regulator as claimed in claim 2, wherein a reduction in the operating current results in a reduction of the response time of the feedback loop and an increase in the operating current results in an increase in the response time of the feedback loop.

4. A voltage regulator as claimed in claims 2 or 3, wherein the feedback loop comprises a differential amplifier and the operating current is the operating current of the differential amplifier.

5. A voltage regulator as claimed in claim 4, wherein a slew rate associated with the differential amplifier is dependent upon the magnitude of the op-

erating current, and consequently the response time of the feedback loop is correspondingly dependant.

6. A voltage regulator as claimed in any previous claim, further comprising a transistor having a first junction for acting as the input for the voltage source, a second junction acting as the output for the regulated voltage and a third junction acting as a return for the feedback loop.

7. A voltage regulator as claimed in claim 4, wherein the differential amplifier comprises a current mirror in which the operating current and a bias current mirror one another, such that the means for controlling the operating current of the differential amplifier comprises means for controlling the bias current.

8. A voltage regulator as claimed in claim 4, wherein differential amplifier comprises a current mirror in which the operating current and a bias current mirror one another, such that the means for controlling the operating current of the differential amplifier comprises means for controlling the ratio of the operating current and the bias current in the current mirror.

9. An electronic device incorporating the voltage regulator as claimed in any of claims 1 to 8.

10. A method for controlling a voltage regulator having a feedback loop by controlling the response time of the feedback loop in accordance with a signal input to an auxiliary input of the feedback loop.

11. A method as claimed in claim 10, wherein the step of controlling the response time comprises controlling an operating current of the feedback loop.

12. A method as claimed in claim 11, wherein the operating current is increased to increase the response time and the operating current is reduced to reduce the response time.

13. A method as claimed in any of claims 10 to 12, wherein the voltage regulator is incorporated into an electronic device and the signal input to an auxiliary input originates in the electronic device.

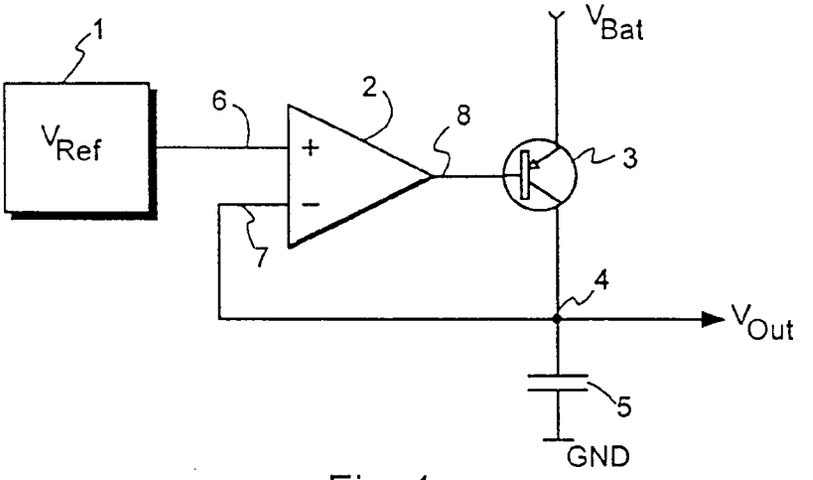


Fig. 1

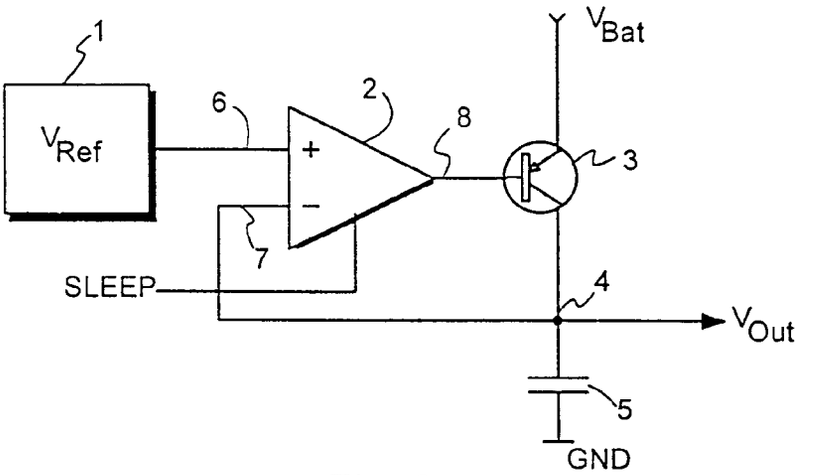


Fig. 2

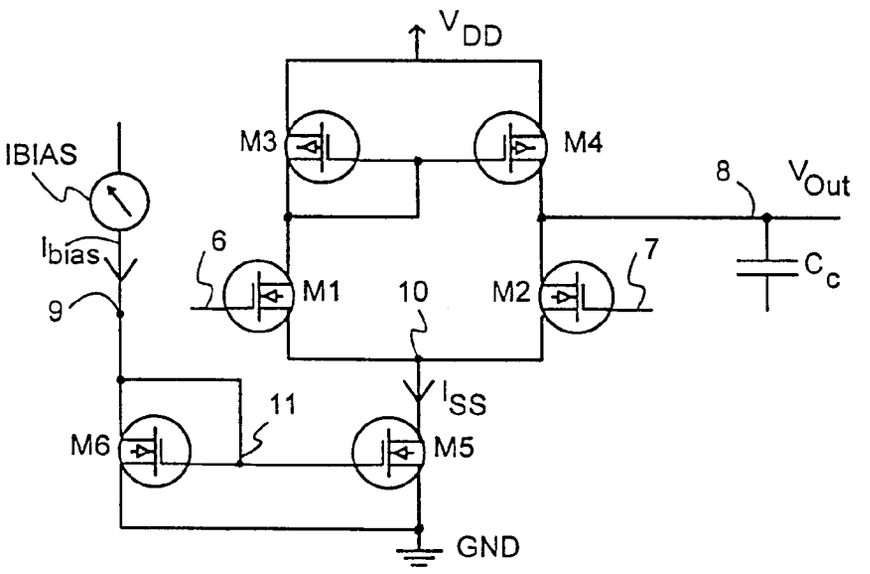


Fig. 3

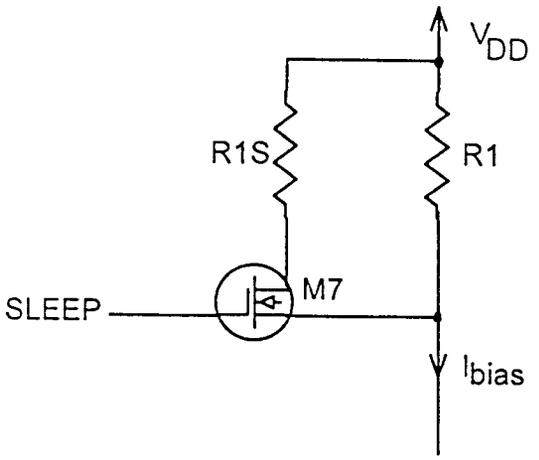


Fig. 4

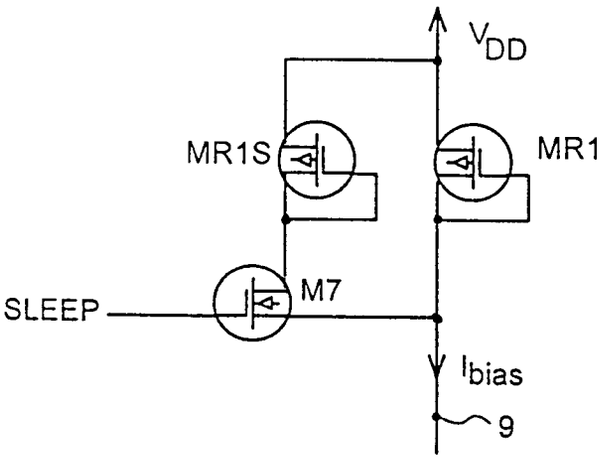


Fig. 5

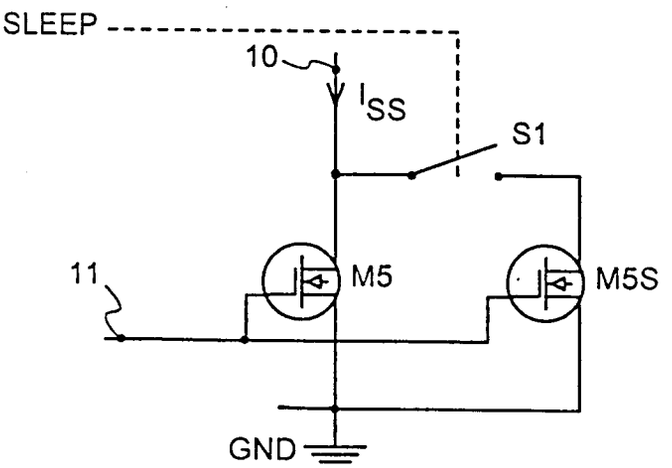


Fig. 6

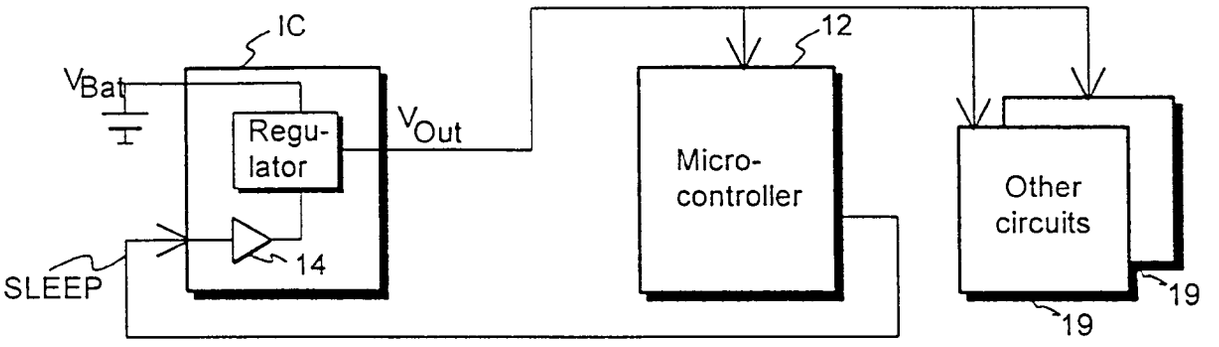


Fig. 7a

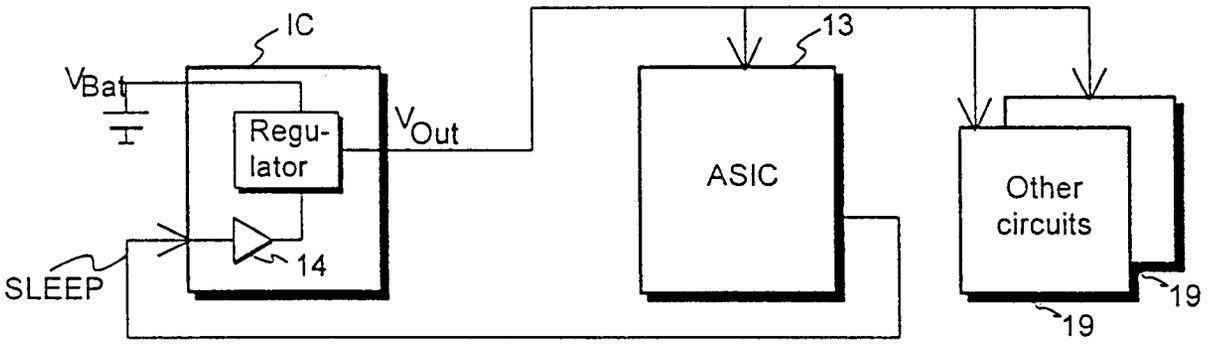


Fig. 7b

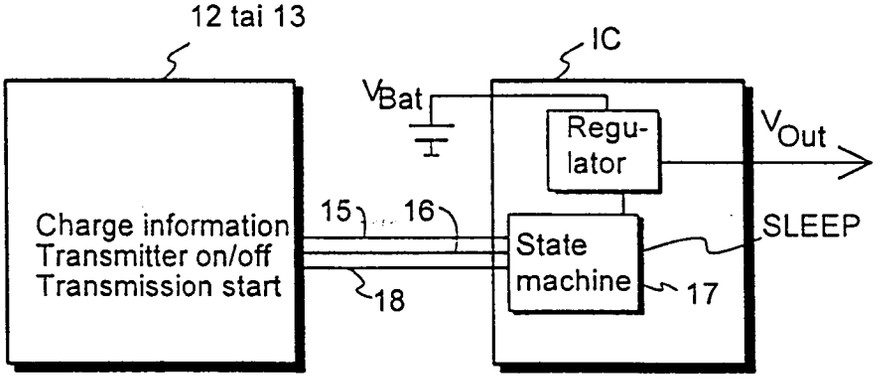


Fig. 7c