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(54) **FLAT PANEL DEVICE WITH INTERNAL SUPPORT STRUCTURE**

FLACHER BILDSCHIRM MIT INNERER TRAGSTRUKTUR

DISPOSITIF A PANNEAU PLAT POURVU D'UNE STRUCTURE INTERNE DE SUPPORT

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Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] This invention relates to flat panel devices such as flat cathode ray tube (CRT) displays. This invention also relates to techniques used in fabricating flat panel devices:

2. Related Art

[0002] U.S. Patent 4,451,759 discloses a flat panel CRT display in which a group of spacers are situated between a pair of glass plates. Each spacer consists of (a) a hollow cylinder integral with, and protruding from the interior surface of, one of the plates and (b) a cylindrical pin integral with, and protruding from the interior surface of, the other plate. The pins are respectively inserted into the hollow cylinders to form the spacers. U. S. Patent 4,451,759 mentions that a resistive coating can be provided on at least one of the pins and cylinders.

[0003] European Patent Publication 523,702 AI discloses a flat panel CRT display in which a face plate and a rear plate are separated by at least one spacer wall configured to avoid electrification (charging) of the outer wall surfaces. Each spacer wall typically consists of a main glass wall and an electroconductive film situated over both side surfaces of the main wall so as to contact the rear plate or electroconductive material situated over the rear plate. In some embodiments, the electroconductive film of each spacer wall extends over the main wall's end surface adjacent to the rear plate. The electroconductive film of each spacer is furnished with an electrical potential no greater than the potential supplied to electron-emissive elements formed over the rear plate. European Patent Application EP 0,580,244 A discloses a flat-panel type picture display device comprising the features as defined in the preamble of claim 1.

[0004] Numerous attempts have been made in recent years to construct a flat CRT display (also known as a "flat panel display") to replace the conventional deflected-beam CRT display in order to provide a lighter and less bulky display. In addition to flat CRT displays, other flat panel displays, such as plasma displays, have also been developed.

[0005] In flat panel displays, a faceplate, a backplate, and connecting walls around the periphery of the faceplate and backplate form an enclosure. In some flat panel displays, the enclosure is held at vacuum pressure, e.g., in flat CRT displays, approximately

$$1 \times 10^{-7} \text{ torr (1 torr} = 133.32 \frac{\text{kg}}{\text{ms}^2}\text{)}$$

The interior surface of the faceplate is coated with light

emissive elements such as phosphor or phosphor patterns which define the active region of the display. The light emissive elements are caused to emit light, e.g., cathodic elements located adjacent the backplate are excited to release electrons which are accelerated toward the phosphor on the faceplate, causing the phosphor to emit light which is seen by a viewer at the exterior surface of the faceplate (the "viewing surface").

[0006] During display operation, the electron-emissive elements are selectively excited to cause certain of the elements to emit electrons that move towards phosphors on the faceplate. These phosphors, upon being struck by the impinging electrons, emit light that is visible at the exterior surface of the faceplate.

[0007] In vacuum pressure flat panel displays, a force is exerted on the walls of the flat panel display due to the differential pressure between the internal vacuum pressure and the external atmospheric pressure that, left unopposed, can make the flat panel display collapse. In rectangular displays having greater than an approximately 1 inch (1 inch = 0.0254 cm) diagonal (the diagonal is the distance between opposite corners of the active region), the faceplate and backplate are particularly susceptible to this type of mechanical failure due to their high aspect ratio. Here, "aspect ratio" is defined as either the width, i.e., distance between the interior surfaces of opposing connecting walls, or the height, i.e., distance between the interior surface of the faceplate and the interior surface of the backplate, divided by the thickness. The faceplate or backplate of a flat panel display may also fall due to external forces resulting from impacts sustained by the flat panel display.

[0008] spacers have been used to internally support the faceplate and/or backplate. Previous spacers have been walls or posts located between pixels (phosphor regions that define the smallest individual picture element of the display) in the active region of the display.

[0009] The presence of the spacers may adversely affect the flow of electrons toward the faceplate in the vicinity of the spacer. For example, stray electrons may electrostatically charge the surface of the spacer, changing the voltage distribution near the spacer from the desired distribution and resulting in distortion of the electron flow, thereby causing distortions in the image produced by the display.

SUMMARY OF THE INVENTION

[0010] According to one aspect of the invention as defined in claim 1, a flat panel device includes a spacer for providing internal support of the device. In particular, for devices which operate with an internal vacuum pressure, the spacer prevents the device from collapsing as a result of stresses arising from the differential pressure between the internal vacuum pressure (i.e., any pressure less than atmospheric pressure) and the external atmospheric pressure. The spacer also internally supports the device against stresses arising from external impact forces. Ad-

ditionally, surfaces of the spacer within the enclosure are treated to prevent or minimize charge buildup on the spacer surfaces. Consequently, the presence of the spacer does not adversely affect the flow of electrons near the spacer, so that the image produced by the device is not distorted.

[0011] In one embodiment of the invention, a coating is formed on spacer surfaces, the coating being a material having a secondary emission ratio δ less than 4 and a sheet resistance between 10^9 and 10^{14} ohms/ \square . The coating is selected from a group of materials including chromium oxide, copper oxide, carbon, titanium oxide and vanadium oxide.

[0012] In another embodiment of the invention, a first coating is formed on spacer surfaces. A second coating is formed over the first coating. The first coating is a material having a sheet resistance between 10^9 and 10^{14} ohms/ \square . The second coating is a material having a secondary emission ratio δ less than 4.

[0013] In yet another embodiment of the invention, spacer surfaces are first surface-doped to produce a sheet resistance between 10^9 and 10^{14} ohms/ \square , then a coating is formed over the doped spacer surfaces, the coating being a material having a secondary emission ratio δ less than 4. The coating is selected from a group of materials including chromium oxide, copper oxide, carbon, titanium oxide and vanadium oxide.

[0014] In still another embodiment, spacer surfaces are surface-doped to produce a sheet resistance between 10^9 and 10^{14} ohms/ \square .

[0015] The spacer can be made of, for instance, ceramic and can be a spacer wall, a spacer structure, or some combination of a spacer wall, spacer walls, and spacer structure. The flat panel device also contains a mechanism to emit light. The flat panel device can include a field emitter cathode or a thermionic cathode.

[0016] In an additional embodiment of the invention, one or more electrodes are formed on the treated spacer surfaces. For instance, an electrode can be formed near an interface of the spacer and backplate, the voltage of the electrode being controlled to achieve a desired voltage distribution in the vicinity of the interface, thereby deflecting the flow of electrons as desired to correct for distortions resulting from imperfections in the surface treatment or misalignment of the spacer. In a further embodiment, this electrode can be formed with a serpentine path with respect to an interior surface of the backplate in order to achieve a desired voltage distribution.

[0017] A voltage divider establishes the voltage of each electrode. In one embodiment, the voltage divider is a resistive coating formed on the spacer surfaces. The sheet resistance of the coating must be closely controlled to achieve accurate voltages on the electrodes.

[0018] In the flat panel device of the invention, a strip of electrically conductive material ("edge metallization") is formed on an end surface of the spacer near the backplate, and in intimate contact with the entire length of the spacer. If a resistive coating is formed on the spacer sur-

faces, the edge metallization is electrically connected to the resistive coating. In that case, the edge metallization and the resistive coating are formed such that an interface between the edge metallization and the resistive coating is at a constant distance from an interior surface of the backplate. In like manner, edge metallization is formed between an edge surface of the spacer and the faceplate to establish good electrical connection between the faceplate and spacer.

[0019] In a method as defined in claim 21 according to another aspect of the invention, a flat panel device is assembled by mounting a spacer between a backplate and faceplate, treating surfaces of the spacer to prevent or minimize charge buildup on the spacer surfaces, coating an edge surface of the spacer with edge metallization such that the edge metallization forms an electrical connection between the spacer and backplate, and sealing the backplate and faceplate together to encase the spacer in an enclosure. The surfaces can be treated by forming a resistive coating or coatings, by surface doping, by surface doping and forming a resistive coating or coatings, or by firing to reduce the surface.

BRIEF DESCRIPTION OF THE DRAWINGS

[0020]

Figure 1A is a detailed perspective sectional view of a portion of a flat panel display.

Figures 1B and 1C are plan views of internal parts of the display of Figure 1A as seen respectively from the positions of, and in the directions of, arrows C and D. Figure 1D is a cross-sectional side view of the full flat-panel CRT display of Figure 1A.

Figure 2 is a simplified cross-sectional view illustrating a flat panel display including spacer walls and a spacer structure according to an embodiment of the invention.

Figures 3A and 3B are simplified cross-sectional views of a flat panel display according to an embodiment of the invention illustrating a coating formed on surfaces of spacer walls. Figure 3A is a cross-sectional view taken along plane 3B-3B of Figure 3B, and Figure 3B is a cross-sectional view taken along plane 3A-3A of Figure 3A.

Figure 4 is a graph of voltage versus distance from a field emitter in a direction perpendicular to a baseplate on which the field emitter is situated.

Figure 5 is a graph of secondary emission ratio versus voltage illustrating the characteristics of two materials.

Figures 6A through 6D are cross-sectional views illustrating the interface between a spacer wall, metallization and focusing ridges of the backplate according to various embodiments of the invention.

[0021] Like reference symbols are employed in the drawings and in the description of the preferred embod-

iments to represent the same or very similar item or items.

DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

[0022] In the following description, embodiments of the invention are described with respect to a flat cathode ray tube (CRT) display. It is to be understood that the invention is also applicable to other flat panel displays such as plasma displays or vacuum fluorescent displays. Further, the invention is not limited to use with displays, but can be used with other flat panel devices used for other purposes such as optical signal processing, optical addressing for use in controlling other devices such as, for instance, phased array radar devices, or scanning of an image to be reproduced on another medium such as in copiers or printers. Additionally, the invention is applicable to flat panel devices having non-rectangular screen shapes, e.g., circular, and irregular screen shapes such as might be used in a vehicle dashboard or an aircraft control panel.

[0023] Herein, a flat panel display is a display in which the faceplate and backplate are substantially parallel, and the thickness of the display is small compared to the thickness of a conventional deflected-beam CRT display, the thickness of the display being measured in a direction substantially perpendicular to the faceplate and backplate. Typically, though not necessarily, the thickness of a flat panel display is less than 2 inches (5.08 cm). Often, the thickness of a flat panel display is substantially less than 2 inches, e.g., 0.25 - 1.0 inches (0.64 - 2.54 cm).

[0024] Herein, "spacer" is used to describe generally any structure used as an internal support within a flat panel display. In this disclosure, specific embodiments of spacers according to the invention are described as a "spacer wall" or "spacer walls," or as a "spacer structure." "Spacer" subsumes "spacer wall," "spacer walls," and "spacer structure," as well as any other structure performing the above-described function of a spacer.

[0025] Generally, spacer walls and spacer structures in embodiments of the invention described below are made of a thin material which is readily workable in an untreated state and becomes stiff and strong after a prescribed treatment. The material must also be compatible with use in a vacuum environment. Further, the spacer walls and spacer structures are made of a material having a coefficient of thermal expansion that closely matches the coefficients of thermal expansion of the faceplate and backplate. Matching the coefficients of thermal expansion means that the spacer walls, faceplate and backplate expand and contract approximately the same amount during heating and cooling that occurs when the flat panel display is assembled or operated. Consequently, proper alignment is maintained among the spacer walls, faceplate and backplate.

[0026] In one example, spacer walls are made of a ceramic or glass-ceramic material. In another embodiment, spacer walls are formed from ceramic tape. Here-

after, in description of embodiments of the invention, ceramic or glass-ceramic tapes are the materials used for the spacer walls or spacer structures.

[0027] In this description, the term "ceramic" is often used, in the context of ceramic tape or ceramic layer or ceramic sheet. The term is intended to refer to any of a known family of glass-ceramic tapes, devitrifying glass tapes, ceramic glass tapes, ceramic tapes or other tapes which have plastic binders and ceramic or glass particles and which are flexible and workable in the unfired state, curable to a hard and rigid layer on firing, as well as other materials equivalent thereto, which are initially flexible and may be processed to a final hard and rigid state.

[0028] Spacer walls are formed and assembled into a flat panel display as follows. Strips, having a length and width chosen according to the particular requirements of the flat panel display are cut from a sheet of unfired ceramic or glass-ceramic tape. An advantage of using an unfired ceramic or glass-ceramic is that the strips can be easily fabricated by slitting or die-cutting. The strips are then fired. The fired strips (spacer walls) are placed at appropriate predetermined locations with respect to the faceplate and backplate. During assembly, the spacer walls are held in place so that they are properly aligned with respect to the faceplate and backplate.

[0029] The strips for the spacer walls can also be fabricated by first making and firing sheets of ceramic or glass-ceramic. The fired sheets can then be coated (as explained in more detail below) and cut into strips that form the spacer walls. Alternatively, the fired sheets can be cut into strips and then coated.

[0030] Figure 1A illustrates part of a flat-panel color CRT display that employs an area field-emission cathode in combination with a raised black matrix. The CRT display in Figure 1A contains transparent electrically insulating flat faceplate 302 and electrically insulating flat backplate 303. The internal surfaces of plates 302 and 303 face each other and are typically 0.01 - 2.5 mm apart. Faceplate 302 consists of glass typically having a thickness of 1 mm. Backplate 303 consists of glass, ceramic, or silicon typically having a thickness of 1 mm.

[0031] A group of laterally separated electrically insulating spacer walls 308 are situated between plates 302 and 303. Spacer walls 308 extend parallel to one another at a uniform spacing. Walls 308 extend perpendicular to plates 302 and 303. Each wall 308 consists of ceramic typically having a thickness of 80 - 90 μm . The center-to-center spacing of walls 308 is typically 8 - 25 mm. As discussed further below, walls 308 constitute internal supports for maintaining the spacing between plates 302 and 303 at a substantially uniform value across the entire active area of the display.

[0032] Patterned area field-emission cathode structure 305 is situated between backplate 303 and spacer walls 308. Figure 1B depicts the layout of field-emission cathode structure 305 as viewed in the direction, and from the positions, represented by arrows C in Figure 1A. Cathode structure 305 consists of a large group of

electron-emissive elements 309, a patterned metallic emitter electrode (sometimes referred to as base electrode) divided into a group of substantially identical straight lines 310, a metallic gate electrode divided into a group of substantially identical straight lines 311, and an electrically insulating layer 312.

[0033] Emitter-electrode lines 310 are situated on the interior surface of backplate 303 and extend parallel to one another at a uniform spacing. The center-to-center spacing of emitter lines 310 is typically 315 - 320 μm . Lines 310 are typically formed of molybdenum or chromium having a thickness of 0.5 μm . Each line 310 typically has a width of 100 μm . Insulating layer 312 lies on lines 310 and on laterally adjoining portions of backplate 303. Insulating layer 312 typically consists of silicon dioxide having a thickness of 1 μm .

[0034] Gate-electrode lines 311 are situated on insulating layer 312 and extend parallel to one another at a uniform spacing. The center-to-center spacing of gate lines 311 is typically 105 - 110 μm . Gate lines 311 also extend perpendicular to emitter lines 310. Gate lines 311 are typically formed with a titanium-molybdenum composite having a thickness of 0.02 - 0.5 μm . Each line 311 typically has a width of 30 μm .

[0035] Electron-emissive elements 309 are distributed above the interior surface of backplate 303 in an array of laterally separated multi-element sets. In particular, each set of electron-emissive elements 309 is located above the interior surface of backplate 303 in part or all of the projected area where one of gate lines 311 crosses one of emitter lines 310. Spacer walls 308 extend towards areas between the sets of electron-emissive elements 309 and also between emitter lines 310.

[0036] Each electron-emissive element 309 is a field emitter that extends through an aperture (not shown) in insulating layer 310 to contact an underlying one of emitter lines 310. The top (or upper end) of each field emitter 309 is exposed through a corresponding opening (not shown) in an overlying one of gate lines 311.

[0037] Field emitters 309 can have various shapes such as needle-like filaments or cones. The shapes of field emitters 309 is not particularly material here as long as they have good electron-emission characteristics. Emitters 309 can be manufactured according to various processes.

[0038] A light-emitting structure which contains a black matrix is situated between faceplate 302 and spacer walls 308. The light-emitting structure consists of a group of light-emissive regions 313, a pattern of substantially identical dark ridges 314 that reflect substantially no light, and light-reflective layer 315. Figure 1C depicts the layout of the light-emitting structure as viewed in the direction, and from the positions, represented by arrows D in Figure 1A.

[0039] Light-emissive regions 313 and dark ridges 314 are both situated on the interior surface of faceplate 302. Light-emissive regions 313 are located in spaces between dark ridges 314 (or vice versa). When regions 313

and ridges 314 are struck by electrons emitted from electron-emissive elements 309, light-emissive regions 313 produce light of various colors. Dark ridges 314 are substantially non-emissive of light relative to light-emissive regions 313 and thereby form a black matrix for regions 313.

[0040] More specifically, light-emissive regions 313 consist of phosphors configured in straight equal-width stripes extending parallel to one another at a uniform spacing in the same direction as gate lines 311. Each phosphor stripe 313 typically has a width of 80 μm . The thickness (or height) of phosphor stripes 313 is 1 - 30 μm , typically 25 μm .

[0041] Phosphor stripes 313 are divided into a plurality of substantially identical stripes 313r that emit red (R) light, a like plurality of substantially identical stripes 313g that emit green (G) light, and another like plurality of substantially identical stripes 313b (B) that emit blue light. Phosphor stripes 313r, 313g, and 313b are repeated at every third stripe 313 as indicated in Figure 1A. Each phosphor stripe 313 is situated across from a corresponding one of gate lines 311. Consequently, the center-to-center spacing of stripes 313 is the same as that of gate lines 311.

[0042] Dark ridges 314 similarly extend parallel to one another at a uniform spacing in the same direction as gate lines 311. The center-to-center spacing of ridges 314 is likewise the same as that of lines 311. The ratio of the average height of each dark ridge 314 to its average width is in the range of 0.5 - 3, typically 2. The average width of ridges 314 is 10 - 50 μm , typically 25 μm . The average height of ridges 314 is 20 - 60 μm , typically 50 μm .

[0043] The average height of dark ridges 314 exceeds the thickness (or height) of phosphor stripes 313 by at least 2 μm . In the typical case described above, ridges 314 extend 25 μm above stripes 313. Accordingly, ridges 314 extend further away from faceplate 302 than stripes 313.

[0044] Each ridge 314 contains a dark (essentially black), non-reflective region that occupies the entire width of that ridge 314 and at least part of its height. Figure 4A depicts an example in which these dark non-reflective regions encompass the full height of ridges 314. The later drawings illustrate examples in which the dark non-reflective regions occupy only parts of the ridge height.

[0045] The choice of materials for dark ridges 314 is wide. Ridges 314 can be formed with metals such as nickel, chrome, niobium, gold, and nickel-iron alloys. Ridges 314 can also be formed with electrical insulators such as glass, solder glass (or frit), ceramic, and glass-ceramic, with semiconductors such as silicon, and with materials such as silicon carbide. Combinations of these materials can also be utilized in ridges 314.

[0046] When ridges 314 consist of metal, they become sufficiently soft at a temperature in the range of 300-600°C as to allow objects, such as spacer walls 308,

to be pushed slightly into them. When ridges 314 are formed with solder glass, they so soften at a temperature in the ranges of 300-500°C. When the ridge material is glass, ridges 314 soften at a temperature in the range of 500-700°C.

[0047] Light-reflective layer 315 is situated on phosphor stripes 313 and dark ridges 314 as shown in Figure 1B. The thickness of layer 315 is sufficiently small, typically 50 - 100 nm, that nearly all of the impinging electrons from electron-emissive elements 309 pass through layer 315 with little energy loss.

[0048] The surface portions of light-reflective layer 315 adjoining phosphor stripes 313 are quite smooth. Layer 315 consists of a metal, preferably aluminum. Part of the light emitted by stripes 313 is thus reflected by layer 315 through faceplate 302. That is, layer 315 is basically a mirror. Layer 315 also acts as the final anode for the display. Because stripes 313 contact layer 315, the anode voltage is impressed on stripes 313.

[0049] Spacer walls 308 contact light-reflective layer 315 on the anode side of the display. Because dark ridges 314 extend further toward backplate 303 than phosphor stripes 313, walls 308 specifically contact portions of layer 315 along the tops (or bottoms in the orientation shown in Figure 1A) of ridges 314. The extra height of ridges 314 prevents walls 308 from contacting light-reflective layer 315 along phosphor stripes 313.

[0050] On the cathode side of the display, spacer walls 308 are shown as contacting gate lines 311 in Figure 1A. Alternatively, walls 308 may contact focusing ridges that extend above lines 311.

[0051] The air pressure external to the display is normally atmospheric--i.e., in the vicinity of 760 torr (1 torr = 133.32 kg/m s²). The internal pressure of the display is normally set at a value below 10⁻⁷ torr

$$(1 \text{ torr} = 133.32 \frac{\text{kg}}{\text{ms}^2}).$$

Since this is much less than the normal external pressure, high differential pressure forces are usually exerted on plates 302 and 303. Spacer walls 308 resist these pressure forces.

[0052] Phosphor stripes 313 can be damaged easily if mechanically contacted. Because the extra height of dark ridges 314 creates spaces between walls 308 and the portions of light-reflective layer 315 along stripes 313, walls 308 do not exert their resistance forces directly on stripes 313. The amount of damage that stripes 313 could otherwise incur as a result of these resistive forces is greatly reduced.

[0053] The display is subdivided into an array of rows and columns of picture elements ("pixels"). The boundaries of a typical pixel 316 are indicated by lines with arrowheads in Figure 1A and by dotted lines in Figures 1B and 1C. Each emitter line 310 is a row electrode for one of the rows of pixels. For ease of illustration, only

one pixel row is indicated in Figures 1A, 1B, and 1C as being situated between a pair of adjacent spacer walls 308 (with a slight, but inconsequential, overlap along the sides of the pixel row). However, two or more pixel rows, typically 24 - 100 pixel rows, are normally located between each pair of adjacent walls 308.

[0054] Each column of pixels has three gate lines 311: (a) one for red, (b) a second for green, and (c) the third for blue. Likewise, each pixel column includes one of each of phosphor stripes 313r, 313g, and 313b. Each pixel column utilizes four of dark ridges 314. Two of ridges 314 are internal to the pixel column. The remaining two are shared with pixel(s) in the adjoining column(s).

[0055] Light-reflective layer 315 and, consequently, phosphor stripes 313 are maintained at a positive voltage of 1,500 - 10,000 volts relative to the emitter-electrode voltage. When one of the sets of electron-emissive elements 309 is suitably excited by appropriately adjusting the voltages of emitter lines 310 and gate lines 311, elements 309 in that set emit electrons which are accelerated towards a target portion of the phosphors in corresponding stripe 313. Figure 1A illustrates trajectories 317 followed by one such group of electrons. Upon reaching the target phosphors in corresponding stripe 313, the emitted electrons cause these phosphors to emit light represented by items 318 in Figure 1A.

[0056] Some of the electrons invariably strike parts of the light-emitting structure other than the target phosphors. The tolerance in striking off-target points is less in the row direction (i.e., along the rows) than in the column direction (i.e., along the columns) because each pixel includes phosphors from three different stripes 313. The black matrix formed by dark ridges 314 compensates for off-target hits in the row direction to provide sharp contrast as well as high color purity.

[0057] Figure 1D depicts a cross section of the full CRT of Figure 1A. An electrically insulating outer wall 304 extends between plates 302 and 303 outside the active device area to create a sealed enclosure 301. Outer wall 304, which can be formed by four individual walls arranged in a square or rectangle, typically consists of glass or ceramic having a thickness of 2 - 3 mm. As indicated in Figure 4D, spacer walls 308 typically extend close to outer wall 304. Spacer walls 308 could, however, contact outer wall 304.

[0058] Back plate 303 extends laterally beyond faceplate 302. Electronic circuitry (not shown) such as leads for accessing emitter lines 310 and gate lines 311 is mounted on the interior surface of back plate 303 outside outer wall 304. Light-reflective layer 315 extends through the perimeter seal to a contact pad 319 to which the anode/phosphor voltage is applied.

[0059] Figure 2 is a simplified cross-sectional view, viewed illustrating flat panel display 600 including cathode spacer walls 607 and anode spacer structure 608 according to an embodiment of the invention. Faceplate 602, backplate 603, a top wall (not shown), a bottom wall (not shown), and side walls 604a, 604b form enclosure

601 which is held at vacuum pressure, e.g., approximately 1×10^{-7} torr

$$(1 \text{ torr} = 133.32 \frac{\text{kg}}{\text{ms}^2}).$$

The interior side of faceplate 602 is coated with phosphor. Layer 605 is formed between faceplate 602 and backplate 603 within enclosure 601 and extends through a sealed area of the top wall, bottom wall and side walls 604a, 604b to the outside of enclosure 601. Addressing grid 606 is formed on the portion of layer 605 corresponding to the active region of faceplate 602. Cathode spacer walls 607 and anode spacer structure 608 (referred to as a "grid-to-grid spacer structure") are disposed between backplate 603 and addressing grid 606, and faceplate 602 and addressing grid 606, respectively.

[0060] A thermionic cathode is located between addressing grid 606 and backplate 603. The thermionic cathode includes cathode wires 609, backing electrodes 612 and electron steering grids 613. Cathode wire 609 is heated to release electrons. A voltage may be applied to backing electrode 612 to help direct the electrons toward addressing grid 606. Electron steering grid 613 may be used to help extract electrons from cathode wire 609 and distribute the flow of electrons evenly between each cathode spacer wall 607. Voltages applied to electrodes (not shown) formed on the surface of holes 611 formed in addressing grid 606 govern whether the electrons pass through addressing grid 606. Electrons that pass through addressing grid 606 continue through holes 614 in anode spacer structure 608 to strike the phosphor coated on faceplate 602.

[0061] In Figure 2, one cathode wire 609 is shown between each cathode spacer wall 607. It is to be understood that there can be more than one cathode wire 609 between each cathode spacer wall 607.

[0062] In each of the above-described examples, the spacers must not interfere with the trajectory of the electrons passing between the cathode and the phosphor coating on the faceplate. Thus, the walls of the spacers must be sufficiently electrically conductive so that the spacers do not charge up and attract or repel the electrons to a degree that unacceptably distorts the paths of the electrons. Additionally, the spacers must be sufficiently electrically insulative so that there is no large current flow from the high voltage phosphor resulting in large power losses. Spacers formed from electrically insulative material and coated with a thin electrically conductive material are preferred.

[0063] Figure 3A is a simplified cross-sectional view of a portion of flat panel display 900 including coating 904 formed on spacer walls 908 according to an embodiment of the invention, taken along plane 9B-9B of Figure 3B. Figure 3B is a simplified cross-sectional view of a portion of flat panel display 900, taken along plane 9A-9A of Figure 3A. Flat panel display 900 includes faceplate

902, backplate 903 and side walls (not shown) which together form sealed enclosure 901 that is held at vacuum pressure, e.g., approximately 1×10^{-7} torr or less.

[0064] Focusing ribs (or ridges) 912 are situated above the interior surface of backplate 903 and perpendicular to the plane of Figure 3A. In the trough formed between each pair of focusing ribs 912, field emitters 909 are formed on an interior surface of backplate 903. Field emitters 909 are formed in groups of approximately 1000. Although not illustrated in Figures 3A and 3B, a pattern of emitter-electrode lines analogous to emitter lines 310 in the embodiment of Figure 1A lie under field emitters 909 above backplate 903. Likewise a pattern of unshown gate-electrode lines analogous to gate lines 311 in Figure 1A are situated above field emitters 909.

[0065] A matrix of dark ridges 911 is situated within enclosure 901 on faceplate 902, as described in more detail above with respect to Figures 1A - 1D. Phosphor 913 is formed to partially fill each trough between ridges 911. Anode 914, which is a thin electrically conductive material such as aluminum, is formed on phosphor 913.

[0066] Spacer walls 908 support faceplate 902 against backplate 903. The surfaces of each spacer wall 908 intermediate the opposing ends are coated with resistive coating 904 or are surface doped, as described in more detail below. Resistive coating 904 prevents or minimizes charge build-up on spacer wall 908 that can distort the flow of electrons 915.

[0067] One end of each spacer wall 908 contacts a plurality of ridges 911 and is coated with edge metallization 905. An opposite end of each spacer wall 908 contacts a plurality of focusing ribs 912 and is coated with edge metallization 906. Edge metallization 905 and 906 can be made of, for instance, aluminum or nickel. Edge metallizations 905 and 906 provide good electrical contact between coating 904 and faceplate 902 or focusing ribs 912, respectively, so that the voltage at the ends of spacer walls 908 is well-defined and a uniform ohmic contact is formed. The interface between spacer wall 908, coating 904 and edge metallization 905 can take on a number of configurations, as described in more detail below. Electrodes 917 are formed on the coated (or doped) surfaces of each spacer wall 908, and are used to "segment" the voltage rise from emitters 909 to anode 914.

[0068] In another embodiment of the invention, spacer walls 908 are formed without electrodes 917.

[0069] Each group of field emitters 909 emit electrons 915 toward the interior surface of faceplate 902. Circuitry (not shown) is formed as part of flat panel display 900, e.g., on integrated circuit chips that can be attached to, for instance, an exterior surface of backplate 903, and used to control the voltage of electrodes 917. Typically, the voltage of each of electrodes 917 is set so that the voltage increases linearly from the voltage level at field emitters 909 to the higher voltage at anode 914. Thus, electrons 915 are accelerated toward faceplate 902 to strike phosphor 913 and cause light to emanate from flat

panel display 900.

[0070] For optimum focusing, the desired equipotential lines, in the plane of Figure 3A, near focusing ribs 912, follow a serpentine path, rising above focusing ribs 912 and falling above the cavity in which emitters 909 are located. However, the presence of spacer wall 909 imposes an equipotential line at this location, i.e., the bottom of spacer wall 909, that is straight. According to the invention, one of electrodes 917 can be located near the bottom of spacer wall 909 and formed in a serpentine path in order to create a potential field having equipotential lines with the desired serpentine shape.

[0071] Figure 4 is a graph of voltage versus distance 907 (Figure 3B) from field emitters 909. Anode 914 is spaced apart from field emitters 909 by distance 916, and is held at a higher voltage (designated as HV in Figure 4) than field emitters 909. For a group of field emitters 909 that are distant from spacer walls 908, e.g., field emitters 909b, spacer walls 908 do not interfere with the flow of electrons 915 from field emitters 909 and the voltage change from field emitters 909 to anode 914 is approximately linear as shown in Figure 4.

[0072] It is necessary that the voltage change near each spacer wall 908 also change linearly between field emitters 909 and anode 914, so that the flow of electrons is not distorted (and the display image thereby degraded). However, for a group of a field emitters 909 that are near one of spacer walls 908, e.g., field emitter 909a, the adjacent spacer wall 908 can interfere with the flow of electrons 915 from field emitters 909. Stray electrons 915 emitted from field emitters 909a will strike spacer wall 908, typically resulting in the accumulation of charge on spacer wall 908. For a given electron density (current density j) striking spacer wall 908, an amount of charge equal to $j \cdot (1 - \delta)$ accumulates at the surface of spacer wall 908. For $\delta \neq 1$, the accumulation of charge causes a change in voltage at the surface of spacer wall 908 from the desired voltage, resulting in a non-zero flow of electrons from spacer wall 908. If the conductivity of spacer wall 908 is low, the change in voltage will cause the electron flow near spacer wall 908 to be distorted, resulting in degradation of the image display.

[0073] Generally, the deviation of voltage near spacer wall 908 from the desired voltage (based on a linear voltage drop from field emitters 909 to anode 914) is given by the equation:

$$\Delta V = \rho_s \cdot [x \cdot (x-d)/2] \cdot j \cdot (1 - \delta) \quad (1)$$

where

ΔV = voltage deviation (in volts)
 ρ_s = sheet resistance of the surface of the spacer wall (in ohms/□)
 x = distance from nearest electrode, $0 < x < d$ (in cm)
 d = distance between electrodes (in cm)

j = current density striking the surface of the spacer wall (in amperes)
 δ = secondary emission ratio (dimensionless)

5 The above equation assumes that current at current density j strikes spacer wall 908 uniformly and that the sheet resistance ρ_s of spacer wall 908 is uniform. More exactly, equation (1) would account for the dependence of current density j on the position on spacer wall 908, and the dependence of secondary emission ratio δ on the exact voltage at the position on spacer wall 908.

[0074] As can be seen from equation (1), the maximum voltage deviation ΔV occurs at the midpoint between two electrodes 917 (i.e., the quantity $[x \cdot (x-d)/2]$ is maximized), and is proportional to the distance between the electrodes squared. For this reason, providing additional electrodes 917 minimizes the voltage deviation near spacer wall 908 and, thus, the distortion of the flow of electrons 915 toward faceplate 902. The addition of n electrodes of width w to a spacer wall 908 of height h reduces the power consumption of flat panel display 900 according to the ratio given below:

$$25 \quad \frac{P_{\text{NEW}}}{P_{\text{OLD}}} = \frac{d - nw}{d \cdot (n + 1)^2} \quad (2)$$

For example, the addition of four electrodes, each electrode being 4 mils wide, to a spacer wall 908 having a height h of 100 mils (1 mil = 0,000254 m) reduces the I^2R power loss for a given ΔV_{max} by a factor of approximately 30.

[0075] This more efficient charge bleed-off allows a higher value of sheet resistance ρ_s and significant savings in power consumption. Another advantage is that if electrodes 917 protrude slightly, electrodes 917 will intercept much of the charge, preventing the charge from striking the high resistance sections which hold off the voltage. However, each additional electrode 917 increases the manufacturing cost of display 900. The number of electrodes 917 included in flat panel display 900 is chosen as a trade-off between the aforementioned factors.

[0076] As further seen in equation (1), for a given number of electrodes 917, the voltage deviation ΔV also decreases as the sheet resistance ρ_s decreases, and as the secondary emission ratio δ approaches 1. Thus, it is desirable that the surfaces of spacer walls 908 have a low sheet resistance ρ_s and a secondary emission ratio δ that approaches 1. Since the secondary emission ratio δ can only go as low as zero, but can increase to a very high number, the secondary emission ratio requirement is typically stated as a preference for a material having a low value of secondary emission ratio δ .

[0077] Figure 5 is a graph of secondary emission ratio δ versus voltage illustrating the characteristics of two materials: material 1101 and material 1102. For most high resistivity materials, such as material 1101, the second-

ary emission ratio δ is greater than 1 (and frequently much greater) for an energy range between 100 volts to 10,000 volts, resulting in a positively charged surface. Anode 914 is typically maintained at a positive voltage of 1500 - 10,000 volts relative to emitters 909 as is the case with anode 315 and emitters 309 as described above for Figure 1A. Further, as described above, spacer walls 908 are preferably made of an electrically insulative (i.e., high resistivity) material. Thus, spacer walls 908 are typically positively charged (and frequently highly positively charged), resulting in distortion of the flow of electrons 915 from emitters 909.

[0078] However, material 1102 has a secondary emission ratio δ that, for the voltage range in flat panel display 900, remains near 1. Since the voltage deviation ΔV varies as the quantity $1-\delta$, when the surfaces of spacer walls 908 are made of material 1102, little charge (positive or negative) accumulates on the surfaces of spacer walls 908. Consequently, the presence of spacer walls 908 has little impact on the voltage drop between field emitters 909 and anode 914, and, therefore, the distortion of the flow of electrons 915 due to the presence of spacer walls 908 is minimized.

[0079] According to the invention, the surfaces of spacer walls 908 facing into enclosure 901 are treated with a material having a secondary emission ratio δ characteristic that looks much like that of material 1102 in Figure 11. Further, the surface is treated so that the surface resistance will be low relative to the bulk resistivity of spacer wall 908, enabling charge to flow easily from spacer walls 908 to backplate 903 or from faceplate 902, but not so low that there will be high current flow from the high voltage phosphor on faceplate 902 and, thus, large power loss.

[0080] In one embodiment of the invention, spacer walls 908 are ceramic and coating 904 is a material having a secondary emission ratio δ less than 4 and a sheet resistance ρ_s between 10^9 and 10^{14} ohms/ \square . In an additional embodiment, the material used for coating 904 has the above sheet resistance ρ_s and a secondary emission ratio δ less than 2. The coating 904 according to this embodiment is, for instance, chromium oxide, copper oxide, carbon, titanium oxide, vanadium oxide or a mixture of these materials. In a further embodiment, coating 904 is chromium oxide. Coating 904 has a thickness between 0.05 and 20 μm .

[0081] In another embodiment of the invention, coating 904 includes a first coating formed on spacer wall 908 of a material having a sheet resistance ρ_s between 10^9 and 10^{14} ohms/ \square without regard to the magnitude of the secondary emission ratio δ . The first coating is then covered by a second coating having a secondary emission ratio δ less than 4 in one embodiment, and less than 2 in another embodiment. The material for the first coating is, for instance, titanium-chromium-oxide, silicon carbide or silicon nitride. The material for the second coating is, for instance, chromium oxide, copper oxide, carbon, titanium oxide, vanadium oxide or a mixture of those materials.

The total thickness of coating 904 is between 0.05 and 20 μm .

[0082] In yet another embodiment of the invention, spacer walls 908 are surface doped to produce a sheet resistance ρ_s between 10^9 and 10^{14} ohms/ \square , then covered with coating 904 having a secondary emission ratio δ of less than 4 in one embodiment and less than 2 in another embodiment. The dopant can be, for instance, titanium, iron, manganese or chromium. Coating 904 is, for instance, chromium oxide, copper oxide, carbon, titanium oxide or vanadium oxide, a mixture of those materials. In one embodiment, coating 904 is chromium oxide. Coating 904 has a thickness between 0.05 and 20 μm .

[0083] In still another embodiment, spacer walls 908 are surface-doped to a concentration to produce a sheet resistance between 10^9 and 10^{14} ohms/ \square . The dopant can be, for instance, titanium, iron, manganese or chromium.

[0084] In another embodiment of the invention, spacer walls 908 are made of a partially electrically conductive ceramic or glass-ceramic material.

[0085] The above-described coating 904 can be formed on spacer wall 908 by any suitable method. For example, coating 904 can be formed according to well-known techniques by, for instance, thermal or plasma-enhanced chemical vapor deposition, sputtering, evaporation, screen printing, roll-on, spraying or dipping. Whatever method is used, it is desirable to form coating 904 with a sheet resistance uniformity of $\pm 2\%$. Typically this is done by controlling the thickness of coating 904 within a specified tolerance.

[0086] An alternative to coating spacer surfaces is to take advantage of a material contained in the initial ceramic layers which can be made to become slightly conductive in a later firing.

[0087] In the above embodiments, treatment of spacer walls to minimize or eliminate charging of the surfaces of the spacer walls is described. In embodiments of the invention including a spacer structure, e.g., spacer structure 608 (Figure 2), the surfaces of holes in the spacer structure through which electrons flow are treated, as described above, to minimize or eliminate charging of those surfaces.

[0088] Figures 6A through 6D are cross-sectional views illustrating the interface between a spacer wall, resistive coating, edge metallization and focusing ribs according to various embodiments of the invention. The coating in each embodiment can be one of the coatings described above with respect to Figures 3A and 3B. In each embodiment, a sharply defined edge metallization/resistive coating interface is formed that is straight and at a constant height above the cathode so that a straight equipotential is defined at the base of the spacer wall along the length of the spacer wall parallel to the backplate. Edge metallization according to the embodiments of the invention described below can be formed on the edge surfaces of the spacer walls by the techniques de-

scribed above for formation of resistive coating 904.

[0089] In Figure 6A, resistive coating 1204 is formed on side surfaces 1208a of spacer wall 1208. Coating 1204 is formed on side surfaces 1208a so that coating 1204 does not extend beyond the end of side surfaces 1208a. Edge metallization 1206 is formed on end surface 1208b of spacer wall 1208 so that edge metallization 1206 does not extend beyond coating 1204.

[0090] In Figure 6B, resistive coating 1214 is formed on side surfaces 1218a and end surface 1218b of spacer wall 1218 to entirely cover spacer wall 1218. Edge metallization 1206 is formed adjacent the portion of coating 1218 formed on end surface 1218b of spacer wall 1218 so that edge metallization 1206 does not extend beyond the edge of coating 1204.

[0091] In Figure 6C, resistive coating 1214 is formed on side surfaces 1218a and end surface 1218b of spacer wall 1218 to entirely cover spacer wall 1218. Edge metallization 1216 is formed adjacent the portion of coating 1214 formed on end surface 1218b of spacer wall 1218 such that metallization 1216 overlaps coating 1214 and extends around the corner of coating 1214 to a well-defined height.

[0092] In Figure 6D, resistive coating 1204 is formed on side surfaces 1208a of spacerwall 1208, as in Figure 6A, so that coating 1204 does not extend beyond the end of side surfaces 1208a. Edge metallization 1216 is formed adjacent the portion of coating 1204 formed on end surface 1208b of spacer wall 1208 such that metallization 1216 overlaps coating 1204 and extends around the corner of coating 1204 to a well-defined height.

[0093] As described above, electrodes 917 are formed at intervals on the surfaces of spacer walls 908 that are exposed within enclosure 901. The voltages at these electrodes 917 are set by a voltage divider. The voltage divider can either be coating 904 or a resistive strip, outside the active region of display 900, connected to electrically conductive traces extending from each of electrodes 917. In order to achieve the desired voltages on each electrode 917, the voltage divider can be "trimmed" by removing material from the voltage divider at selected locations to increase the resistance at those locations as necessary. The trimming can be done by, for instance, using a laser to ablate material from the voltage divider. Alternatively, material can be removed from selected ones of the electrically conductive traces, e.g., the length of one or more of the traces outside of enclosure 901 can be shortened, extending from a voltage divider outside the enclosure to electrodes 917 to achieve the same effect.

[0094] While the invention has been described with reference to particular embodiments, this description is solely for the purpose of illustration and is not to be construed as limiting this scope of the invention claimed below.

[0095] Additional parallel dark non-reflective ridges could be formed on faceplate 302 so as to extend perpendicular to ridges 314.

[0096] Phosphor stripes 313 could be created from thin phosphor films instead of phosphor particles. Light-emissive regions 313 could be implemented with elements other than phosphors (in particle or film form).

5 [0097] A transparent anode that directly adjoins faceplate 302 could be used in place of, or in conjunction with light-reflective layer 315. Such an anode would typically consist of a layer of a transparent electrically conductive material such as indium-tin oxide. Faceplate 302 and, when present, the adjoining transparent anode then constitute a main section of the light-emitting black-matrix structure.

15 Claims

1. A flat panel device (600, 900) comprising:

a faceplate (602, 902);
 a backplate (603, 903, 1203) connected to the faceplate to form a sealed enclosure (601, 901); means (609/612/613, 909/913) for emitting light from the flat panel device;
 a spacer (607/608, 908, 1208, 1218) situated within the enclosure and supporting the backplate and the faceplate against forces acting in a direction toward the enclosure, the spacer having side surfaces (1208a, 1218a) and an end surface (1208b, 1218b) near the backplate, the spacer's side surfaces being treated to inhibit or minimize charge buildup on the spacer's side surfaces such that the spacer has a sheet resistance between 10^9 and 10^{14} ohms/square along the spacer's side surfaces; **characterized in that**
 an edge metallization (906, 1206, 1216) is formed on said end surface along the entire length of said spacer to define an equipotential surface on said end surface along the entire length of said spacer, the edge metallization connecting the spacer to electrically conductive material situated over the backplate.

2. The device according to claim 1, further comprising a coating (904, 1204, 1214) formed over the spacer's side surfaces, the coating being a material having a secondary emission ratio less than 4 and a sheet resistance between 10^9 and 10^{14} ohms/square.

3. The device according to claim 1, further comprising:

a first coating formed over the spacer's side surfaces, the first coating being a material having a sheet resistance between 10^9 and 10^{14} ohms/square; and
 a second coating formed over the first coating, the second coating being a material having a secondary emission ratio less than 4.

4. The device according to claim 1, wherein the spacer's side surfaces are surface-doped with dopant to produce a sheet resistance between 10^9 and 10^{14} ohms/square.
5. The device according to claim 4, wherein the dopant comprises at least one of titanium, iron, manganese, and chromium.
6. The device according to claim 4, further comprising a coating (904, 1204, 1214) formed over the spacer's doped side surfaces, the coating being a material having a secondary emission ratio less than 4.
7. The device according to claim 2 or 6, wherein the coating is selected from the group comprising chromium oxide, copper oxide, carbon, titanium oxide and vanadium oxide.
8. The device according to any of claims 1 - 7, wherein the spacer comprises a generally flat spacer wall (908, 1208, 1218).
9. The device according to any of claims 1 - 7, wherein the spacer comprises a spacer structure (608) through which a plurality of spacer structure holes (614) are formed.
10. The device according to any of claims 1 - 9, further comprising an electrode (917) formed over a surface of the spacer near an interface between the spacer and the conductive material situated over the backplate, the voltage of the electrode being controlled to achieve a desired voltage distribution in the vicinity of the interface.
11. The device according to claim 10, wherein the electrode follows a serpentine path with respect to an interior surface of the backplate.
12. The device according to any of claims 1 - 9, further comprising a plurality of electrodes (917) formed over at least one of the spacer's side surfaces at intervals, the voltage of each electrode being controlled to achieve a desired voltage distribution between the conductive material situated over the backplate and electrically conductive material situated over the faceplate.
13. The device according to claim 12, further comprising a voltage divider (904) that establishes the voltage of each electrode.
14. The device according to claim 13, wherein the voltage divider comprises a resistive coating (904) formed over at least one of the spacer's side surfaces.
15. The device according to any of claims 1 - 14, further comprising second edge metallization (905) situated between a second end surface of the spacer and the faceplate such that the second edge metallization connects the spacer to electrically conductive material situated over the faceplate.
16. The device according to claim 15, further comprising a resistive coating (904, 1204, 1214) formed over the spacer's side surfaces, the first and second edge metallizations being electrically connected to the resistive coating.
17. The flat panel device according to any of claims 1 - 16, further including side walls (604a, 604b) through which the faceplate is connected to the backplate.
18. The device according to any of claims 1 - 17, wherein the means for emitting light comprises:
a field emitter cathode (909); and
light-emissive material (913) situated over the faceplate.
19. The device according to claim 1, wherein the spacer's treated side surfaces comprise a coating (904, 1204, 1214) formed over the spacer's side surfaces, the coating being a material having a secondary emission ratio less than 4 and a sheet resistance between 10^9 and 10^{14} ohms/square.
20. The device according to claim 19, wherein the coating is selected from the group comprising chromium oxide, copper oxide, carbon, titanium oxide and vanadium oxide.
21. A method for assembling a flat panel device (600, 900), the method comprising the steps of:
mounting a spacer (607/608, 908, 1208, 1218) between a backplate (603, 903, 1203) and a faceplate (602, 902);
treating side surfaces (1208a, 1218a) of the spacer to prevent or minimize charge buildup on the spacer's side surfaces such that the spacer has a sheet resistance between 10^9 and 10^{14} ohms/square along the spacer's side surfaces;
defining an equipotential surface on an end surface (1208b, 1218b) of the spacer along the entire length of said spacer, by coating said end surface, along the entire length of said spacer, with edge metallization (906, 1206, 1216) that connects the spacer to electrically conductive material provided over the backplate; and
sealing the backplate and the faceplate together to encase the spacer in an enclosure (601, 901).
22. The method according to claim 21, wherein the step

of treating comprises forming a resistive coating (904, 1204, 1214) over the spacer's side surfaces.

23. The method according to claim 22, wherein the resistive coating has a secondary emission ratio less than 4 and a sheet resistance between 10^9 and 10^{14} ohms/square. 5
24. The method according to claim 21, wherein the step of treating comprises: 10
- forming over the spacer's side surfaces a first coating having a sheet resistance between 10^9 and 10^{14} ohms/square; and
- forming over the first coating a second coating having a secondary emission ratio less than 4. 15
25. The method according to claim 21, wherein the step of treating comprises doping the spacer's side surfaces with dopant to provide the spacer's side surfaces with a sheet resistance between 10^9 and 10^{14} ohms/square. 20
26. The method according to claim 25, wherein the dopant comprises at least one of titanium, iron, manganese, and chromium. 25
27. The method according to claim 25, wherein the step of treating further includes forming over the spacer's doped side surfaces a coating (904, 1204, 1214) having a secondary emission ratio less than 4. 30
28. The method according to any of claims 21 - 27, wherein the spacer comprises a generally flat spacer wall (908, 1208, 1218). 35

Patentansprüche

1. Flachbildschirmeinrichtung (600, 900), die folgendes umfasst: 40
- eine Frontplatte (602, 902);
- eine Rückplatte (603, 903, 1203), die mit der Frontplatte verbunden ist, um eine abgedichtete Umhüllung (601, 901) zu bilden; 45
- ein Mittel (609/612/613, 909/913) zum Emittieren von Licht von der Flachbildschirmeinrichtung;
- einen Abstandshalter (607/608, 908, 1208, 1218), der in der Umhüllung angeordnet ist und die Rückplatte und die Frontplatte gegenüber in einer Richtung auf die Umhüllung zu wirkenden Kräften stützt, wobei der Abstandshalter Seitenflächen (1208a, 1218a) und eine Endfläche (1208b, 1218b) in der Nähe der Rückplatte aufweist, wobei die Seitenflächen des Abstandshalters so behandelt sind, daß der Ladungsauf- 50

bau auf den Seitenflächen des Abstandshalters derart verhindert wird oder minimiert ist, daß der Abstandshalter entlang den Seitenflächen des Abstandshalters einen Flächenwiderstand zwischen 10^9 und 10^{14} Ohm/Quadrat aufweist,

dadurch gekennzeichnet, dass

eine Kantenmetallisierung (906, 1206, 1216) an der Endfläche entlang der gesamten Länge des Abstandshalters ausgebildet ist, welche eine Äquipotentialfläche auf der Endfläche entlang der gesamten Länge des Abstandshalters bildet und die Kantenmetallisierung den Abstandshalter mit über der Rückplatte angeordnetem elektrisch leitendem Material verbindet.

2. Einrichtung nach Anspruch 1, weiterhin mit einer Beschichtung (904, 1204, 1214), die über den Seitenflächen des Abstandshalters ausgebildet ist, wobei die Beschichtung aus einem Material mit einer sekundären Emissionsrate unter 4 und einem Flächenwiderstand zwischen 10^9 und 10^{14} Ohm/Quadrat besteht.
3. Einrichtung nach Anspruch 1, die weiterhin folgendes umfaßt:
- eine erste Beschichtung, die über den Seitenflächen des Abstandshalters ausgebildet ist, wobei die erste Beschichtung aus einem Material mit einem Flächenwiderstand zwischen 10^9 und 10^{14} Ohm/Quadrat besteht; und
- eine zweite Beschichtung, die über der ersten Beschichtung ausgebildet ist, wobei die zweite Beschichtung aus einem Material mit einer sekundären Emissionsrate unter 4 besteht.
4. Einrichtung nach Anspruch 1, wobei die Seitenflächen des Abstandshalters mit einer Dotierungssubstanz oberflächendotiert sind, um einen Flächenwiderstand zwischen 10^9 und 10^{14} Ohm/Quadrat zu erhalten.
5. Einrichtung nach Anspruch 4, wobei die Dotierungssubstanz aus mindestens einem der Stoffe Titan, Eisen, Mangan und Chrom besteht.
6. Einrichtung nach Anspruch 4, weiterhin mit einer Beschichtung (904, 1204, 1214), die über den dotierten Seitenflächen des Abstandshalters ausgebildet ist, wobei die Beschichtung aus einem Material mit einer sekundären Emissionsrate unter 4 besteht.
7. Einrichtung nach Anspruch 2 oder 6, wobei die Beschichtung ausgewählt ist aus der Gruppe bestehend aus Chromoxid, Kupferoxid, Kohlenstoff, Titanoxid und Vanadiumoxid.

8. Einrichtung nach einem der Ansprüche 1-7, wobei der Abstandshalter eine allgemein flache Abstandshalterwand (908, 1208, 1218) umfaßt.
9. Einrichtung nach einem der Ansprüche 1-7, wobei der Abstandshalter eine Abstandshalterstruktur (608) umfaßt, durch die mehrere Abstandshalterstrukturlöcher (614) ausgebildet sind.
10. Einrichtung nach einem der Ansprüche 1-9, weiterhin mit einer Elektrode (917), die über einer Fläche des Abstandshalters nahe einer Grenzfläche zwischen dem Abstandshalter und dem über der Rückplatte angeordneten leitenden Material ausgebildet ist, wobei die Spannung der Elektrode so gesteuert wird, daß in der Nähe der Grenzfläche eine gewünschte Spannungsverteilung erzielt wird.
11. Einrichtung nach Anspruch 10, wobei die Elektrode bezüglich einer Innenfläche der Rückplatte einen schlangenförmigen Weg aufweist.
12. Einrichtung nach einem der Ansprüche 1-9, weiterhin mit mehreren Elektroden (917), die in Abständen über mindestens einer der Seitenflächen des Abstandshalters ausgebildet sind, wobei die Spannung jeder Elektrode so gesteuert wird, daß zwischen dem über der Rückplatte angeordneten leitenden Material und über der Frontplatte angeordnetem, elektrisch leitendem Material eine gewünschte Spannungsverteilung erzielt wird.
13. Einrichtung nach Anspruch 12, weiterhin mit einem Spannungsteiler (904), der die Spannung jeder Elektrode festlegt.
14. Einrichtung nach Anspruch 13, wobei der Spannungsteiler eine Widerstandsbeschichtung (904) umfaßt, die über mindestens einer der Seitenflächen des Abstandshalters ausgebildet ist.
15. Einrichtung nach einem der Ansprüche 1-14, weiterhin mit einer zweiten Kantenmetallisierung (905), die derart zwischen einer zweiten Endfläche des Abstandshalters und der Frontplatte angeordnet ist, daß die zweite Kantenmetallisierung den Abstandshalter mit über der Frontplatte angeordnetem elektrisch leitendem Material verbindet.
16. Einrichtung nach Anspruch 15, weiterhin mit einer Widerstandsbeschichtung (904, 1204, 1214), die über den Seitenflächen des Abstandshalters ausgebildet ist, wobei die erste und zweite Kantenmetallisierung mit der Widerstandsbeschichtung elektrisch verbunden ist.
17. Flachbildschirmeinrichtung nach einem der Ansprüche 1-16, weiterhin mit Seitenwänden (604a, 604b),
- durch die die Frontplatte mit der Rückplatte verbunden ist.
18. Einrichtung nach einem der Ansprüche 1-17, wobei das Mittel zum Emittieren von Licht aus folgendem besteht:
- einer Feldemitterkathode (909); und
einem über der Frontplatte angeordneten lichtemittierenden Material (913).
19. Einrichtung nach Anspruch 1, wobei die behandelten Seitenflächen des Abstandshalters eine Beschichtung (904, 1204, 1214) umfassen, die über den Seitenflächen des Abstandshalters ausgebildet ist, wobei die Beschichtung aus einem Material mit einer sekundären Emissionsrate unter 4 und einem Flächenwiderstand zwischen 10^9 und 10^{14} Ohm/Quadrat besteht.
20. Einrichtung nach Anspruch 19, wobei die Beschichtung ausgewählt ist aus der Gruppe bestehend aus Chromoxid, Kupferoxid, Kohlenstoff, Titanoxid und Vanadiumoxid.
21. Verfahren zur Montage einer Flachbildschirmeinrichtung (600, 900), wobei das Verfahren die folgenden Schritte umfaßt:
- Befestigen eines Abstandshalters (607/608, 908, 1208, 1218) zwischen einer Rückplatte (603, 903, 1203) und einer Frontplatte (602, 902);
Behandeln von Seitenflächen (1208a, 1218a) des Abstandshalters, so daß der Ladungsaufbau auf den Seitenflächen des Abstandshalters derart verhindert wird oder minimiert ist, daß der Abstandshalter entlang den Seitenflächen des Abstandshalters einen Flächenwiderstand zwischen 10^9 und 10^{14} Ohm/Quadrat aufweist;
Definieren einer Equipotentialfläche auf einer Endfläche (1208b, 1218b) des Abstandshalters entlang der gesamten Länge des Abstandshalters durch Beschichten der Endfläche entlang der gesamten Länge des Abstandshalters mit einer Kantenmetallisierung (906, 1206, 1216), die den Abstandshalter mit über der Rückplatte angeordnetem elektrisch leitendem Material verbindet; und
Abdichten der Rückplatte und Frontplatte miteinander, um den Abstandshalter in einer Umhüllung (601, 901) zu ummanteln.
22. Verfahren nach Anspruch 21, bei dem der Behandlungsschritt das Ausbilden einer Widerstandsbeschichtung (904, 1204, 1214) über den Seitenflächen des Abstandshalters umfaßt.

23. Verfahren nach Anspruch 22, bei dem die Widerstandsbeschichtung eine sekundäre Emissionsrate unter 4 und einen Flächenwiderstand zwischen 10^9 und 10^{14} Ohm/Quadrat aufweist.

24. Verfahren nach Anspruch 21, bei dem der Behandlungsschritt folgendes umfaßt:

Ausbilden einer ersten Beschichtung mit einem Flächenwiderstand zwischen 10^9 und 10^{14} Ohm/Quadrat über den Seitenflächen des Abstandshalters; und

Ausbilden einer zweiten Beschichtung mit einer sekundären Emissionsrate unter 4 über der ersten Beschichtung.

25. Verfahren nach Anspruch 21, bei dem bei dem Behandlungsschritt die Seitenflächen des Abstandshalters mit einer Dotierungssubstanz dotiert werden, um den Seitenflächen des Abstandshalters einen Flächenwiderstand zwischen 10^9 und 10^{14} Ohm/Quadrat zu verleihen.

26. Verfahren nach Anspruch 25, wobei die Dotierungssubstanz aus mindestens einem der Stoffe Titan, Eisen, Mangan und Chrom besteht.

27. Verfahren nach Anspruch 25, wobei bei dem Behandlungsschritt weiterhin über den dotierten Seitenflächen des Abstandshalters eine Beschichtung (904, 1204, 1214) mit einer sekundären Emissionsrate unter 4 ausgebildet wird.

28. Verfahren nach einem der Ansprüche 21-27, wobei der Abstandshalter eine allgemein flache Abstandshalterwand (908, 1208, 1218) umfaßt.

Revendications

1. Dispositif à écran plat (600, 900) comprenant :

une plaque frontale (602, 902),
une plaque arrière (603, 903, 1203) accouplée à la plaque frontale pour former un boîtier hermétique (601, 901) ;

des moyens (609/612/613, 909/913) pour émettre une lumière à partir du dispositif à écran plat ;
une entretoise (607/608, 908, 1208, 1218) située à l'intérieur du boîtier et supportant la plaque arrière et la plaque frontale contre des forces appliquées vers le boîtier, l'entretoise ayant des surfaces latérales (1208a, 1218a) et une surface d'extrémité (1208b, 1218b) près de la plaque arrière, les surfaces latérales de l'entretoise étant traitées pour empêcher ou minimiser une accumulation de charge sur les surfaces latérales de l'entretoise de telle sorte que l'en-

tretoise ait une résistance de couche comprise entre 10^9 et 10^{14} ohms/carré le long des surfaces latérales de l'entretoise ;

5 **caractérisé en ce que**

une métallisation de bordure (906, 1206, 1216) est formée sur ladite surface d'extrémité sur l'ensemble de la longueur de ladite entretoise pour définir une surface équipotentielle sur ladite surface d'extrémité sur l'ensemble de la longueur de ladite entretoise, la métallisation de bordure reliant l'entretoise au matériau électriquement conducteur situé au-dessus de la plaque arrière.

10 2. Dispositif selon la revendication 1, comprenant en outre un revêtement (904, 1204, 1214) formé au-dessus des surfaces latérales de l'entretoise, le revêtement étant un matériau ayant un taux d'émission secondaire inférieur à 4 et une résistance de couche comprise entre 10^9 et 10^{14} ohms/carré.

20 3. Dispositif selon la revendication 1, comprenant en outre :

25 un premier revêtement formé au-dessus des surfaces latérales de l'entretoise, le premier revêtement étant un matériau ayant une résistance de couche comprise entre 10^9 et 10^{14} ohms/carré ; et

30 un second revêtement formé au-dessus du premier revêtement, le second revêtement étant un matériau ayant un taux d'émission secondaire inférieur à 4.

35 4. Dispositif selon la revendication 1, dans lequel les surfaces latérales de l'entretoise sont enduites de dopant pour produire une résistance de couche comprise entre 10^9 et 10^{14} ohms/carré.

40 5. Dispositif selon la revendication 4, dans lequel le dopant comprend au moins un parmi le titane, le fer, le manganèse et le chrome.

45 6. Dispositif selon la revendication 4, comprenant en outre un revêtement (904, 1204, 1214) constitué au-dessus des surfaces latérales enduites de l'entretoise, le revêtement étant un matériau ayant un taux d'émission secondaire inférieur à 4.

50 7. Dispositif selon la revendication 2 ou 6, dans lequel le revêtement est sélectionné parmi le groupe comprenant l'oxyde de chrome, l'oxyde de cuivre, le carbone, l'oxyde de titane et l'oxyde de vanadium.

55 8. Dispositif selon l'une quelconque des revendications 1 à 7, dans lequel l'entretoise comprend une paroi d'entretoise généralement plane (908, 1208, 1218).

9. Dispositif selon l'une quelconque des revendications 1 à 7, dans lequel l'entretoise comprend une structure d'entretoise (608) à travers laquelle une pluralité de trous de structure d'entretoise (614) sont formés.
10. Dispositif selon l'une quelconque des revendications 1 à 9, comprenant en outre une électrode (917) formée au-dessus d'une surface de l'entretoise près d'une interface entre l'entretoise et le matériau conducteur situé au-dessus de la plaque arrière, la tension de l'électrode étant contrôlée pour obtenir une répartition de la tension souhaitée à proximité de l'interface.
11. Dispositif selon la revendication 10, dans lequel l'électrode suit une trajectoire en serpentín par rapport à la surface interne de la plaque arrière.
12. Dispositif selon l'une quelconque des revendications 1 à 9, comprenant en outre une pluralité d'électrodes (917) formées au-dessus d'au moins une des surfaces latérales de l'entretoise à équidistance, la tension de chaque électrode étant commandée pour obtenir une répartition de la tension souhaitée entre le matériau conducteur situé au-dessus de la plaque arrière et un matériau conducteur situé au-dessus de la plaque frontale.
13. Dispositif selon la revendication 12, comprenant en outre un diviseur de tension (904) qui établit la tension de chaque électrode.
14. Dispositif selon la revendication 13, dans lequel le diviseur de tension comprend un revêtement résistif (904) formé au-dessus d'au moins une des surfaces latérales de l'entretoise.
15. Dispositif selon l'une quelconque des revendications 1 à 14, comprenant en outre une seconde métallisation de bordure (905) située entre une seconde surface d'extrémité de l'entretoise et la plaque frontale de telle sorte que la seconde métallisation de bordure relie l'entretoise au matériau conducteur situé au-dessus de la plaque frontale.
16. Dispositif selon la revendication 15, comprenant en outre un revêtement résistif (904, 1204, 1214) formé au-dessus des surfaces latérales de l'entretoise, les première et seconde métallisations de bordure étant connectées électriquement au revêtement résistif.
17. Dispositif à écran plat selon l'une quelconque des revendications 1 à 16, comprenant en outre des parois latérales (604a, 604b) par le biais desquelles la plaque frontale est reliée à la plaque arrière.
18. Dispositif selon l'une quelconque des revendications 1 à 17, dans lequel les moyens pour émettre de la lumière comprennent :
- une cathode à émission de champ (909) ; et un matériau électroluminescent (913) situé au-dessus de la plaque frontale.
19. Dispositif selon la revendication 1, dans lequel les surfaces latérales traitées de l'entretoise comprennent un revêtement (904, 1204, 1214) formé au-dessus des surfaces latérales de l'entretoise, le revêtement étant un matériau ayant un taux d'émission secondaire inférieur à 4 et une résistance de couche comprise entre 10^9 et 10^{14} ohms/carré.
20. Dispositif selon la revendication 19, dans lequel le revêtement est sélectionné parmi le groupe comprenant l'oxyde de chrome, l'oxyde de cuivre, le charbon, l'oxyde de titane et l'oxyde de vanadium.
21. Procédé pour assembler un dispositif à écran plat (600, 900), ledit procédé comprenant les étapes consistant à :
- monter une entretoise (607/608, 908, 1208, 1218) entre une plaque arrière (603, 903, 1203) et une plaque frontale (602, 902) ; traiter les surfaces latérales (1208a, 1218a) de l'entretoise pour empêcher ou minimiser l'accumulation de charge sur les surfaces latérales de l'entretoise de telle sorte que l'entretoise ait une résistance de couche comprise entre 10^9 et 10^{14} ohms/carré le long des surfaces latérales de l'entretoise ; définir une surface équipotentielle sur une surface d'extrémité (1208b, 1218b) de l'entretoise en enduisant ladite surface d'extrémité, sur l'ensemble de la longueur de ladite entretoise, avec une métallisation de bordure (906, 1206, 1216) qui relie l'entretoise à un matériau électriquement conducteur situé au-dessus de la plaque arrière ; et sceller la plaque arrière et de la plaque frontale pour enfermer l'entretoise dans un boîtier (601, 901).
22. Procédé selon la revendication 21, dans lequel l'étape de traitement comprend la formation d'un revêtement résistif (904, 1204, 1214) au-dessus des surfaces latérales de l'entretoise.
23. Procédé selon la revendication 22, dans lequel le revêtement résistif a un taux d'émission secondaire inférieur à 4 et une résistance de couche comprise entre 10^9 et 10^{14} ohms/carré.
24. Procédé selon la revendication 21, dans lequel l'étape de traitement comprend :

la formation au-dessus des surfaces latérales de l'entretoise d'un premier revêtement ayant une résistance de couche comprise entre 10^9 et 10^{14} ohms/carré ; et

la formation au-dessus du premier revêtement d'un second revêtement ayant un taux d'émission secondaire inférieur à 4. 5

25. Procédé selon la revendication 21, dans lequel l'étape de traitement comprend le dopage des surfaces latérales de l'entretoise avec du dopant pour donner aux surfaces latérales de l'entretoise une résistance de couche comprise entre 10^9 et 10^{14} ohms/carré. 10

26. Procédé selon la revendication 25, dans lequel le dopant comprend au moins un matériau parmi le titane, le fer, le manganèse et le chrome. 15

27. Procédé selon la revendication 25, dans lequel l'étape de traitement comprend en outre la formation au-dessus des surfaces latérales dopées de l'entretoise d'un revêtement (904, 1204, 1214) ayant un taux d'émission secondaire inférieur à 4. 20

28. Procédé selon l'une quelconque des revendications 21 à 27, dans lequel l'entretoise comprend une paroi d'entretoise généralement plane (908, 1208, 1218). 25

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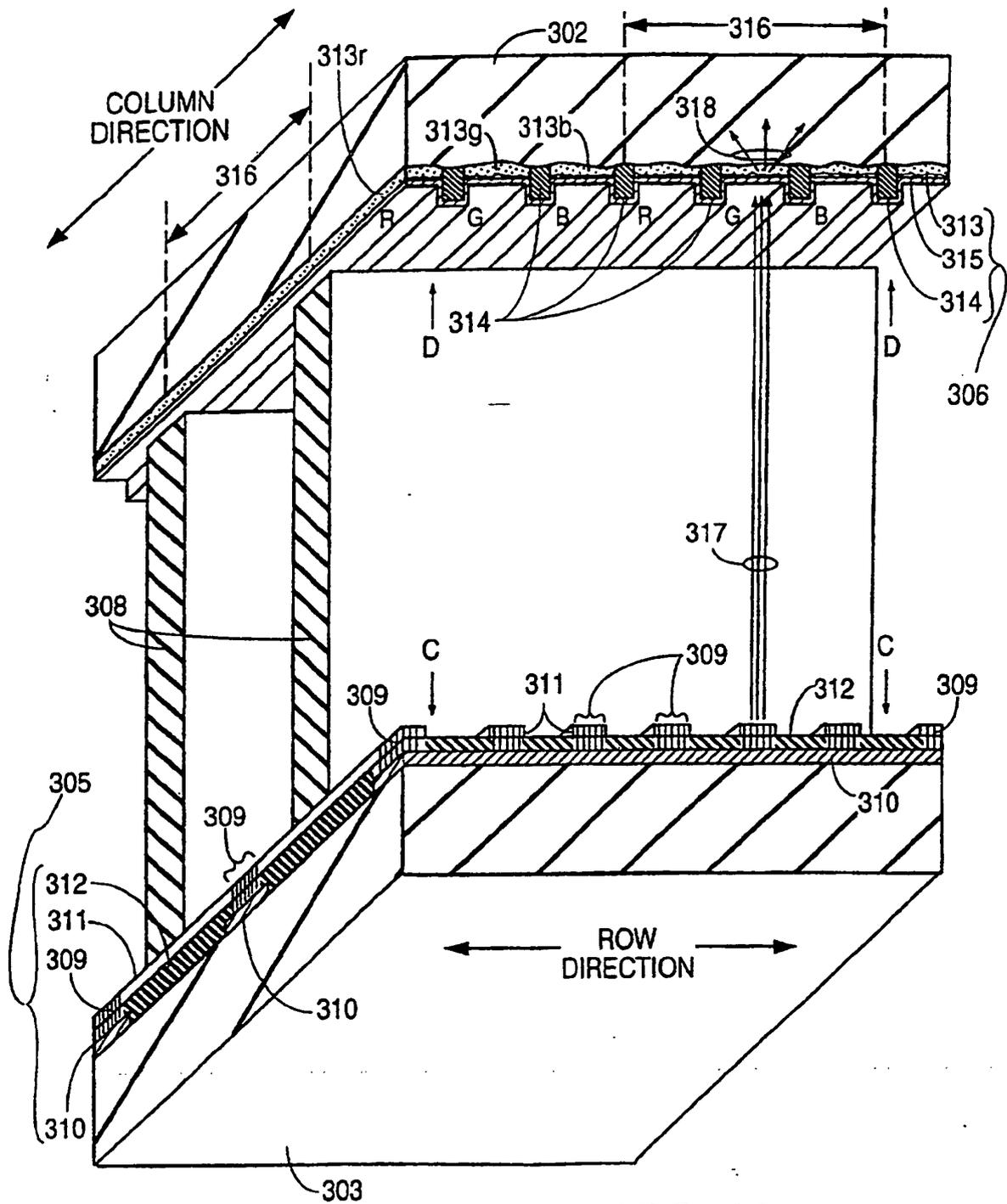
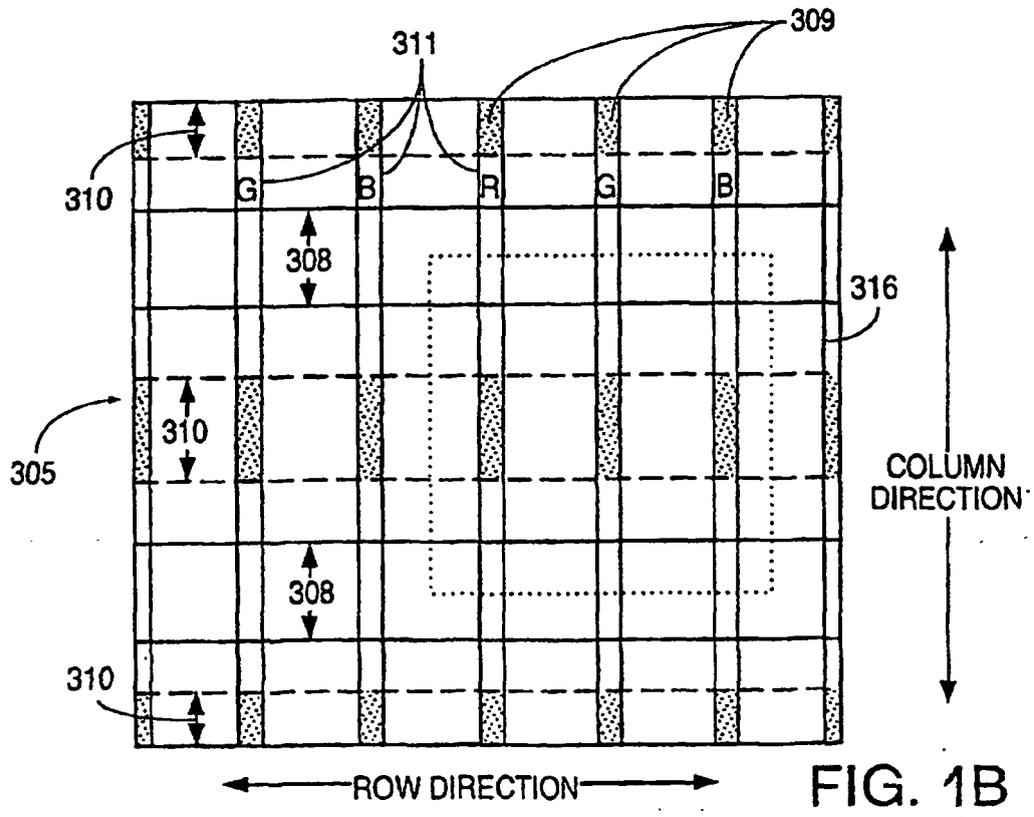
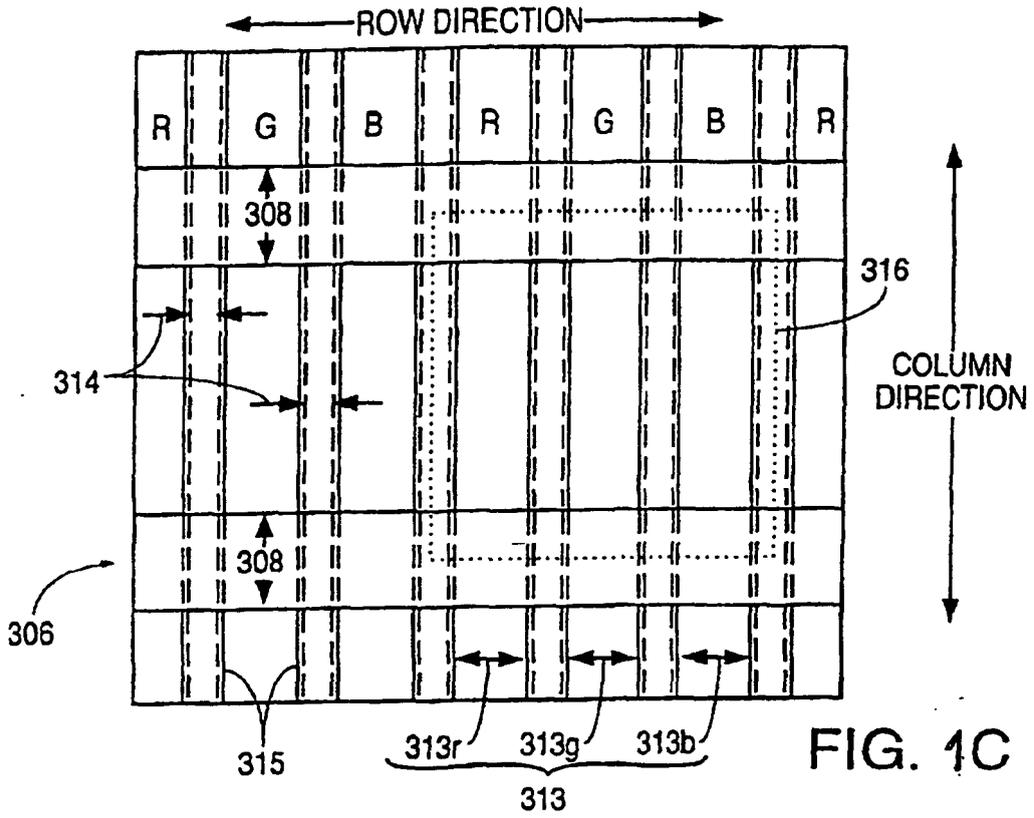


FIG. 1A



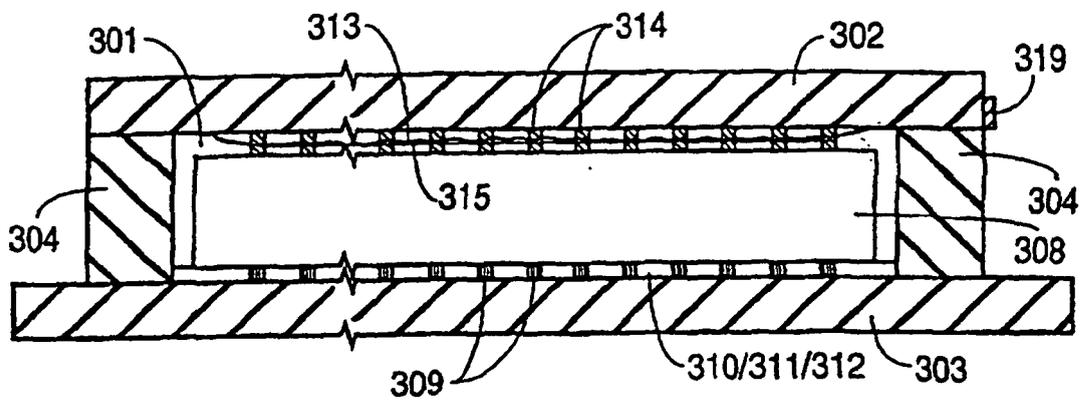


FIG. 1D

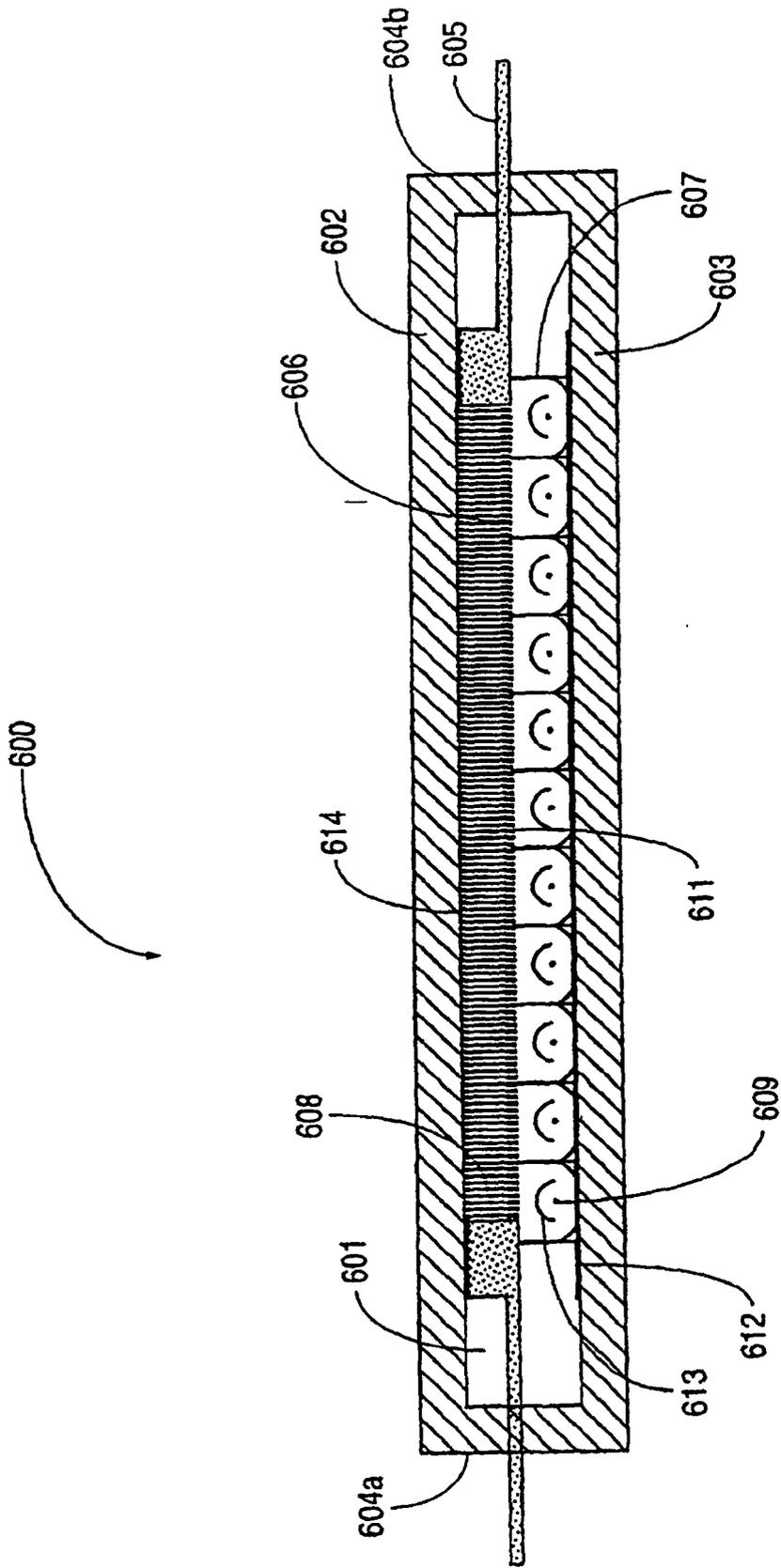


FIG. 2

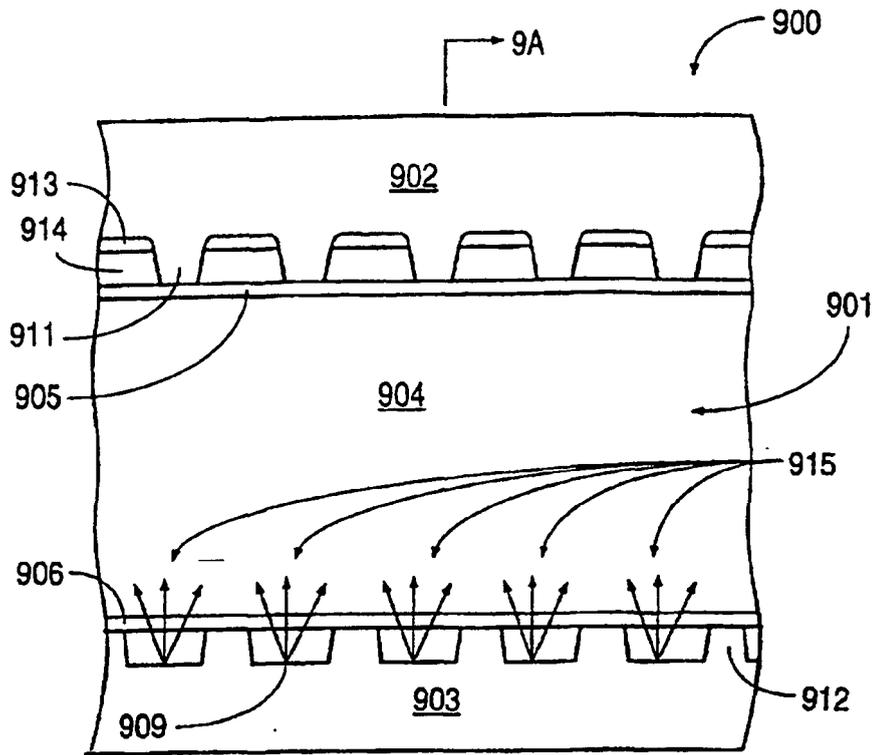


FIG. 3A

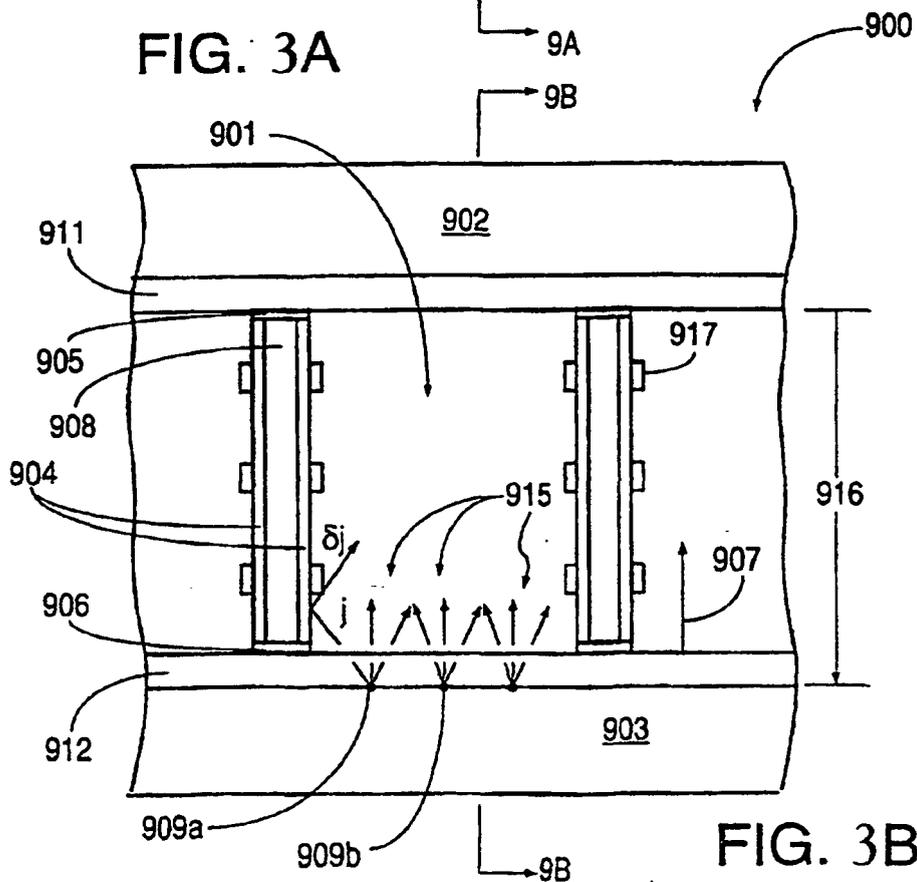


FIG. 3B

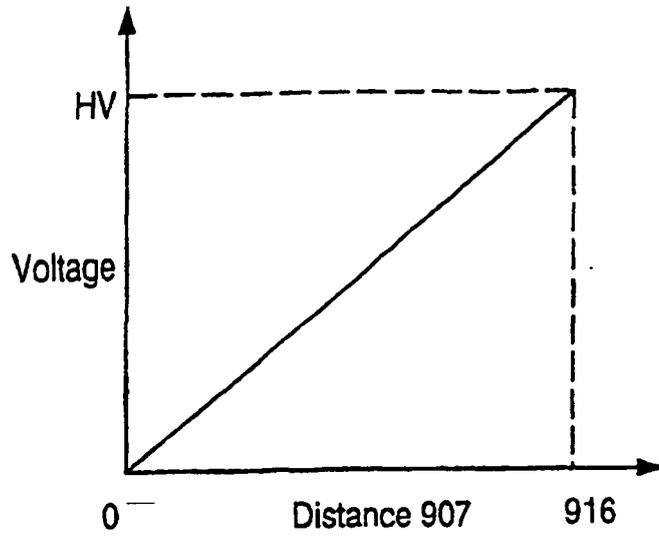


FIG. 4

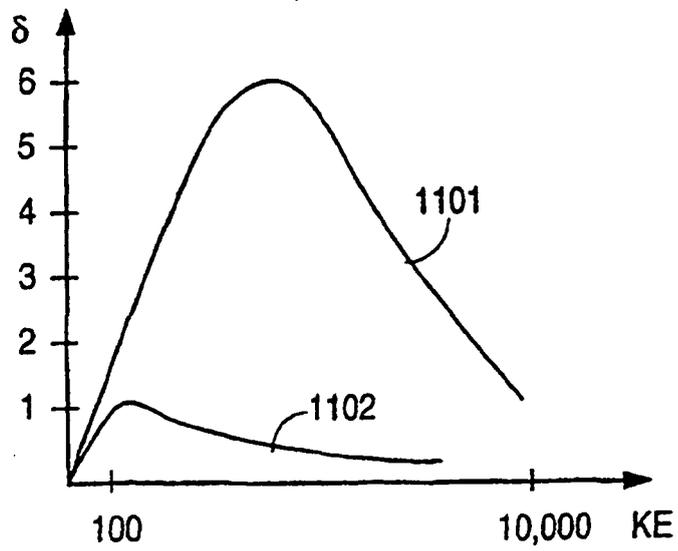


FIG. 5

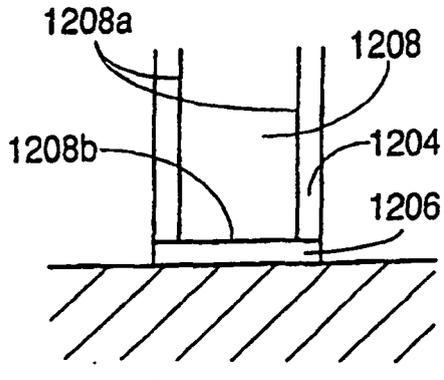


FIG. 6A

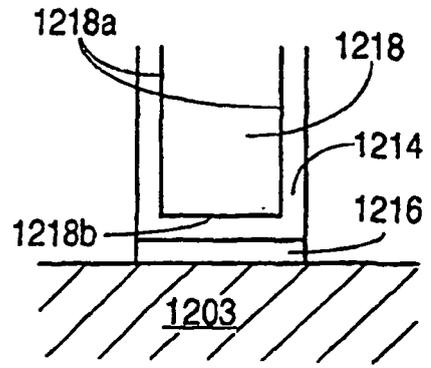


FIG. 6B

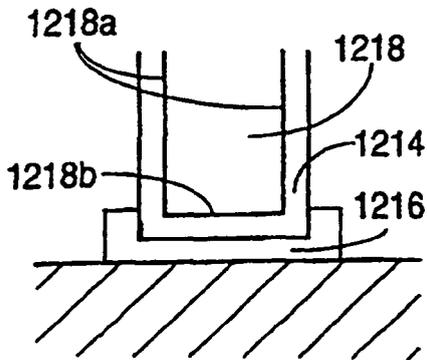


FIG. 6C

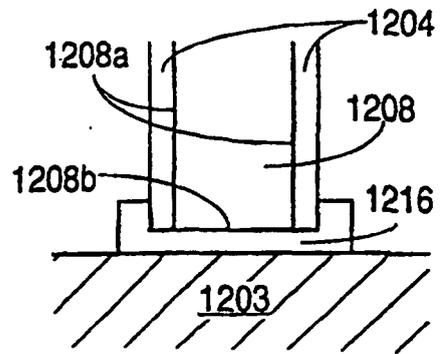


FIG. 6D