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**EP 0 694 899 A1**

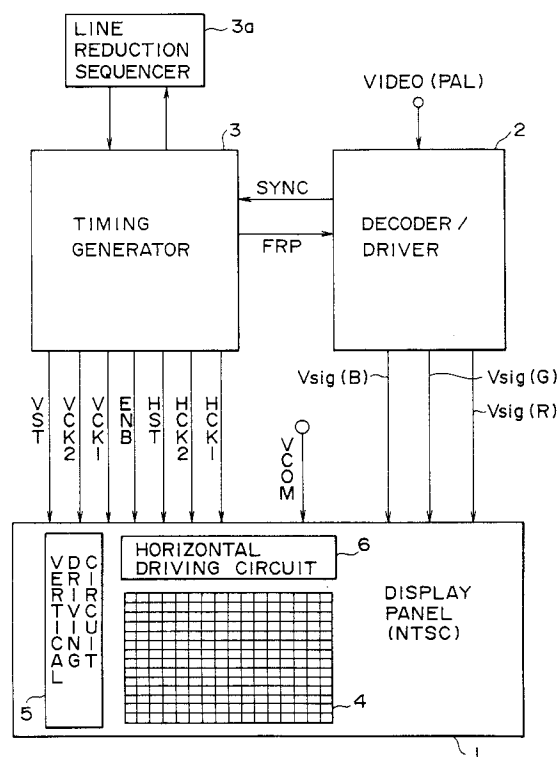
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**DE FR GB**(30) Priority: **22.07.1994 JP 192876/94**(71) Applicant: **SONY CORPORATION**  
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**London WC1R 5LX (GB)**(54) **Display device adapted to display video signals from different video standards**

(57) A display device contrived to improve the quality of a displayed video image by alleviating an undesired phenomenon that the image is seen to be discontinuous in reducing the number of lines of the video signal at a fixed rate. The display device comprises a display panel having a plurality of pixels arranged to form a matrix in conformity with the standard of a normal video signal including a predetermined number of lines per field; a vertical driving circuit for sequentially selecting the pixels of one row; a horizontal driving circuit for writing the video signal in the selected pixels of one row; a signal source for supplying the normal video signal to the display panel and also inputting thereto a second video signal whose number of lines per field is greater than that prescribed in the standard of the normal video signal; and a circuit for controlling the driving of the display panel. This circuit serves to control the timing of the sequential selection by the vertical driving circuit to thereby reduce surplus lines included in the second video signal inputted to the display panel, and further serves to change the positions of the lines to be reduced every field.

**FIG. 1****EP 0 694 899 A1**

## Description

The present invention relates to a display device which comprises a display panel, a decoder/driver for supplying a video signal thereto, and a timing generator for controlling the driving of the display panel. And more particularly, the invention relates to a display device capable of inputting a video signal, which conforms with the PAL standard, to a display panel designed in conformity with, e.g., the NTSC standard.

Japan has adopted the NTSC system, where one frame is composed of 525 lines. Therefore, an active matrix type display panel is usually so constituted as to conform with the NTSC standard, thereby enabling display of a predetermined number of lines per field. However, some other systems have been adopted in foreign countries, such as the PAL standard and the SECAM standard used in Europe. In the PAL system for example, one frame is composed of 625 lines. When a video signal based on the PAL system is inputted to a display panel designed for the NTSC system, it has been necessary heretofore to perform an operation of reducing surplus lines from the video signal of the PAL system at a certain rate, since the number of lines displayable on an active matrix type liquid crystal display panel or the like is fixed.

However, in simple fixed-rate reduction of predetermined lines, the information of the reduced lines is completely lost, so that there arise some problems including conspicuous deterioration of the image quality as, for example, the displayed video image is seen to be discontinuous.

It is therefore an object of the present invention to provide an improved display device where the quality of a displayed image can be enhanced. In this display device, when lines of a video signal are thinned out to be reduced at a predetermined rate in case a video signal of the PAL system for example is inputted to a display panel designed for the NTSC system, different lines are thinned out to be reduced every field to consequently alleviate an undesired phenomenon that the video image is seen to be discontinuous.

According to an aspect of the present invention, there is provided a display device which fundamentally comprises a display panel, a signal source for supplying a video signal thereto, and a timing means for controlling the driving of the display panel. The display panel has a plurality of pixels arranged to form a matrix in conformity with the standard of a first video signal including a predetermined number of lines per field, a vertical driving circuit for sequentially selecting the pixels of one row, and a horizontal driving circuit for writing the video signal of one line in the selected pixels of one row. The signal source is capable of inputting to the display panel a second video signal whose number of lines per field is greater than that of the first video signal. Another characteristic requisite is that the timing means controls the timing of the sequential selection by the vertical driving circuit to reduce surplus lines included in the second video sig-

nal inputted to the display panel, and changes the positions of the lines to be reduced every field.

More specifically, the display panel has a plurality of pixels arranged to form a matrix in conformity with the NTSC standard of a first video signal composed of 525 lines. Meanwhile the signal source inputs to the display panel a second video signal of 625 lines conforming with the PAL standard. In this case, the timing means reduces surplus lines at a rate of one per six or seven lines while changing the positions of the lines to be reduced. For example, the timing means alternately interchanges the positions of the lines reduced in a first field and a second field. The timing means may be so modified as to cyclically shift the positions of the lines reduced in each cycle consisting of three or more fields. It is possible to employ, as the aforementioned display panel, an active matrix liquid crystal display panel which has a plurality of pixels each comprising a pixel electrode, a counter electrode disposed opposite to the pixel electrode with a gap, a liquid crystal held in the gap, and a switching element for driving the pixel electrode.

In the present invention using a display panel where the number of displayed lines is fixed as in an active matrix type liquid crystal display panel or the like, when lines of a video signal are thinned out to be reduced at a predetermined rate in case a video signal of the PAL system for example is inputted to a display panel designed for the NTSC system, different lines are thinned out to be reduced every field to consequently alleviate a phenomenon that the video image is seen to be discontinuous, hence enhancing the quality of the displayed image.

The invention will be further described by way of non-limitative example, with reference to the accompanying drawings, in which:-

Fig. 1 is a block diagram showing the entire constitution of a display device according to the present invention;

Fig. 2 is a typical diagram for explaining the operation of the display device of the invention;

Fig. 3 is another typical diagram for explaining the operation of the display device of the invention;

Fig. 4 is a block diagram showing an exemplary display panel incorporated in the display device of Fig. 1;

Fig. 5 is a circuit diagram for explaining the operation of line reduction;

Fig. 6 is a waveform chart for explaining the operation of line reduction;

Fig. 7 is a timing chart for explaining the operation of line reduction; and

Fig. 8 is a timing chart for explaining the operation of the display device according to the present invention.

Hereinafter a preferred embodiment of the present invention will be described in detail with reference to the accompanying drawings. Fig. 1 is a block diagram showing a basic constitution of the display device according to the present invention. As shown, this display device comprises a display panel 1, a signal source for supplying a video signal thereto, and a timing means for controlling the driving of the display panel 1. A decoder/driver 2 is employed as the signal source, and a combination of a timing generator 3 and a line reduction sequencer 3a is employed as the timing means. The display panel 1 has a plurality of pixels 4, a vertical driving circuit 5 and a horizontal driving circuit 6. The plurality of pixels 4 are arranged to form a matrix in conformity with the standard (e.g., NTSC standard) of a first video signal including a predetermined number of lines per field. The vertical driving circuit 5 sequentially selects the pixels of one row, and the horizontal driving circuit 6 writes a video signal of one line in the selected pixels of one row. The decoder/driver 2 is capable of inputting to the display panel 1 a second video signal whose number of lines per field is greater than that of the first video signal. The timing generator 3 controls the timing of the sequential selection performed by the vertical driving circuit 5 and reduces, at a predetermined rate, surplus lines included in the second video signal inputted to the display panel 1. One of the characteristic requisites of the present invention is such that the line reduction sequencer 3a controls the timing generator 3 in such a manner as to change the positions of the lines to be reduced every field. More specifically, the line reduction sequencer 3a supplies to the timing generator 3 a reduction sequence signal which designates the positions of lines to be reduced every field. And in response to the reduction sequence signal, the timing generator 3 halts the operations of both the vertical driving circuit 5 and the horizontal driving circuit 6 under control to thereby interrupt display of the relevant line.

In this embodiment, the display panel 1 has a plurality of pixels arranged to form a matrix in conformity with the NTSC standard of a first video signal composed of 525 lines. Meanwhile the decoder/driver 2 inputs to the display panel 1 a second video signal of 625 lines conforming with the PAL standard. The timing generator 3 reduces surplus lines at a rate of one per six or seven lines. In this case, the line reduction sequencer 3a supplies a predetermined reduction sequence signal to the timing generator 3 and reduces the surplus lines while changing the positions thereof every field.

Still referring to Fig. 1 continuously, the function of each component in the device will be described below in detail. The display panel 1 is equipped with a screen conforming with the NTSC standard. And a multiplicity of pixels 4 are arranged to form a matrix on this screen. The

display panel 1 performs its ordinary display operation when a video signal of the NTSC standard is inputted thereto, or performs predetermined reduction display driving when a video signal Vsig of the PAL standard is inputted. In this embodiment, the display panel 1 is of full color type and receives a video signal Vsig separated into three primary colors R, G and B. The display panel 1 has a vertical driving circuit 5 to sequentially select the pixels 4 row by row, and also has a horizontal driving circuit 6 to write the video signal Vsig of one line (one horizontal period) in the selected pixels 4 of one row. When a video signal Vsig of the PAL standard is inputted, the vertical driving circuit 5 performs an operation of reducing a predetermined number of surplus lines from the video signal Vsig of the PAL standard under timing control and then displays the signal thus processed.

The decoder/driver 2 has a decoder section to receive a supply voltage of, e.g., 5V and a driver section to receive a supply voltage of 12V. The decoder section decodes a composite video signal VIDEO inputted from an external device and extracts a luminance signal and a chroma signal therefrom while transferring to the timing generator 3 a synchronizing signal SYNC separated from the composite video signal VIDEO. The driver section separates the AC video signal Vsig into R, G and B components and supplies the same to the display panel 1 in response to an inversion signal FRP inputted from the timing generator 3.

On the basis of the synchronizing signal SYNC, the timing generator 3 generates various timing signals and supplies the same to the display panel 1 to control the timing thereof. More specifically, first timing signals (vertical start signal VST, vertical clock signals VCK1 and VCK2) are supplied to the vertical driving circuit 5 to sequentially select pixels row by row. Meanwhile second timing signals (horizontal start signal HST, horizontal clock signals HCK1 and HCK2) are supplied to the horizontal driving circuit 6 to write the video signal Vsig of one line in the selected pixels 4 of one row. And a third timing signal, which is a reduction mask signal ENB, is supplied to the vertical driving circuit 5 so as to be used for line reduction driving. As described above, the line reduction sequencer 3a supplies to the timing generator 3 a reduction sequence signal which designates the positions of lines to be reduced every field. Then, in response to this reduction sequence signal, the timing generator 3 adjusts the timing to apply each timing signal, such as VST, HST or ENB, to the display panel 1. The display panel also receives a reference voltage VCOM applied to the counter electrode.

Fig. 2 is a typical diagram showing an exemplary operation of line reduction performed in the display device of the present invention. In this example, the positions of lines to be reduced are alternately interchanged in a first field and a second field. More specifically, in a first field (odd field), there are reduced 2nd line, 8th line, 14th line and so forth. Thus, the reduction is executed at such a rate that one line is thinned out of six lines. And in a sec-

ond field (even field), there are reduced 5th line, 11th line and so forth.

Fig. 3 typically shows another exemplary operation of line reduction. In this example, the positions of lines to be reduced are cyclically shifted in three or more fields which constitute a unitary cycle. More specifically, the positions of lines to be reduced in a unitary cycle of six fields are shifted cyclically at such a rate that one line is thinned out of six lines. Namely, in a first field are reduced 1st line, 7th line, 13th line and so forth; in a second field are reduced 4th line, 10th line and so forth; in a third field are reduced 2nd line, 8th line, 14th line and so forth; in a fourth field are reduced 5th line, 11th line and so forth; in a fifth field are reduced 3rd line, 9th line and so forth; and in a sixth field are reduced 6th line, 12th line and so forth. Each of such line reduction sequences is designated by a reduction sequence signal outputted from the line reduction sequencer 3a.

Fig. 4 is a block diagram showing a concrete constitution of the display panel included in Fig. 1. As mentioned, the display panel 1 is equipped with a regular screen 11 where a multiplicity of pixels 4 are arranged to form a matrix. In this example, merely a single pixel 4 is shown for the purpose of simplifying the explanation. This pixel 4 is composed of a minute liquid crystal cell LC. A gate line X in a row and a signal line Y in a column are so disposed as to intersect each other, and an individual pixel 4 is provided at the intersection of such two lines. Further a thin-film transistor Tr is also formed integrally to serve as a switching element for on/off driving the pixel. A gate electrode of the thin-film transistor Tr is connected to a corresponding gate line X, while a source electrode thereof is connected to a corresponding signal line Y, and a drain electrode thereof is connected to a pixel electrode disposed at one end of a corresponding liquid crystal cell LC. The other end of the liquid crystal cell LC is connected to a counter electrode, and a desired reference voltage VCOM is applied thereto. Each gate line X is connected to the vertical driving circuit 5. Meanwhile each signal line Y is connected via a horizontal switch HSW to a video line 7 and is supplied with the video signal Vsig. The individual horizontal switch HSW is turned on or off under control of the horizontal driving circuit 6.

The vertical driving circuit 5 operates in accordance with the input signals VST, VCK1 and VCK2 received via a level converter circuit 8. That is, the vertical driving circuit 5 successively transfers vertical start signals VST in response to the vertical clock signals VCK1 and VCK2 of mutually opposite phases to thereby produce gate pulses  $\phi_1, \phi_2, \dots, \phi_N$  in individual stages and then supplies such pulses to the individual gate lines X respectively. And in response to such gate pulses  $\phi$ , the thin-film transistors Tr are switched on or off to sequentially select the pixels 4 of one row.

Meanwhile the horizontal driving circuit 6 operates in accordance with the input signals HST, HCK1 and HCK2 received also via the level converter circuit 8. That

is, the horizontal driving circuit 6 successively transfers horizontal start signals HST in response to the horizontal clock signals HCK1 and HCK2 of mutually opposite phases to thereby produce sampling pulses. The horizontal switch HSW is controlled to be turned on or off in accordance with the sampling pulses, whereby the video signal Vsig supplied via the video line 7 is sampled to each signal line Y. The video signal Vsig thus sampled is written in the liquid crystal pixel 4 via the thin-film transistor Tr placed in its on-state. In this manner, the horizontal driving circuit 6 writes the video signal Vsig of one horizontal period sequentially in the selected pixels 4 of one row. The display panel 1 is further equipped with a gate circuit 9 between the vertical driving circuit 5 and the gate line X. The gate circuit 9 consists of a two-input one-output AND gate element 10 provided in each stage of the gate line X. The output terminal of each AND gate element 10 is connected to the corresponding gate line X. One input terminal of each AND gate element 10 is connected to the corresponding stage of the vertical driving circuit 5, while the other input terminal thereof is supplied with a mask signal ENB via the level converter circuit 8.

Fig. 5 shows an exemplary concrete constitution of the vertical driving circuit 5 included in Fig. 4. As shown, the vertical driving circuit 5 consists of D-type flip flops (DFF) connected in multiple stages. In this diagram, merely two DFF corresponding to an Ath stage and an (A + 1)th stage are shown to facilitate understanding. As mentioned, the vertical driving circuit 5 transfers a vertical start signal to each stage in response to the vertical clock signals VCK1 and VCK2, thereby outputting gate pulses. In this embodiment, a gate circuit 9 is inserted between the vertical driving circuit 5 and the gate line X. As described, the gate circuit 9 consists of an AND gate element 10 disposed in correspondence to each stage. One input terminal of each AND gate element 10 is supplied with a pulse from the corresponding DFF, while the other input terminal thereof is supplied with a mask signal ENB. And the output terminal of each AND gate terminal 10 is connected to the corresponding gate line X.

The operation performed in the constitution of Fig. 5 will now be described below with reference to Fig. 6. When a vertical start signal has been transferred to the Ath-stage DFF, the clock signals VCK1 and VCK2 are temporarily interrupted, and a pulse DA having a duration of two horizontal periods (2H) is outputted from the Ath-stage DFF. And in synchronism therewith, a low-active mask signal ENB is inputted to the AND gate element 10. As a result, the potential of the gate line X corresponding to the Ath stage is changed to the ground level, so that the vertical scanning is brought to a temporal halt during a period of 1H by the above operation. This halt is a line reduction period.

Fig. 7 is a timing chart showing the waveforms of gate pulses outputted successively from the vertical driving circuit 5. As mentioned, the vertical scanning is brought to a temporal halt only during a period of 1H after

output of the gate pulse  $\phi_A$  from the Ath stage, and then line reduction is performed. During this period, the video signal is transferred ineffectively and is therefore not written in any pixel. And after the lapse of such line reduction period, a gate pulse  $\phi_{A+1}$  is outputted from the next stage. Thus, the video signal can be reduced by temporarily halting the vertical scanning at a predetermined rate.

Finally, Fig. 8 is a timing chart of signals showing an operation to write a video signal. First, in order to make the present invention better understood with facility, an explanation will be given on a writing operation with regard to the NTSC standard. In this case, none of line reduction is performed, and ordinary line sequential writing is executed. After the lapse of a predetermined over-scanning period, a vertical start signal VST is inputted to the vertical driving circuit from the timing generator. The vertical start signal VST is sequentially transferred every 1H in synchronism with a vertical clock signal VCK1, whereby the aforementioned gate pulse is outputted. And in synchronism therewith, a horizontal start signal HST is inputted every 1H to the horizontal driving circuit from the timing generator, so that a video signal of one line can be sequentially written in the pixels of one row.

On the other hand, when a video signal conforming with the PAL standard is inputted, line reduction driving is performed in accordance with the present invention. The shown example represents a case where a 4th line is designated to be reduced. After the lapse of a predetermined over-scanning period, a vertical start signal VST is inputted to the vertical driving circuit from the timing generator. The vertical start signal VST is sequentially transferred every 1H in synchronism with a vertical clock signal VCK1, whereby a gate pulse is outputted. And in synchronism therewith, a horizontal start signal HST is inputted every 1H to the horizontal driving circuit from the timing generator, so that 1st to 3rd lines of the video signal are written successively in the pixels of 1st to 3rd rows. Subsequently at the timing of output of a 4th line, the clock signal VCK1 is temporarily interrupted and, in response thereto, the mask signal ENB is turned to a low level only during a period of 1H. Due to the timing control described above, the vertical scanning is brought to a temporal halt, and the 4th line is transferred ineffectively during such a halt. Thereafter the ordinary operation is resumed, and then 5th, 6th, 7th and 8th lines are written successively in the pixels of the corresponding rows. And an inversion signal FRP is synchronized with such line reduction timing, so that accurate 1H inversion driving is rendered possible even after the line reduction.

As described hereinabove, according to the present invention using a display panel where the number of displayed lines is fixed as in an active matrix type liquid crystal display panel or the like, remarkable effects can be attained in improving the displayed image quality in such a manner that, when lines of a video signal are thinned out to be reduced at a predetermined rate in case a video

signal of the PAL system for example is inputted to a display panel designed for the NTSC system, different lines are thinned out to be reduced every field to consequently alleviate an undesired phenomenon that the video image is seen to be discontinuous, hence enhancing the quality of the displayed image.

## Claims

1. A display device comprising:
  - a display panel having a plurality of pixels arranged to form a matrix in conformity with the standard of a first video signal including a predetermined number of lines per field;
  - a vertical driving circuit for sequentially selecting the pixels of one row;
  - a horizontal driving circuit for writing the video signal in the selected pixels of one row;
  - a signal source for supplying the first video signal to said display panel, said signal source capable of inputting to said display panel a second video signal whose number of lines per field is greater than that prescribed in the standard of said first video signal; and
  - a means for controlling the driving of said display panel, said means serving to control the timing of the sequential selection by said vertical driving circuit to thereby reduce surplus lines included in the second video signal inputted to said display panel, and further serving to change the positions of the lines to be reduced every field.
2. The display device according to claim 1, wherein said vertical driving circuit and said horizontal driving circuit are formed integrally in said display panel.
3. The display device according to claim 1 or 2, wherein said display panel has a plurality of pixels arranged in conformity with the standard of a first video signal composed of 525 lines, and said signal source inputs to said display panel a second video signal of 625 lines conforming with a specific standard, and said control means reduces surplus lines at a rate of one per six or seven lines while changing the positions of the lines to be reduced.
4. The display device according to claim 3, wherein the standard of said first video signal is the NTSC standard, and the standard of said second video signal is the PAL or SECAM standard.
5. The display device according to claim 1, 2, 3 or 4, wherein said control means alternately interchanges the positions of the lines reduced in a first field and a second field.
6. The display device according to claim 1, 2, 3 or 4,

wherein said control means cyclically shifts the positions of the lines reduced in each cycle consisting of three or more fields.

7. The display device according to any one of the preceding claims, wherein said display panel is an active matrix liquid crystal display panel which has a plurality of pixels comprising a plurality of pixel electrodes, counter electrodes disposed opposite to said pixel electrodes with a gap, a liquid crystal held in said gap, and switching elements for driving said pixel electrodes.

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FIG. 1

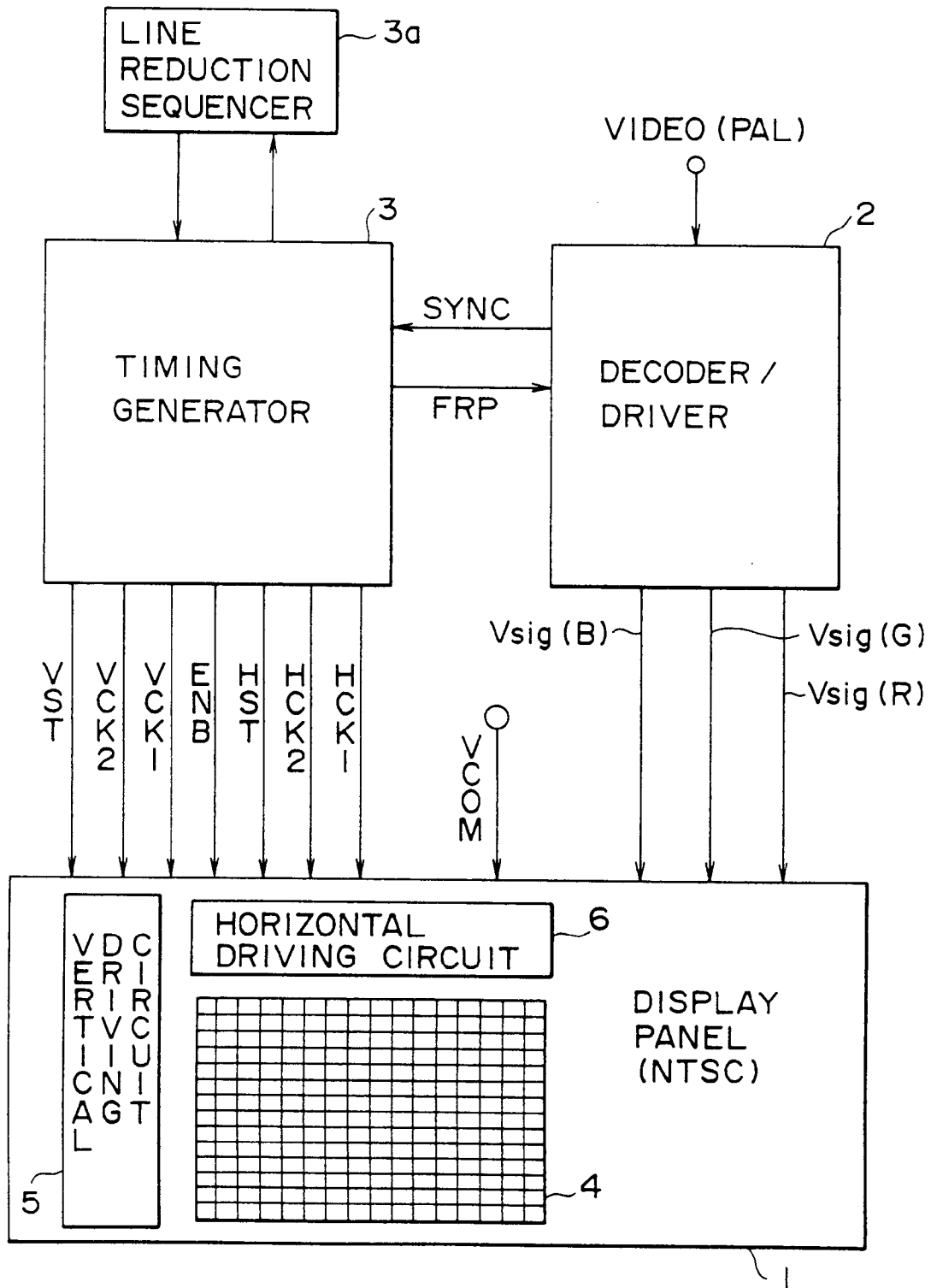


FIG. 2

| LINE | 1ST FIELD | 2ND FIELD |
|------|-----------|-----------|
| 1    |           |           |
| 2    |           |           |
| 3    |           |           |
| 4    |           |           |
| 5    |           |           |
| 6    |           |           |
| 7    |           |           |
| 8    |           |           |
| 9    |           |           |
| 10   |           |           |
| 11   |           |           |
| 12   |           |           |
| 13   |           |           |
| 14   |           |           |

FIG. 3

| LINE | 1ST FIELD | 2ND FIELD | 3RD FIELD | 4TH FIELD | 5TH FIELD | 6TH FIELD |
|------|-----------|-----------|-----------|-----------|-----------|-----------|
| 1    |           |           |           |           |           |           |
| 2    |           |           |           |           |           |           |
| 3    |           |           |           |           |           |           |
| 4    |           |           |           |           |           |           |
| 5    |           |           |           |           |           |           |
| 6    |           |           |           |           |           |           |
| 7    |           |           |           |           |           |           |
| 8    |           |           |           |           |           |           |
| 9    |           |           |           |           |           |           |
| 10   |           |           |           |           |           |           |
| 11   |           |           |           |           |           |           |
| 12   |           |           |           |           |           |           |
| 13   |           |           |           |           |           |           |
| 14   |           |           |           |           |           |           |

FIG. 4

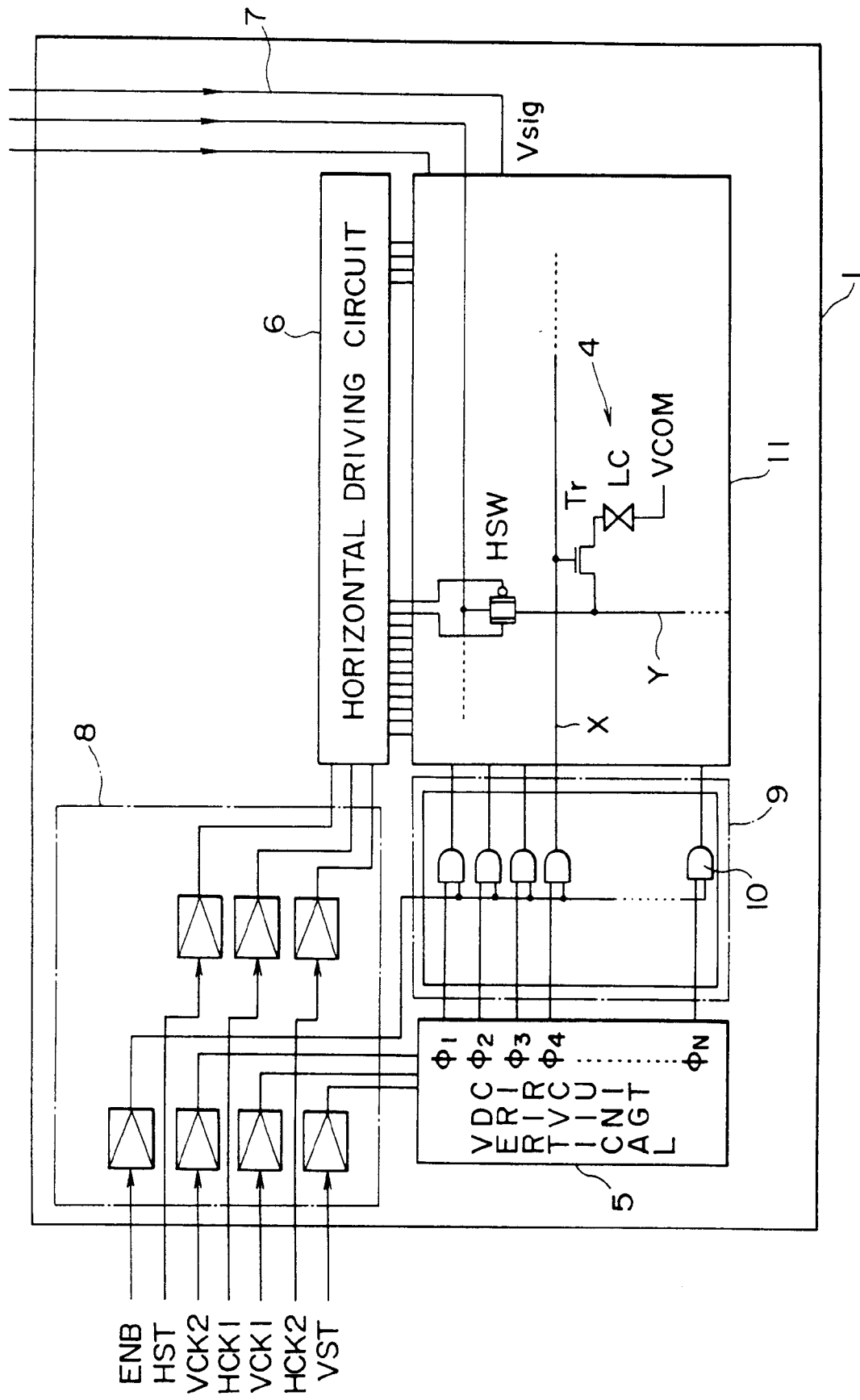


FIG. 5

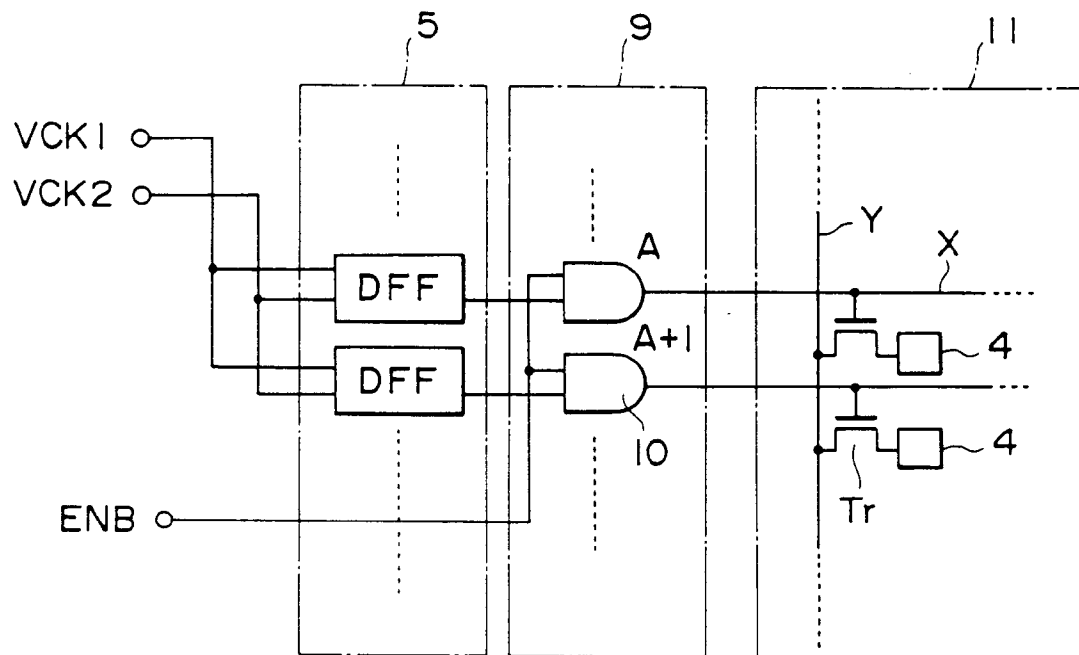


FIG. 6

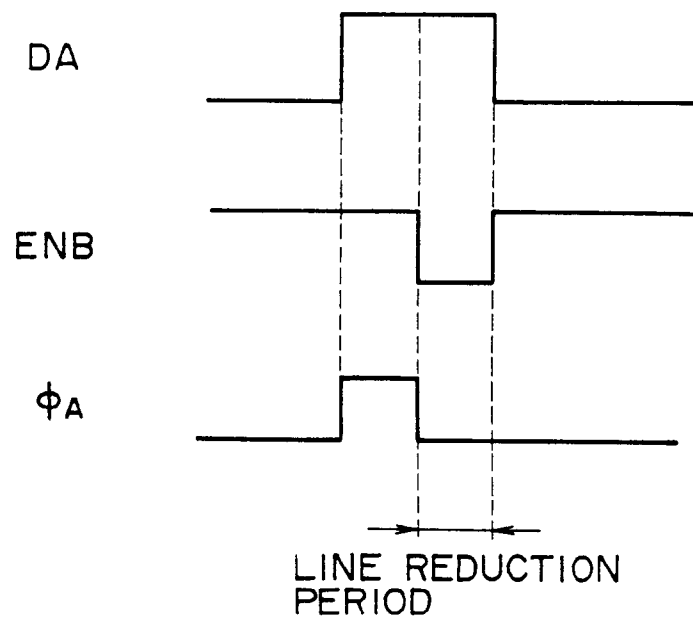


FIG. 7

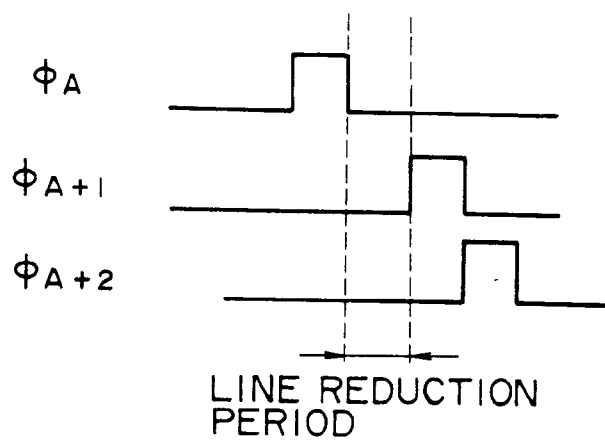
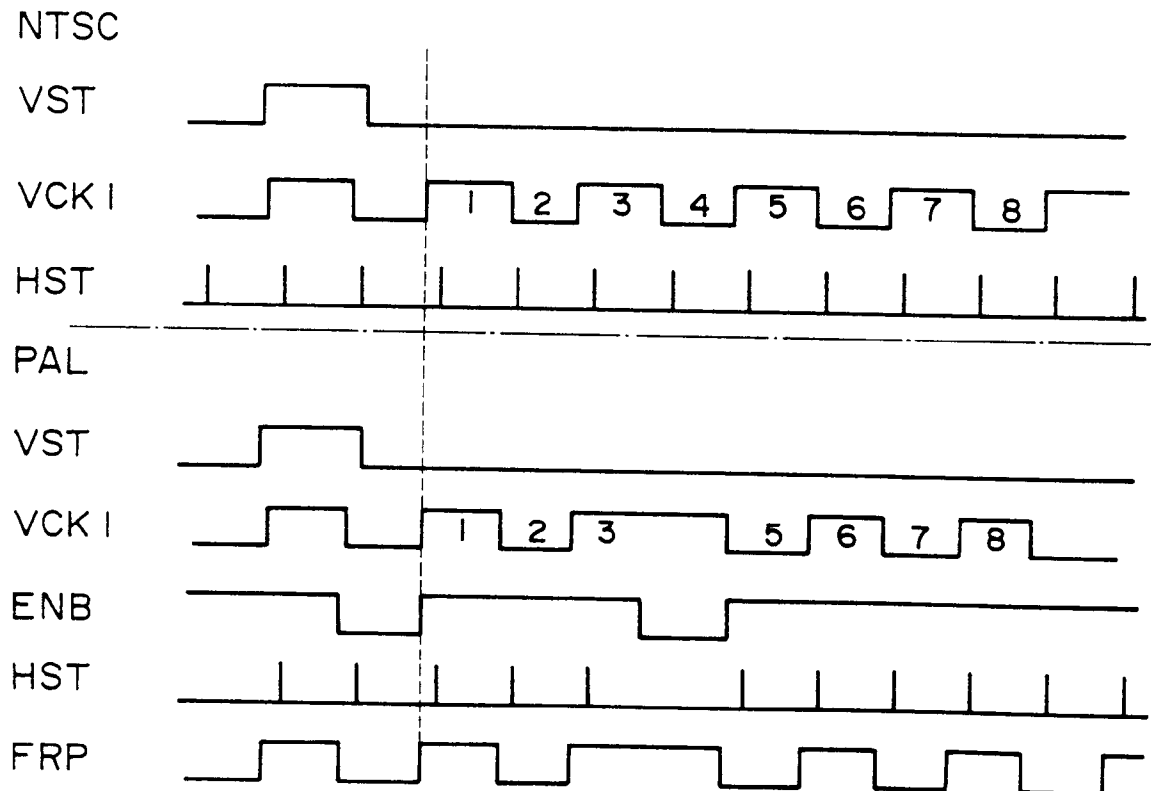


FIG. 8





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# EUROPEAN SEARCH REPORT

Application Number  
EP 95 30 5079

| DOCUMENTS CONSIDERED TO BE RELEVANT                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                                                                                                                                                                                                                                                      |                                                             |                                              |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------|----------------------------------------------|
| Category                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Citation of document with indication, where appropriate, of relevant passages                                                                                                                                                                        | Relevant to claim                                           | CLASSIFICATION OF THE APPLICATION (Int.Cl.6) |
| X<br>Y<br>A                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | EP-A-0 408 347 (SHARP K.K.)<br><br>* column 8, line 20 - column 9, line 11 *<br>* column 11, line 9 - line 21 *<br>* column 14, line 1 - line 48 *<br>* figures 4,7,8 *<br>---                                                                       | 1,3-5,7<br>2<br>6                                           | G09G3/20<br>G09G3/36                         |
| X                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | PATENT ABSTRACTS OF JAPAN<br>vol. 17 no. 331 (E-1386), 23 June 1993<br>& JP-A-05 037909 (SHARP CO.)<br>* abstract *                                                                                                                                  | 1,5                                                         |                                              |
| X                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | DE-A-38 36 558 (BAYERISCHE MOTOREN WERKEN AG)<br>* claims 1,6 *                                                                                                                                                                                      | 1                                                           |                                              |
| Y                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | IEEE JOURNAL OF SOLID-STATE CIRCUITS,<br>vol. 25, no. 2, April 1990 NEW YORK US,<br>pages 531-538, XP 000116698<br>I. DE RYKE ET AL. '2 MHz clocked LCD<br>drivers on glass'<br>* page 531, left column, line 1 - right<br>column, line 5 *<br>----- | 2                                                           |                                              |
| The present search report has been drawn up for all claims                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |                                                                                                                                                                                                                                                      |                                                             |                                              |
| Place of search<br><b>THE HAGUE</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                                                                                                                                                                                                                                                      | Date of completion of the search<br><b>16 November 1995</b> | Examiner<br><b>Farricella, L</b>             |
| <p><b>CATEGORY OF CITED DOCUMENTS</b></p> <p>X : particularly relevant if taken alone<br/>Y : particularly relevant if combined with another document of the same category<br/>A : technological background<br/>O : non-written disclosure<br/>P : intermediate document</p> <p>T : theory or principle underlying the invention<br/>E : earlier patent document, but published on, or after the filing date<br/>D : document cited in the application<br/>L : document cited for other reasons<br/>-----<br/>&amp; : member of the same patent family, corresponding document</p> |                                                                                                                                                                                                                                                      |                                                             |                                              |

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