

(19)



Europäisches Patentamt

European Patent Office

Office européen des brevets



(11)

EP 0 694 932 A1

(12)

EUROPEAN PATENT APPLICATION

(43) Date of publication:
31.01.1996 Bulletin 1996/05

(51) Int. Cl.⁶: H01F 17/00, H01F 27/29

(21) Application number: 95304759.4

(22) Date of filing: 07.07.1995

(84) Designated Contracting States:
AT DE ES FR GB IT

(30) Priority: 29.07.1994 GB 9415316

(71) Applicant: PLESSEY SEMICONDUCTORS
LIMITED
Swindon, Wiltshire SN2 2QW (GB)

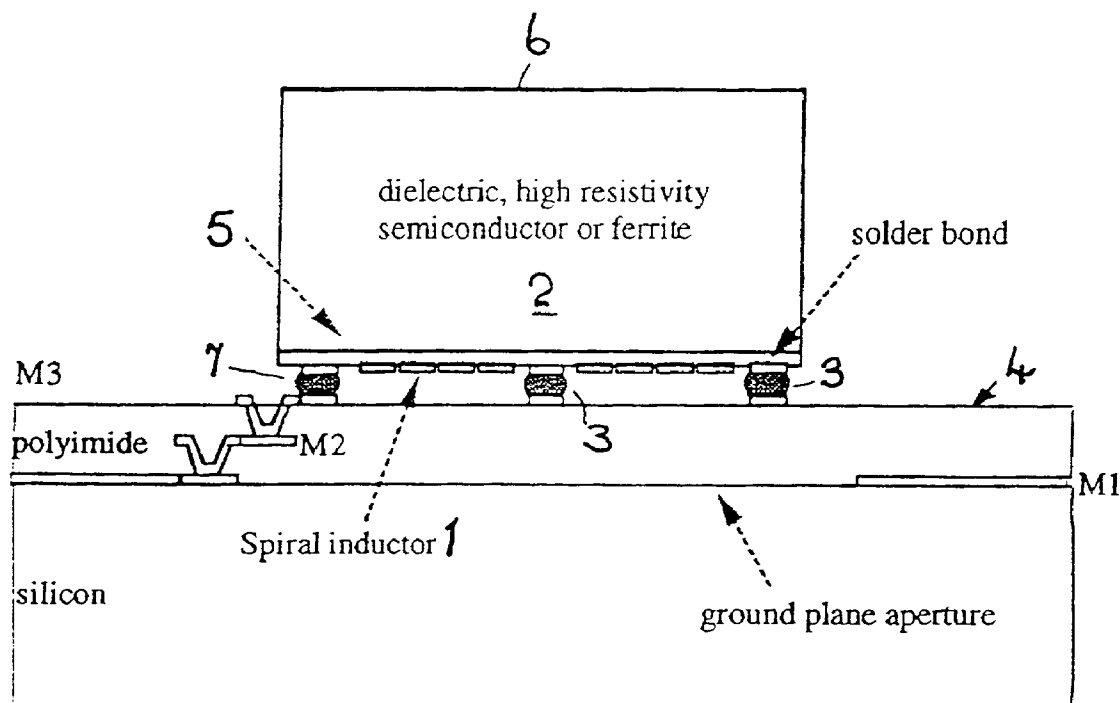
(72) Inventor: Pedder, David John
Long Compton, Warwickshire CV36 5LB (GB)

(74) Representative: Hoste, Colin Francis
Chelmsford, Essex CM1 2QX (GB)

(54) Inductor device

(57) An inductor device for a multichip module, surface-mount or direct-chip attach assembly is formed on a chip or substrate of a dielectric material, high resistivity semiconductor or ferrite as a spiral metallisation, with solder bumps formed on the terminations of the spiral for

connection to corresponding conductors on the underlying surface of the assembly. The use of the flip chip solder bonding technique ensures precise lateral alignment and vertical spacing of the chip with respect to the underlying surface.



EP 0 694 932 A1

Description

There is a growing requirement, in the construction of very compact, low cost radios and other rf communications circuits, for small, high performance and cost effective inductor components.

Surface mountable chip inductors have recently become available that measure 2 by 1.25mm in area (a standard surface mount format), and that offer inductance values up to some 20 nH, with self resonant frequencies of 1 to 2 GHz and quality factors that peak at about 80 at about 0.5 of the self resonant frequency. These inductors are lithographically defined and employ a copper metallisation for low resistance and high quality factor. Such components are available at typical costs of 60 cents each, with costs predicted to fall to 30 cents each as production volumes rise.

Very compact inductors may also be realised in an integrated form within the upper metallisation layers of a multichip module type D (MCM-D) substrate structure. Such inductors can provide inductance values between 1 and 100 nH within a 1mm square footprint (using single or multilayer spiral structures), with self resonant frequencies between 20GHz and 500 Mhz. Quality factor in these MCM-D inductors is determined by the inductor resistance at low frequencies, while the peak quality factor is related to the nature and dielectric structure of the substrate employed. High resistivity silicon substrates with inductors defined in an aluminium-polyimide structure can provide quality factors between about 5 and 20, depending upon the inductor structure and inductance value. The peak quality factor occurs at a frequency between 0.25 and 0.5 of the self resonant frequency. MCM-D inductors on sapphire or other good dielectric substrates can achieve quality factors up to 30, with the peak quality factor occurring at about 0.5 of the self resonant frequency. The effective cost of such inductors is directly related to the cost per unit area of the MCM-D technology, which is currently about 20 cents per square mm and will fall to 5 to 10 cents per square mm as production volumes rise.

Co-pending Patent Application No. 9411107.7 (P/60064) describes the construction of small, accurate discrete inductors that are to be assembled by flip chip solder bonding. These discrete inductors employ a spiral inductor structure defined in a low resistance copper metallisation layer on the upper surface of a small dielectric chip. Metallic vias are included to make connections between the spiral structure on the upper surface and solder bond connections on the lower surface.

Co-pending Patent Application No. 9413145.5 (P/60243) describes the use of a ferrite chip located over a spiral inductor defined in an MCM-D substrate to increase the specific inductance value or the quality factor of the inductor. The ferrite chip is aligned and supported over the inductor by flip chip solder bonding.

According to the present invention an inductor device for mounting on a multichip module, on a direct-chip-attach assembly or on a surface-mount assembly,

comprises a substantially planar electrically insulating substrate, a spiral metallisation structure on a first major face of said substrate defining an inductive element, and a plurality of solder bumps defined on one of the major faces of said substrate for effecting electrical connection of said inductive element to conductors on said module or assembly.

The solder bumps may be defined on said first major face of said substrate.

An inductor device in accordance with the invention will now be described by way of example with reference to the accompanying drawing, which shows the device diagrammatically in cross-section.

Referring to the drawing the inductor device comprises a copper metallisation 1 in a planar spiral format (square, circular or polygonal) defined on the lower surface of a dielectric material, high resistivity semiconductor or ferrite chip 2 about 1mm square. Suitable dielectric materials include polycrystalline or single crystal alumina (sapphire), or fused quartz, while silicon of greater than 2k.ohm cm resistivity is a suitable high resistivity semiconductor material. Ferrite materials may be selected according to the required permittivity and frequency of operation.

The inductor terminations on the lower face of the chip 2 are provided with solder bump connections 3 to allow flip chip solder bond assembly to mating solder bump or other solderable structures on the MCM, direct chip attach or surface mount substrate 4. Additional solder bond connections may be included as required for mechanical support. The use of the flip chip solder bonding technique ensures precise lateral alignment and vertical spacing of the inductor chip 2 from the underlying substrate 4.

Apertures are defined in any power or ground plane structures in the substrate in the area over which the flip chip inductor 1 is mounted in order to minimise any inductance reduction through image inductance effects and any reduction in self resonant frequency from additional capacitive loading.

Single or multilayer inductors may be defined in this inductor structure, the latter providing higher inductance values for the same chip area. The multilayer inductors are constructed using a multilayer metal-polyimide or similar dielectric structure. The uppermost of the planar spiral inductor metallisation layers may also be separated from direct contact with the chip material by a layer of a low dielectric constant material 5 such as an organic polymer. This low permittivity dielectric layer 5 may be employed to minimise the interturn capacitance when high dielectric constant substrate materials, such as ferrites, are employed.

A further metallisation layer 6 may be defined on the upper surface of the inductor chip 2 to allow laser trimming of the inductance of this structure. This layer 6 provides an image inductance that acts to reduce the primary inductance of the spiral inductor 1 on the lower chip face. The level of inductance reduction depends upon the separation of the image plane 6 from the induc-

tor 1 and the permeability of the chip material. The local removal and/or patterning of this exposed and accessible image inductor layer, for example using a laser beam, can then be used to adjust the effective overall inductance of the flip chip inductor device. Suitable patterning structures include concentric square or circular ring patterns and spiral structures. Concentric ring structures provide image eddy currents that can further reduce the effective inductance in step wise manner according to the number, dimensions and location of the rings with respect to the turns of the primary inductor 1. The concentric ring structures may then be cut to interrupt the individual eddy currents to provide a step wise trimming action that increases the inductance. On the other hand, the effective inductance variation resulting from the use of the spiral trimming action is continuous. Trimming of such inductors may be used to tune oscillator, filter or resonator circuits. The upper surface metallisation may be earthed by means of through-chip and substrate vias if required. The separation of the upper metallisation layer from the inductor, the chip to inductor gap determined by the flip chip solder bond height and the relative permittivity of the chip dielectric material will also determine the additional capacitance of this structure and the influence on the inductor self resonant frequency. For this reason low permittivity materials such as fused quartz may be preferred as the chip material.

The inductor structure may be defined on one face of a suitable substrate wafer in the following manner. A thin metallic adhesion layer (for example using a reactive metal system such as chromium, titanium or nichrome) and a plating seed layer (usually a thin copper layer) are sputter deposited onto the surface in succession. These layers may be between 0.05 and 0.5 micrometres in thickness in a typical case. The adhesion layer provides a strong bond to the chip surface. The copper layer provides a comparable surface onto which to plate additional copper. A thick layer of a photoresist material is applied to this face of the wafer and patterned to define a spiral opening structure into which the copper metallisation that forms the inductor itself is then plated. The copper plating should be of the maximum thickness consistent with good control of the plated structure and small spacing between inductor turns (for lowest resistance at a given inductor pitch and hence maximum quality factor). The inductor geometry will be limited by the resolution and feature aspect ratios that can be defined in the resist, together with the properties of the plating solution (throwing power and plating efficiency). Materials exist that can allow at least 25 micrometre copper thicknesses at feature separations of as little as 10 micrometres. This should lead to inductor peak quality factors of at least 100 in inductors of millimetre dimensions. After electroplating the resist mask and the plating seed layer and adhesion layer are stripped by suitable solvent and etchant treatments from all surface areas apart from where the inductors are defined.

Multilayer inductors (for example 2 or 3 layer inductors that give about 4 or 9 fold greater inductance per unit

area than single layer inductors) may be produced as an extension of the single layer inductor structure by plating copper layers separated by a suitable dielectric such as a compatible polyimide. The multilayer structures require the definition of vias through the interlayer dielectric material. These may be produced by a number of techniques, including dry etching. A polyimide material may also be employed to provide a low permittivity layer between the inductor spirals and the chip material.

The completed single or multilayer plated copper inductor structure is then coated with a suitable passivation (for example a layer of silicon nitride) or a metallic, non-solderable barrier layer material (for example chromium or titanium). If a non-conducting passivation layer is employed, then vias are opened in this layer at the locations where input and output connections are required.

An array of solder bump structures are then defined over the inductor input and output points on the patterned inductor spiral and in a number of other locations as required for mechanical location and support.

The solder bump structure requires a solderable metallisation layer to which the solder bump itself is wetted and which defines the area of the solder bump on the surrounding passivation layer or non-solderable barrier metallisation area. Chromium-copper or chromium-copper-gold multilayer metallisation structures are suitable for this solderable metallisation requirement. The first, chromium layer provides adhesion and an ohmic connection to the underlying copper or barrier metallisation surface, while an alloyed chromium-copper layer follows that provides solderability without layer dissolution (for multiple solder bump melting operations). The final copper or copper-plus-gold layers provide initial solderability, these metals dissolving into the solder on bump reflow and reprecipitating on cooling as intermetallic compounds of tin. The gold, if employed, allows the solderable layer to be exposed to the atmosphere without oxidation prior to solder deposition. Solderable metallisation layers of this type may be defined by sequential vapour deposition through an etched metal foil or similar physical masking structure.

The solder itself may be a tin-lead eutectic composition (63Sn-37Pb by wt. - melting point 183 °C) for direct chip attach or surface mount applications, or may be a 95Pb-5Sn composition (melting point 310°C) for MCM-D applications. The solder may be applied by electrodeposition using a seed layer and photoresist masking scheme similar to that described for the plating of the copper inductor structure on the first face of the wafer. Alternatively a physical masking structure may be employed with a vapour deposition process similar to that described for the solderable metallisation deposition. The solder may be deposited as separate layers of lead and tin or as an alloy.

After deposition and patterning of the solderable metallisation and solder layers, the solder bumps are reflowed by heating to above the solder liquidus temperature under inert or reducing atmosphere conditions.

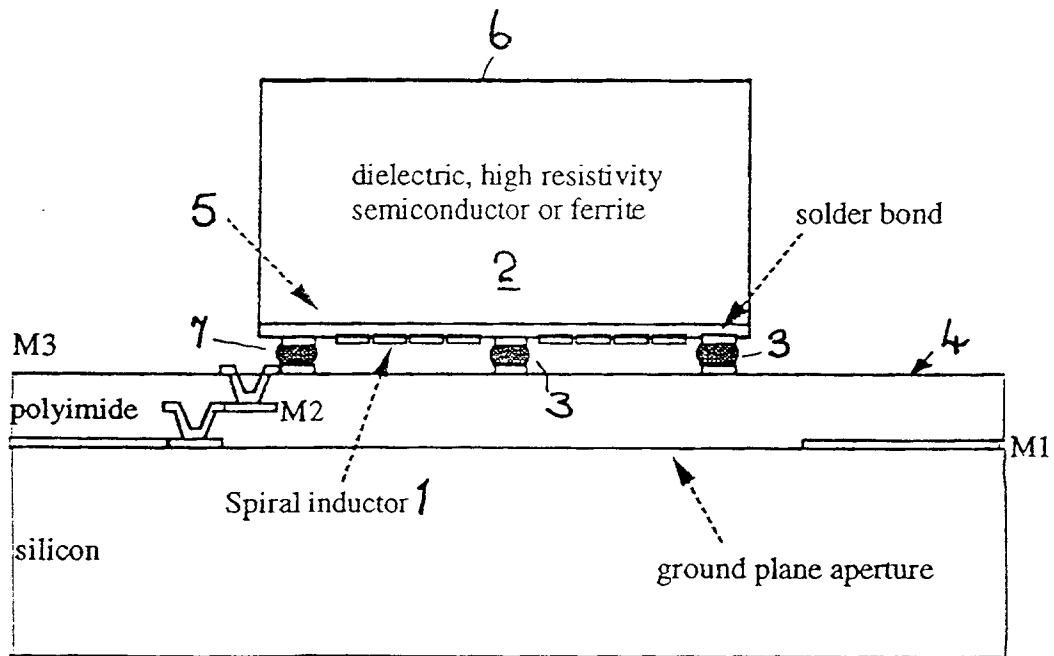
Solder bump diameters between 50 and 125 micrometres are considered appropriate for the flip chip inductor structure. Bump heights between 30 and 100 micrometres are suitable, depending upon the application. Such bump geometries are also typical for flip chip solder bonded ICs for MCM and DCA applications. Solder bumps are defined over the input and output connections to the inductor and also distributed across the chip surface to provide mechanical support for the mounted flip chip inductor. A typical flip chip inductor would employ 5 or 6 solder bumps comprising central and corner or edge bumps 3 for inductor contacts, plus three or four additional corner bumps 7 for mechanical support. A preferred flip chip inductor size would be 0.5, 1.0, 1.15, 1.5 or 2.0 mm on a side, giving some consistency with the trend in discrete surface mount component sizes. A square format may be preferred for inductors for MCM use, whereas a rectangular format would suit direct-chip attach and surface mount applications.

As noted above, a further metallisation layer 6 may be defined on the upper surface of the inductor wafer to allow laser trimming of the diced and mounted inductor structure. This layer 6 may employ a variety of metallisation materials, including, for example, titanium, chromium or aluminium or some combination of such materials. No lithographic or other patterning of this layer is required at the wafer fabrication stage and indeed this layer may be deposited, for example by sputter deposition, prior to the processing of the inductor face. The optical reflectivity and electrical resistivity of this layer will determine the ease of laser trimming and the losses in the inductor image plane.

The use of a photolithographic patterning process to define the inductor geometry enables very accurate inductor dimensions and hence highly reproducible inductor values. The use of copper as the inductor metallisation provides minimal inductor series resistance and hence maximum quality factor.

Claims

1. An inductor device for mounting on a multichip module, on a direct-chip-attach assembly or on a surface mount assembly, comprising a substantially planar electrically insulating substrate, a spiral metallisation structure on a first major face of said substrate defining an inductive element, and a plurality of solder bumps formed on one of the major faces of said substrate for effecting electrical connection of said inductive element to conductors of said module or assembly.
2. An inductor device in accordance with Claim 1 wherein solder bumps are formed on said first major face of said substrate.
3. An inductor device in accordance with Claim 1 or Claim 2 wherein said metallisation structure is separated from the material of said substrate by a layer of low permittivity material.
4. An inductor device in accordance with Claim 1, Claim 2 or Claim 3 wherein a trimmable metallisation layer is formed on the opposite major face of said substrate to said first major face.
5. An inductor device in accordance with Claim 4 wherein said trimmable metallisation layer is patterned in a concentric ring pattern or a spiral pattern.
6. An inductor device in accordance with any preceding claim wherein said metallisation structure is coated with a passivating layer of electrically insulating material.
7. An inductor device in accordance with any one of Claims 1 to 5 wherein said metallisation structure is coated with a non-solderable metallisation layer.
8. An inductor device in accordance with any preceding claim wherein said substrate is of ferrite material.





European Patent
Office

EUROPEAN SEARCH REPORT

Application Number
EP 95 30 4759

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	PATENT ABSTRACTS OF JAPAN vol. 018 no. 442 (E-1593) ,17 August 1994 & JP-A-06 140267 (KYOCERA CORP) 20 May 1994, * abstract * ---	1, 4	H01F17/00 H01F27/29
A	EP-A-0 398 485 (PLESSEY OVERSEAS) 22 November 1990 * abstract * * column 1, line 19 - line 26; figure 4 * ---	1	
A	EP-A-0 551 735 (AVX CORP) 21 July 1993 * column 4, line 16 - line 29; figure 1 * ---	1, 6, 8	
A	PATENT ABSTRACTS OF JAPAN vol. 008 no. 036 (E-227) ,16 February 1984 & JP-A-58 196005 (TOUTSUU:KK) 15 November 1983, * abstract * ---	1, 3, 4	
A	PATENT ABSTRACTS OF JAPAN vol. 012 no. 362 (E-663) ,28 September 1988 & JP-A-63 116410 (FUJIKURA LTD) 20 May 1988, * abstract * -----	1, 4, 5	TECHNICAL FIELDS SEARCHED (Int.Cl.6) H01F
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 18 October 1995	Examiner Marti Almeda, R
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons ----- & : member of the same patent family, corresponding document	

EPO FORM 1503 01.92 (P04C01)