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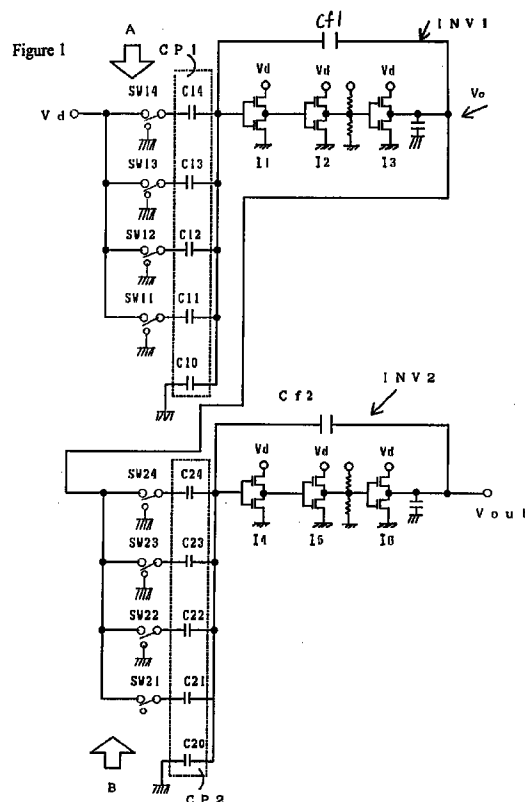
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(54) Multiplication circuit

(57) A multiplication circuit comprising a plurality of weighting circuit serially connected which comprises a plurality of switching means to which a common analog input voltage is inputted, the switching means being controlled by digital signals, a capacitive coupling with a plurality of capacitances each of which is connected to one of the switching means, an amplifier with high open gain to which an output of the amplifier is connected and a feedback capacitance connecting an output of the amplifier to an input.



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Description**Field of the Invention**

5 The present invention relates to a multiplication circuit for generating an analog voltage as a multiplication result for an analog computation.

Background of the Invention

10 The inventors of the present invention have proposed a multiplication circuit in Japanese Application No. Hei 05-020676 and US Patent Application No. 08/181,118. This multiplication circuit, as shown in Figure 2, generates an analog voltage corresponding to a multiplication of a digital multiplier and an analog input voltage by a capacitive coupling. The output of the capacitive coupling is inputted to two stages inverted amplifiers INV1 and INV3, or INV2 and INV3 so that the output is kept stable and accurate. These amplifiers consist of MOS inverters of 3 stages, the outputs of which are
15 connected through a feedback capacitances to their inputs.

The inverted amplifier keeps linearity and stability in the relationship between the input and output by a large open gain of a multiplication gains of MOS inverters of three stages.

This multiplication circuit performs multiplication of digital multiplier and analog data, however it can not execute multiplication of digital data and digital data.

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Summary of the Invention

The present invention is invented so as to solve the conventional problems and has a purposes to provide a multiplication circuit for outputting an analog data as a multiplication result of a multiplication of digital data and digital data.

25 Multiplication circuit according to the present invention performs weighting of an analog input voltage by capacitive couplings of two stages or more. The capacitive coupling is controlled in weight according to the digital data to be multiplied.

According to the present invention, a digital data is multiplied by a digital data and the calculation result is outputted as an analog data which can be used in another analog calculation or other usages.

30 Detailed Description of the Drawings

Figure 1 is a circuit diagram of the first embodiment of a multiplication circuit according to the present invention, and Figure 2 is a circuit diagram showing a multiplication circuit to be compared with the present invention.

35 Preferred Embodiment of the Present Invention

Hereinafter an embodiment of the present invention is described with referring to the attached drawings.

In Figure 1, a multiplication circuit has a plurality of the first switching circuits SW11, SW12, SW13 and SW14 which are connected to capacitances C11, C12, C13 and C14, respectively, of a capacitive coupling CP1. The capacitive
40 coupling has further capacitance C10 grounded.

An output of capacitive coupling CP1 is inputted to an inverting amplifier INV1 consisting of MOS inverters 11, 12 and 13 of 3 stages, and an output of inverting amplifier INV1 is connected to its input through feedback capacitance Cf1. INV1 keeps a linearity and stability between the input and output by a large gain as multiplication of triple gain of MOS inverters.

45 Switching means SW11, SW12, SW13 and SW14 are switches of two inputs and one output for alternatively connecting a common analog input voltage Vd or the ground to the capacitances C11, C12, C13 and C14. Switching means SW11, SW12, SW13 and SW14 are controlled by digital signal A with 4 bits. When ai (i = 1 to 4) is "1", then Cli is connected to Vd and when ai is "0", then Cli is grounded, when each bit of signal A is designated as a1, a2, a3 and a4. When output of INV1 is Vo, then formula 1 is defined.

50

Formula 1

$$Vo = -Vd \sum_{i=1}^4 ai \cdot C1i / Cf1 \quad (1)$$

55 Switching means SW21, SW22, SW23 and SW24 are switches of two inputs and one output and are controlled by digital signal B of 4 bits. When each bit of signal B is designated as b1, b2, b3 and b4, Vo is connected when bi is "1" and the ground is connected when bi is "0". An output Vout of INV2 is defined as in formula 2.

Formula 2

$$V_{out} = -V_o \sum_{i=1}^4 b_i \cdot C2_i / Cf2 \quad (2)$$

Formula 3 is obtained when formula 1 is taken in formula 2.

Formula 3

$$V_{out} = V_d \left\{ \left(\sum_{i=1}^4 a_i \cdot C1_i \right) \left(\sum_{i=1}^4 b_i \cdot C2_i \right) \right\} / (Cf1 \cdot Cf2) \quad (3)$$

When formula 4 is defined, then formula 5 is obtained.

Formula 4

$$C1_i = 2^{i-1}, C2_i = 2^{i-1}, Cf1 = Cf2 = 16, C10 = 1, C20 = 1 \quad (4)$$

Formula 5

$$V_{out} = V_d (A/16) (B/16) \quad (5)$$

By enlarging a circuit size of capacitive couplings CP1 and CP2, multiplication of large digital data is possible. By increasing number of stages of inverting amplifiers, a multi-steps multiplications of digital variables is realized. According to the inventor's experience, enough linearity characteristic can be obtained by inverters of three stages. In order to minimize the circuit of sufficient performances, the inverting amplifier type multiplication is preferable.

Multiplication circuit according to the present invention performs weighting of an analog input voltage by capacitive couplings of two stages or more and the capacitive coupling is controlled in weight according to the digital data to be multiplied, so that it can provide a multiplication circuit for outputting an analog data as a multiplication result of a multiplication of digital data and digital data.

Claims

1. A multiplication circuit comprising a plurality of weighting circuit serially connected which comprises,

- i) a plurality of switching means to which a common analog input voltage is inputted, said switching means being controlled by digital signals;
- ii) a capacitive coupling with a plurality of capacitances each of which is connected to one of said switching means;
- iii) an amplifier with high open gain to which an output of said amplifier is connected; and
- iv) a feedback capacitance connecting an output of said amplifier to an input.

2. A multiplication circuit comprising;

- i) the plurality of the first switching means to which a common analog input voltage is inputted,
- ii) the first capacitive coupling having a plurality of capacitances each of which is connected to one of said first switching means;
- iii) the first inverting amplifier connected to an output of said first capacitance, said first inverting amplifier comprising MOS inverters of stages of odd number;
- iv) the first feedback capacitance for connecting an output of said inverting amplifier to an its input;
- v) a plurality of the second switching means connected to an output of said inverting amplifier;
- vi) the second capacitive coupling connected to an output of said second switching means;
- vii) the second inverting amplifier connected an output of said second capacitive coupling, said second inverting amplifier comprising MOS inverters of stages of odd number;
- viii) the second feedback capacitance for connecting an output of said second inverting amplifier to its input; and
- ix) said second inverting amplifier serially connects an odd number of MOS inverters.

Figure 1

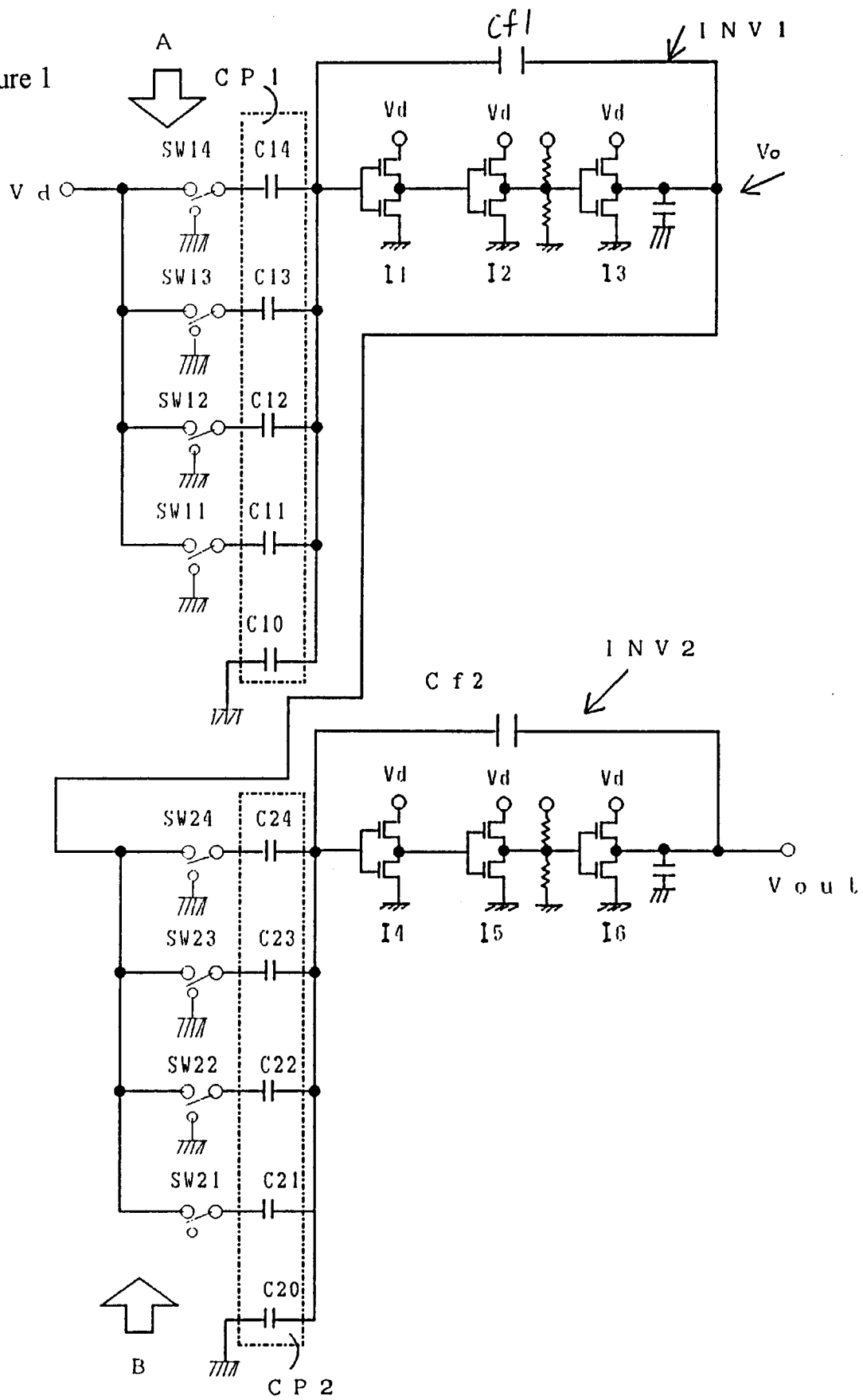
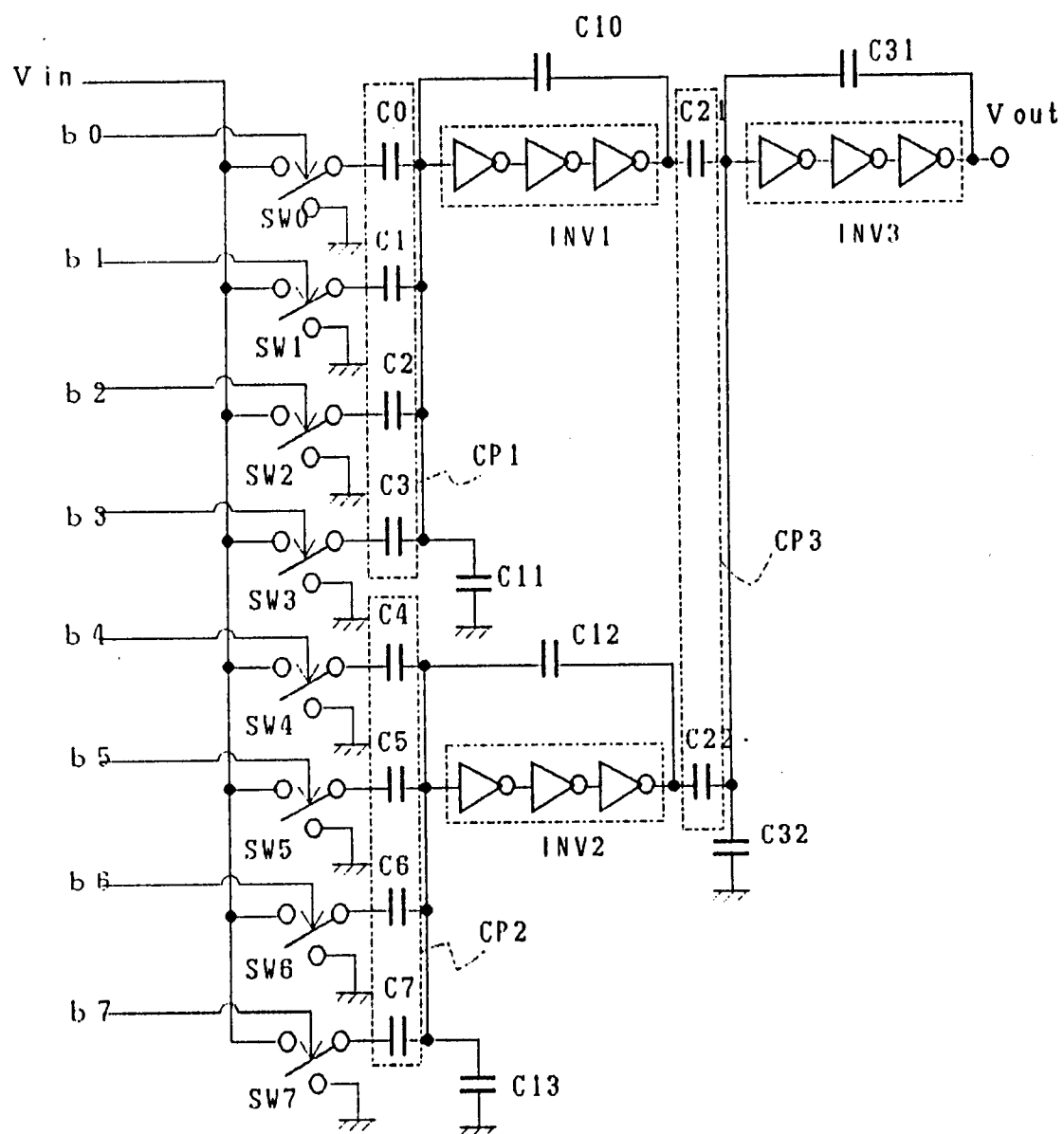


Figure 2





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EUROPEAN SEARCH REPORT

Application Number
EP 95 11 4823

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
P,D, A	US-A-5 361 219 (SHOU ET AL) * column 1, line 53 - column 3, line 14; figure 1 * ---	1	G06J1/00
A	US-A-4 654 815 (MARIN) * column 2, line 40 - column 3, line 12; figure 2 * -----	1	
			TECHNICAL FIELDS SEARCHED (Int.Cl.6)
			G06J
The present search report has been drawn up for all claims			
Place of search		Date of completion of the search	Examiner
THE HAGUE		1 February 1996	GUIVOL, Y
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document			

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