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(54) **High precision current mirror for low voltage supply**

Hochgenauer Stromspiegel für niedrige Versorgungsspannung

Miroir de courant de haute précision pour alimentation à basse tension

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Description

Field of the Invention

[0001] This invention relates to a high-precision current generating circuit.

[0002] The invention particularly concerns a high-precision current generating circuit for a low-impedance circuit user outlet, being of the type which comprises a current mirror having an input branch which is applied a reference current and an output branch which supplies a proportional current to the reference current.

[0003] As is well known, a current mirror configuration is a conventional circuit arrangement which is normally employed to generate a constant output current proportional to a given reference current.

[0004] Current mirrors have many applications in the field of integrated circuits, and are used in particular for biasing differential circuits in oscillator circuits, sample-and-hold circuits, and digital-to-analog converters.

[0005] In certain of these applications, such as high-resolution digital-to-analog converter circuits, it is highly important that the current from the generator be precise, constant over time, and unaffected by possible variations in load draw or variations in supply voltage.

Background Art

[0006] Current mirror generator circuits of conventional design are described in P. R. Gray and R. G. Meyer "Analysis and Design of Analog Integrated Circuits", Wiley, New York, 1984, pages 233-246 and 703-718.

[0007] Such circuits can be implemented, in general, either using transistors of the bipolar type or transistors of the MOS type.

[0008] In its simplest form, the current mirror described in the above-mentioned book comprises two transistors and a reference current generator. In its simplest form, the reference generator comprises a resistor connected in series with one of the two transistors.

[0009] This prior approach is quite straightforward circuit-wise, and is widely used with circuits which do not require high precision.

[0010] The relatively low precision of such a circuit can be explained in relation to its implementation with transistors of the MOS type. The output current from the generator is supplied by one of the two MOS transistors comprising the mirror, and as is well recognized, the internal resistance of a MOS transistor varies with the difference in potential between its drain and source terminals. Since the drain terminal of the transistor, which outputs the current, is usually connected to a load whose impedance may not be always constant, the voltage V_{ds} between the drain and the source of the transistor may also vary during the normal operation of the circuit. This variation in voltage results in a variation in the internal resistance of the transistor, and consequently in the output current from the circuit.

[0011] Other circuit designs have been developed in order to provide current generators with enhanced precision.

[0012] One of these designs, known from the pertinent literature as a "cascode" current mirror configuration and described in the aforementioned book, enables the output resistance of the current generator to be increased so as to reduce the error due to any variations in the supply voltage. This prior approach, while representing an advance from the standpoint of precision, still has some shortcomings. Its particular cascode structure, for instance, reduces the useful dynamic range for the signal, making the circuit unsuited to low supply voltage applications, e.g. in the 2.5 to 3 volts range.

[0013] A further prior approach, also described in the aforementioned book, is the Wilson configuration of the current generating circuit. This is an improvement over the former arrangement as far as precision is concerned, but is again beset with the same drawbacks as the former approach in that it retains the cascode configuration. Also, this approach disallows the biasing of plural output branches on the basis of a single reference current and cannot provide plural output currents.

[0014] EP 0 523 266 relates to an integrable current mirror circuit having a reference transistor in which flows the input current, and an output transistor, in which flows an output current proportional to the input current. Such a circuit comprises an operational amplifier comparing the voltage across the input and output transistors and providing a control voltage to the gate terminals of the transistors, in order to maintain equal voltage values at said terminals.

[0015] Moreover, EP 0 403 195 relates to a current mirror circuit comprising an actively controllable feedback element (in the form of a P-channel MOS transistor), connected to the output of a differential amplifier, whose purpose is to equalise the drain voltages of a pair of MOS transistors.

[0016] The underlying technical problem of this invention is to provide a current generating circuit which has such high-precision functional features, and constructional features of reduced silicon area occupation in the integrated circuit, as to overcome the aforementioned drawbacks besetting the prior art.

[0017] This technical problem is solved by a high-precision current generating circuit of the type which comprises a transistor current mirror as defined in Claim 1.

[0018] The features of this invention will be apparent from the following detailed description of embodiments thereof, with reference to the accompanying illustrative drawings, in which:

Figure 1 is a diagram showing schematically a current generating circuit according to this invention;

Figure 2 shows a first implementation of the current generating circuit of this invention;

Figure 3 is a detailed diagram showing a preferred embodiment of the current generating circuit in Figure 1;

Figure 4 shows a second implementation of the current generating circuit according to the invention;

Figure 5 shows a third implementation of the current generating circuit according to the invention; and

Figure 6 illustrates an exemplary application of the current generating circuit according to the invention.

Detailed Description

[0019] With reference in particular to the example of Figure 1, generally and schematically shown at 1 is a high-precision current generating circuit which embodies this invention.

[0020] The circuit 1 is a current mirror configuration, and comprises two transistors M1 and M2 of the N-channel MOS type. The first transistor M1 forms substantially the input branch 2 of the current mirror and has its source terminal S1 connected to a fixed potential reference, specifically the electric ground GND of the circuit. The drain terminal D1 of the transistor M1 is connected to a reference current Iref generator.

[0021] The output branch 3 of the current mirror comprises the second transistor M2. The source terminal S2 of the transistor M2 is connected to the circuit electric ground GND, its drain terminal D2 being the output terminal of the circuit.

[0022] The control terminals G1 and G2 of both transistors M1 and M2 are connected together.

[0023] Advantageously, a voltage regulator 4 is connected to the drain terminals D1 and D2 of the transistors M1 and M2 to maintain at said terminals a drain-source voltage value, Vds1 and Vds2, which is the same for both transistors.

[0024] The voltage regulator 4 comprises an operational amplifier OA having two inputs, one of the inverting (-) type and another of the non-inverting (+) type, and an output U.

[0025] The non-inverting (+) input of the amplifier OA is connected to the drain terminal D1 of the first transistor M1. The inverting (-) input is connected to the drain terminal D2 of the second transistor M2, and the output U is connected to the common node A between the gate terminals G1 and G2 of both transistors M1, M2.

[0026] A compensation capacitor C1 is connected between the output U and the non-inverting (+) input of the operational amplifier.

[0027] As regards the operation of the circuit in Figure 1, the reference current Iref being flowed through the first transistor M1 is mirrored into the current Iout from the second transistor M2. In fact, the two transistors have their source terminals S1 and S2, and gate terminals

G1 and G2, connected together.

[0028] The provision of the voltage regulator 4, consisting of the operational amplifier OA, implies that the drain-source voltages Vds1 and Vds2 should be the same value for both transistors M1 and M2. Accordingly, since the transistors M1 and M2 also have the same gate-source voltage, they will be operating in exactly the same condition.

[0029] The bias voltage of the two transistors M1 and M2 is supplied from the output U of the operational amplifier OA.

[0030] The two feedback branches existing between the output U of the operational amplifier OA and the two (+) and (-) inputs will now be discussed. These two branches are formed essentially by the two transistors M1 and M2.

[0031] In particular, the output terminal U of the amplifier OA is connected to the gate terminal G1 of the transistor M1, and the drain terminal D1 of this transistor is connected to the non-inverting (+) input of the amplifier OA.

[0032] With the signal present on the drain terminal of a transistor always being shifted 180 degrees from the signal present on the gate terminal thereof, the feedback loop on this branch is bound to be a negative one. The capacitor C1, also feedback connected between the output U and the non-inverting (+) input of the amplifier OA, applies a typical compensation, referred to as "pole splitting", whereby the poles are split by Miller's Effect.

[0033] As for the feedback branch connected to the inverting (-) input of the amplifier OA, it is at once apparent that the feedback at this input is a positive one. In fact, the signal present on the amplifier output U is inverted by the transistor M2 before it is applied to the inverting (-) input.

[0034] It is therefore necessary that, to reduce the loop gain of such positive feedback to a value of less than one, the load connected to the output of this current generator, on the drain terminal D2 of the transistor M2, has a very low input impedance value.

[0035] Shown in Figure 2 is a wiring diagram for a first implementation of the current generating circuit in Figure 1. In particular, the same circuit arrangement as in the previous embodiment has now been implemented using P-channel MOS transistors.

[0036] The circuit 1 comprises two P-channel transistors M1 and M2, and a voltage regulator 4. The first transistor M3 forms the input branch 2 of the current mirror and has its source terminal S3 connected to a fixed potential reference, specifically the positive pole Vcc of the supply voltage generator, while its drain terminal D3 is connected to a reference current Iref generator.

[0037] The output branch 3 of the current mirror consists of a second P-channel transistor M4. The source terminal S4 of this transistor is connected to the positive pole Vcc of the supply voltage generator, while the transistor drain terminal D4 is coincident with the output terminal of the circuit.

[0038] The control terminals G3 and G4 of both transistors M3 and M4 are connected together.

[0039] Advantageously, a voltage regulator 4 is connected to the drain terminals D3 and D4 of the transistors M3 and M4, thereby maintaining on said terminals a drain-source voltage value, V_{ds3} and V_{ds4} , which is the same for both transistors.

[0040] The voltage regulator 4 comprises an operational amplifier OA having two inputs, one of the inverting (-) type and another of the non-inverting (+) type, and an output U.

[0041] The non-inverting (+) input of the amplifier OA is connected to the drain terminal D3 of the first transistor M3. The inverting (-) input is connected to the drain terminal D4 of the second transistor M4, while the output U is connected to the common node A between the gate terminals G3 and G4 of both transistors M3 and M4.

[0042] A compensation capacitor C1 is connected between the output U and the non-inverting (+) input of the operational amplifier.

[0043] The circuit of Figure 2 operates in the same manner as the previously described circuit of Figure 1.

[0044] The voltage regulator 4, consisting of the operational amplifier OA, implies that the drain-source voltages, V_{ds3} and V_{ds4} , at the two transistors M3 and M4 should be the same value.

[0045] Accordingly, with the transistors M3 and M4 at the same gate-source voltage, they will operate in exactly the same condition.

[0046] Similar to the circuit of Figure 1, the feedback existing at the inverting (-) input of the operational amplifier OA is a positive one. It is therefore necessary that, to reduce the loop gain of said positive feedback to a value of less than one, the load connected to the output of this current generator has a very low input impedance value.

[0047] The circuit of Figure 1 is illustrated in greater detail by Figure 3; in particular, an optional embodiment of the operational amplifier OA using transistors of the MOS type is shown.

[0048] This amplifier OA is formed by four MOS transistors denoted by M5, M6, M7 and M8, in a known circuit arrangement. The two P-channel transistors M5 and M6 form the differential input stage, while the drain terminal D8 of the N-channel transistor M8 is the output terminal U of the amplifier.

[0049] Shown in Figure 4 is a wiring diagram for a second implementation of the current generating circuit illustrated by Figure 1. In particular, a circuit arrangement is shown which uses bipolar transistors of the NPN type.

[0050] The circuit 1 comprises two transistors T1 and T2 and a voltage regulator 4. The first transistor T1 forms the input branch 2 of the current mirror and has its emitter terminal E1 connected to a fixed potential reference, specifically the electric ground GND of the circuit, while its collector terminal C1 is connected to a reference current I_{ref} generator.

[0051] The output branch 3 of the current mirror con-

sists of a second transistor T2. The emitter terminal E2 of this transistor is connected to the electric ground GND of the circuit, the transistor collector terminal C2 being the output terminal of the circuit.

[0052] The base terminals B1 and B2 of both transistors T1 and T2 are connected together.

[0053] Advantageously, a voltage regulator 4 is connected to the collector terminals C1 and C2 of the transistors T1 and T2 to maintain at said terminals a collector-emitter voltage value, V_{ce1} and V_{ce2} , which is the same for both transistors.

[0054] The voltage regulator 4 comprises an operational amplifier OA having two inputs, one of the inverting (-) type and another of the non-inverting (+) type, and an output U.

[0055] The non-inverting (+) input of the amplifier OA is connected to the collector terminal C1 of the first transistor T1. The inverting (-) input is connected to the collector terminal C2 of the second transistor T2, while the output U is connected to the common node A between the base terminals B1 and B2 of both transistors T1 and T2.

[0056] A compensation capacitor C1 is connected between the output U of the operational amplifier and the non-inverting (+) input thereof.

[0057] The circuit of Figure 4 operates in a similar manner to the circuit of Figure 1.

[0058] The voltage regulator 4, consisting of the operational amplifier OA, implies that the collector-emitter voltages V_{ce1} and V_{ce2} at the two transistors T1 and T2 should be the same value. Accordingly, since the transistors T1 and T2 also have equal base-emitter voltages, they will be operating in similar conditions.

[0059] The feedback existing at the inverting (-) input of the operational amplifier OA is in this circuit positive, as in the circuit of Figure 1. It is necessary, therefore, that in order to reduce the loop gain of said positive feedback to a value of less than unity, the load connected to the output of this current generator has a very low input impedance value.

[0060] Figure 5 shows a wiring diagram for a third implementation of the current generating circuit illustrated by Figure 1. In particular, the same circuit arrangement has been embodied here using bipolar transistors of the PNP type.

[0061] The circuit comprises two transistors T3 and T4 and a voltage regulator 4. The first transistor T3 forms the input branch of the current mirror and has its emitter terminal E3 connected to a fixed potential reference, specifically the positive pole V_{cc} of the supply voltage generator, while its collector terminal C3 is connected to a reference current I_{ref} generator.

[0062] The output branch of the current mirror consists of a second transistor T4. The emitter terminal E4 of this transistor is connected to the positive pole V_{cc} of the supply voltage generator, while the transistor collector terminal C4 is the output terminal of the circuit.

[0063] The base terminals B3 and B4 of both transis-

tors T3 and T4 are connected together.

[0064] Advantageously, a voltage regulator 4 is connected to the collector terminals C3 and C4 of the transistors T3 and T4 to maintain, at said terminals, an equal collector-emitter voltage value, V_{ce3} and V_{ce4} , for both transistors.

[0065] The non-inverting (+) input of the amplifier OA is connected to the collector terminal C3 of the first transistor T3. The inverting (-) input is connected to the collector terminal C4 of the second transistor T4, while the output U is connected to the common node A between the base terminals B3 and B4 of both transistors T3 and T4.

[0066] A compensation capacitor C1 is connected between the output U and the non-inverting (+) input of the operational amplifier.

[0067] The circuit of Figure 5 operates similar to the circuit of Figure 1.

[0068] The voltage regulator 4, comprising the operational amplifier OA, implies that the collector-emitter voltages, V_{ce3} and V_{ce4} , at the two transistors T3 and T4 should be the same. Accordingly, since the transistors T3 and T4 also have the same base-emitter voltage, their conditions of operation will also be the same.

[0069] In a similar way to the circuit of Figure 1, this circuit also has a positive feedback present at the inverting (-) input of the operational amplifier OA, whereby the load connected to the output of this current generator is to have a very low input impedance value, if the loop gain of said positive feedback is to be a value of less than unity.

[0070] Figure 6 shows a wiring diagram for a digital-to-analog converter which employs a high-precision current generating circuit in accordance with this invention.

[0071] In particular, the output branch 30 of the current mirror circuit 10 comprises, additionally to the first transistor M12, two more transistors M13 and M14. The drain D13, D14 and source S13, S14 terminals of these transistors are respectively connected to the drain D12 and source S12 terminals of the first transistor M12, while their gate terminals G13 and G14 are connected, each through a switch sw1 and sw2, to the gate terminal G12 of the first transistor M12.

[0072] The two switches sw1 and sw2 are controlled by the digital input signal, and the currents flowed through the individual transistors M12, M13 and M14 are summed into the output current Iout from the D/A converter. In this particular embodiment, the digital input signal is a two-bit signal, but it would be quite easy, as can be evinced from the modular construction of the output branch 30, to multiply the number of the transistors provided to achieve enhanced resolution for the D/A converter.

[0073] Thus, the circuit of this invention provides a high-precision current generator which is quite simple circuit-wise. In addition, this circuit can be used in different technologies, bipolar and MOS transistors, and can operate on a low supply voltage.

[0074] A further advantage is that the output branch of this current generator can be easily duplicated to output several currents from a single reference current.

Claims

1. A high-precision current generating circuit (1), particularly intended for a low-impedance circuit user, being of the type which comprises:

- a transistor current mirror having an input branch (2) and an output branch (3), wherein the input branch (2) comprises at least a first transistor (M1) and the output branch (3) comprises at least a second transistor (M2), both transistors having first terminals (S1, S2) connected to a fixed potential reference (GND), control terminals (G1, G2) connected together, and second terminal (D1, D2), the second terminal (D1) of the first transistor (M1) being connected to a current (Iref) generator, and
- a voltage regulator (4) having at least a first (+) and a second (-) terminal respectively connected to the second terminal (D1) of the first transistor (M1) and the second terminal (D2) of the second transistor (M2) to maintain equal voltage values at said terminals, said voltage regulator (4) comprising an operational amplifier (OA) having a first input (+) connected to the second terminal (D1) of the first transistor (M1) and a second input (-) connected to the second terminal (D2) of the second transistor (M2), and an output (U) connected to the control terminals (G1, G2) of the first (M1) and the second (M2) transistors, characterised in that:
- said operational amplifier (OA) is of the CMOS type and comprises third (M5) and fourth MOS transistor (M6) forming a differential input stage of the operational amplifier (OA), and fifth (M7) and sixth MOS transistor (M8) forming an output stage of the operational amplifier (OA), the drain terminal (D8) of the sixth MOS transistor (M8) being the output terminal (U) of the amplifier operational amplifier (OA); and
- a compensation capacitor (C1) is connected between the non-inverting (+) input and the output (U) of the operational amplifier (OA).

2. A circuit according to Claim 1, characterized in that said third (M5) and fourth MOS transistor (M6) of the operational amplifier (OA) are P-channel transistors, while said fifth (M7) and sixth MOS transistor (M8) of the operational amplifier (OA) are N-

channel transistors.

3. A circuit according to Claim 2, characterized in that said output (U) of the operational amplifier (OA) supplies a bias voltage to said first (M1) and the second (M2) transistors and in that the first and second transistors (M1, M2) have their source terminals (S1, S2), and gate terminals (G1, G2) connected together, thus forcing their drain-source voltages (V_{ds1} , V_{ds2}) to the same value in such a manner that said transistors (M1, M2) operate in exactly the same condition. 5
4. A circuit according to Claim 1, characterized in that the output branch (3) of said current mirror comprises at least an additional transistor (M13) having first and second terminals and a control terminal, the first (S13) and second (D13) terminals being connected to the corresponding terminals (S2, D2) of the second transistor (M2) and the control terminal (G13) being connected to the control terminal (G2) of said second transistor (M2) through a first switch means (SW1). 10 15 20
5. A circuit according to any of the preceding claims, characterized in that said first, second and additional transistors (M1, M2, M13) are of the N-channel MOS type. 25
6. A circuit according to any of Claims 1 to 4, characterized in that said first, second and additional (M1, M2, M13) transistors are of the P-channel MOS type. 30
7. A circuit according to any of Claims 1 to 4, characterized in that said first, second and additional (M1, M2, M13) transistors are of the NPN bipolar type. 35
8. A circuit according to any of Claims 1 to 4, characterized in that said first, second and additional transistors (M1, M2, M13) are of the PNP bipolar type. 40

Patentansprüche

1. Hochgenaue Stromerzeugungsschaltung (1), die insbesondere für einen impedanzarmen Schaltungsnutzer vorgesehen ist und von der Art ist, die aufweist: 45

einen Transistorstromspiegel mit einem Eingangszweig (2) und einem Ausgangszweig (3), wobei der Eingangszweig (2) mindestens einen ersten Transistor (M1) aufweist und der Ausgangszweig (3) mindestens einen zweiten Transistor (M2) aufweist, wobei beide Transistoren mit einer Festpotentialreferenz (GND) verbundene erste Anschlüsse (S1, S2), zusam-

mengeschaltete Steueranschlüsse (G1, G2) und zweite Anschlüsse (D1, D2) haben, wobei der zweite Anschluß (D1) des ersten Transistors (M1) mit einem Strom-(Iref) Generator verbunden ist, und

einen Spannungsregler (4) mit mindestens einem ersten (+) und einem zweiten (-) Anschluß, die mit dem zweiten Anschluß (D1) des ersten Transistors (M1) bzw. mit dem zweiten Anschluß (D2) des zweiten Transistors (M2) verbunden sind, um gleiche Spannungswerte an den Anschlüssen beizubehalten, wobei der Spannungsregler (4) aufweist: einen Operationsverstärker (OA) mit einem ersten Eingang (+), der mit dem zweiten Anschluß (D1) des ersten Transistors (M1) verbunden ist, und einem zweiten Eingang (-), der mit dem zweiten Anschluß (D2) des zweiten Transistors (M2) verbunden ist, sowie einem Ausgang (U), der mit den Steueranschlüssen (G1, G2) des ersten (M1) und zweiten (M2) Transistors verbunden ist,

dadurch gekennzeichnet, daß:

der Operationsverstärker (OA) vom CMOS-Typ ist und aufweist: einen dritten (M5) und vierten MOS-Transistor (M6), die eine Differenzeingangsstufe des Operationsverstärkers (OA) bilden, sowie einen fünften (M7) und sechsten MOS-Transistor (M8), die eine Ausgangsstufe des Operationsverstärkers (OA) bilden, wobei der Drainanschluß (D8) des sechsten MOS-Transistors (M8) der Ausgangsanschluß (U) des Operationsverstärkers (OA) ist; und ein Ausgleichskondensator (C1) zwischen dem nichtinvertierenden (+) Eingang und dem Ausgang (U) des Operationsverstärkers (OA) verbunden ist.

2. Schaltung nach Anspruch 1, dadurch gekennzeichnet, daß der dritte (M5) und vierte MOS-Transistor (M6) des Operationsverstärkers (OA) p-Kanal-Transistoren sind, während der fünfte (M7) und sechste MOS-Transistor (M8) des Operationsverstärkers (OA) n-Kanal-Transistoren sind. 45

3. Schaltung nach Anspruch 2, dadurch gekennzeichnet, daß der Ausgang (U) des Operationsverstärkers (OA) eine Vorspannung zum ersten (M1) und zweiten (M2) Transistor führt, und dadurch, daß beim ersten und zweiten Transistor (M1, M2) ihre Sourceanschlüsse (S1, S2) und Gateanschlüsse (G1, G2) zusammengeschaltet sind, wodurch ihre Drain-Source-Spannungen (V_{ds1} , V_{ds2}) zwangsweise so auf den gleichen Wert eingestellt sind, daß die Transistoren (M1, M2) in genau dem gleichen Zustand arbeiten. 50 55

4. Schaltung nach Anspruch 1, dadurch gekennzeichnet,

net, daß der Ausgangszweig (3) des Stromspiegels mindestens einen zusätzlichen Transistor (M13) mit einem ersten und zweiten Anschluß sowie einem Steueranschluß aufweist, wobei der erste (S13) und zweite (D13) Anschluß mit den entsprechenden Anschlüssen (S2, D2) des zweiten Transistors (M2) verbunden sind und der Steueranschluß (G13) mit dem Steueranschluß (G2) des zweiten Transistors (M2) über eine erste Schalteinrichtung (SW1) verbunden ist.

5. Schaltung nach einem der vorstehenden Ansprüche, dadurch gekennzeichnet, daß der erste, zweite und zusätzliche Transistor (M1, M2, M13) vom n-Kanal-MOS-Typ sind.
6. Schaltung nach einem der Ansprüche 1 bis 4, dadurch gekennzeichnet, daß der erste, zweite und zusätzliche Transistor (M1, M2, M13) vom p-Kanal-MOS-Typ sind.
7. Schaltung nach einem der Ansprüche 1 bis 4, dadurch gekennzeichnet, daß der erste, zweite und zusätzliche Transistor (M1, M2, M13) vom bipolaren npn-Typ sind.
8. Schaltung nach einem der Ansprüche 1 bis 4, dadurch gekennzeichnet, daß der erste, zweite und zusätzliche Transistor (M1, M2, M13) vom bipolaren pnp-Typ sind.

Revendications

1. Circuit de génération de courant de haute précision (1), destiné en particulier à un circuit d'utilisateur à basse impédance, du type comprenant :
 - un miroir de courant à transistors ayant une branche d'entrée (2) et une branche de sortie (3), dans lequel la branche d'entrée (2) comprend au moins un premier transistor (M1) et la branche de sortie (3) comprend au moins un second transistor (M2), les deux transistors ayant des premières bornes (S1, S2) connectées à une référence de potentiel fixe (GND), des bornes de commande (G1, G2) connectées l'une à l'autre, et des secondes bornes (D1, D2), la seconde borne (D1) du premier transistor (M1) étant connectée à un générateur de courant (Iref), et
 - un régulateur de tension (4) ayant au moins des première (+) et seconde (-) bornes respectivement connectées à la seconde borne (D1) du premier transistor (M1) et à la seconde borne (D2) du second transistor (M2) pour maintenir des valeurs de tension égales sur lesdites bornes, le régulateur de tension (4) comprenant un

amplificateur opérationnel (OA) ayant une première entrée (+) connectée à la seconde borne (D1) du premier transistor (M1) et une seconde entrée (-) connectée à la seconde borne (D2) du second transistor (M2) et une sortie (U) connectée aux bornes de commande (G1, G2) des premier (M1) et second (M2) transistors, caractérisé en ce que :

- l'amplificateur opérationnel (OA) est du type CMOS et comprend des troisième (M5) et quatrième (M6) transistors MOS formant un étage différentiel d'entrée de l'amplificateur opérationnel (OA), et des cinquième (M7) et sixième (M8) transistors MOS formant un étage de sortie de l'amplificateur opérationnel (OA), la borne de drain (D8) du sixième transistor (M8) étant la borne de sortie (U) de l'amplificateur opérationnel (OA), et
 - un condensateur de compensation (C1) est connecté entre l'entrée non-inverseuse (+) et la sortie (U) de l'amplificateur opérationnel (OA).
2. Circuit selon la revendication 1, caractérisé en ce que les troisième (M5) et quatrième (M6) transistors MOS de l'amplificateur opérationnel (OA) sont des transistors à canal P alors que les cinquième (M7) et sixième (M8) transistors MOS de l'amplificateur opérationnel (OA) sont des transistors à canal N.
 3. Circuit selon la revendication 2, caractérisé en ce que la sortie (U) de l'amplificateur opérationnel (OA) fournit une tension de polarisation aux premier (M1) et second (M2) transistors et en ce que les premier et second transistors (M1, M2) ont leurs bornes de source (S1, S2) et leurs bornes de grille (G1, G2) connectées l'une à l'autre, forçant ainsi leur tension drain/source (V_{ds1} , V_{ds2}) à la même valeur, de sorte que lesdits transistors (M1, M2) fonctionnent exactement dans les mêmes conditions.
 4. Circuit selon la revendication 1, caractérisé en ce que la branche de sortie (3) du miroir de courant comprend au moins un transistor supplémentaire (M13) ayant des première et seconde bornes et une borne de commande, les première (S13) et seconde (D13) bornes étant connectées aux bornes correspondantes (S2, D2) du second transistor (M2) et la borne de commande (G13) étant connectée à la borne de commande (G2) du second transistor (M2) par l'intermédiaire d'un premier moyen de commutation (SW1).
 5. Circuit selon l'une quelconque des revendications précédentes, caractérisé en ce que le premier transistor, le second transistor et le transistor supplémentaire (M1, M2, M13) sont de type MOS à canal N.

6. Circuit selon l'une quelconque des revendications 1 à 4, caractérisé en ce que le premier transistor, le second transistor et le transistor supplémentaire (M1, M2, M13) sont de type MOS à canal P.

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7. Circuit selon l'une quelconque des revendications 1 à 4, caractérisé en ce que le premier transistor, le second transistor et le transistor supplémentaire (M1, M2, M13) sont de type bipolaire NPN.

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8. Circuit selon l'une quelconque des revendications 1 à 4, caractérisé en ce que le premier transistor, le second transistor et le transistor supplémentaire (M1, M2, M13) sont de type bipolaire PNP.

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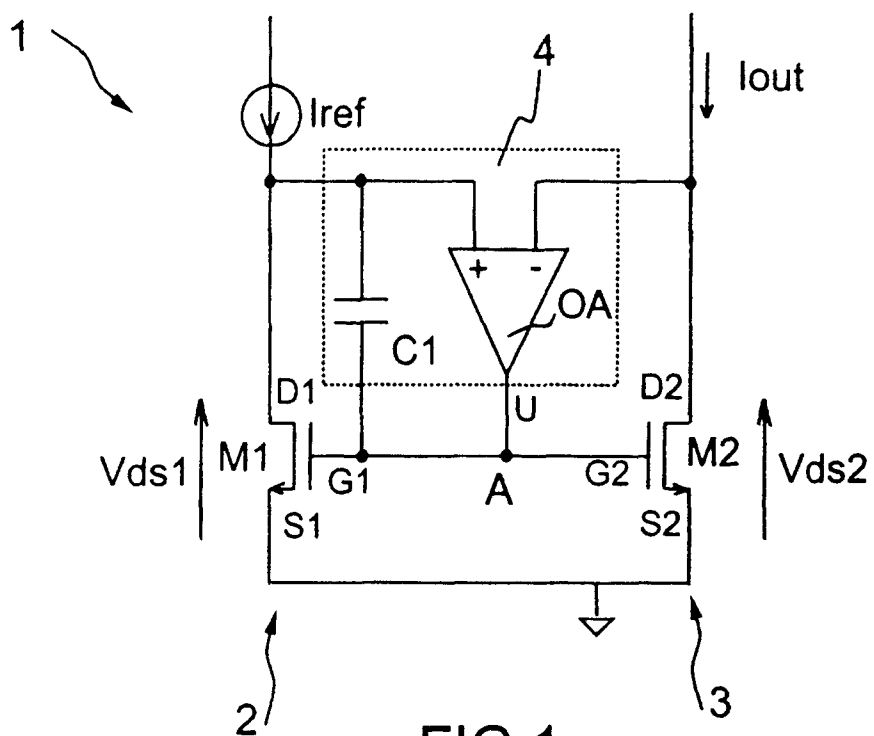


FIG.1

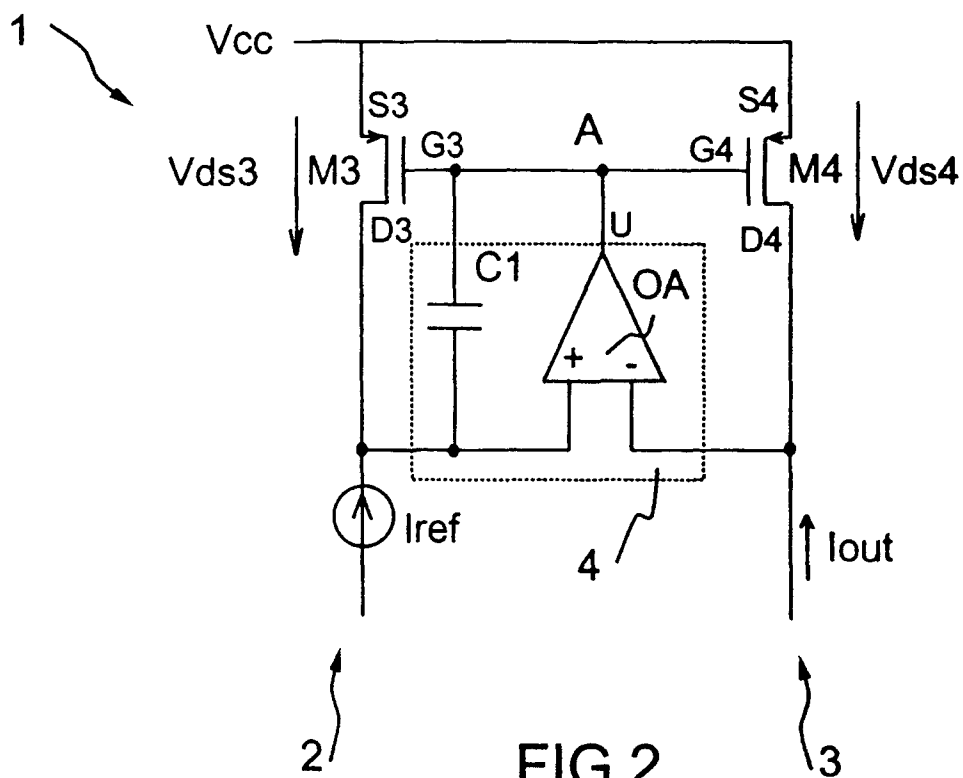


FIG.2

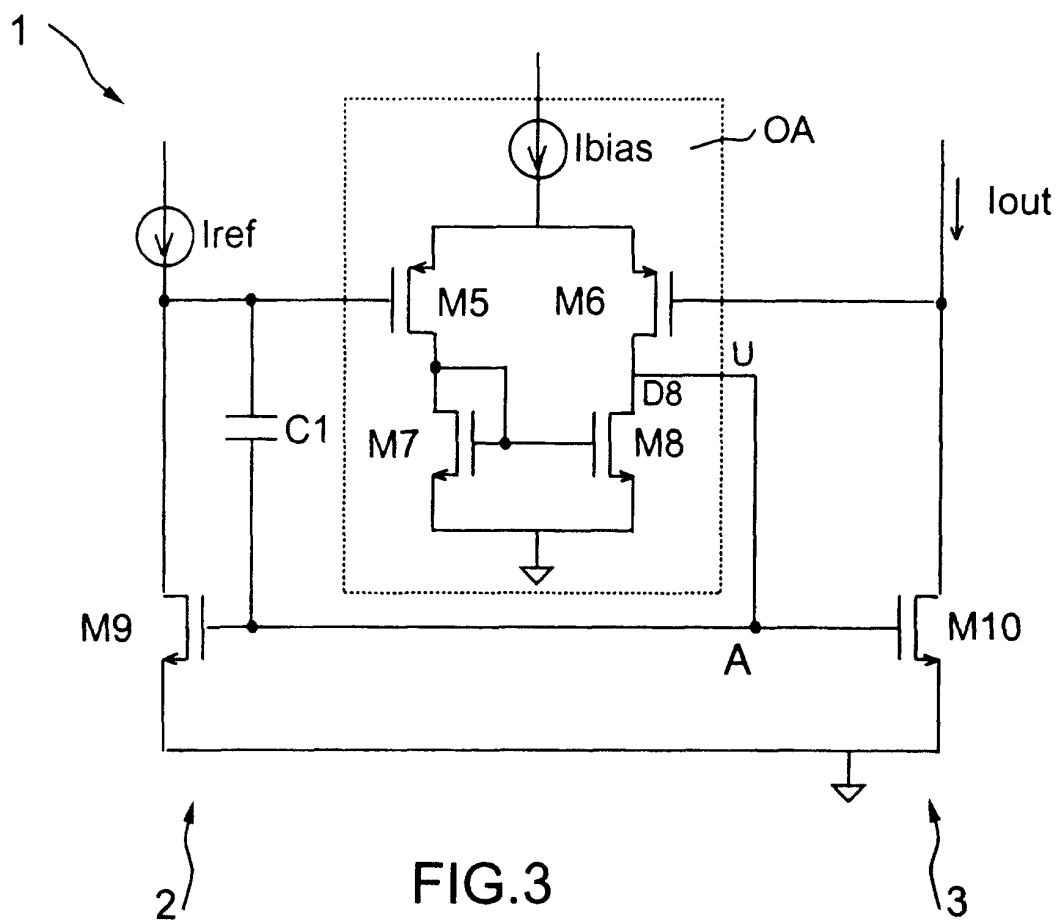


FIG.3

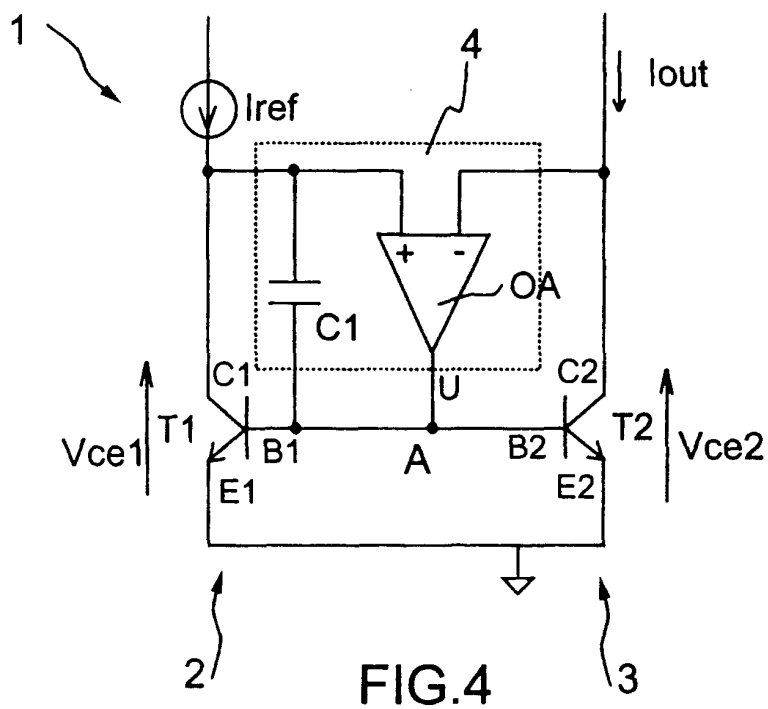


FIG.4

