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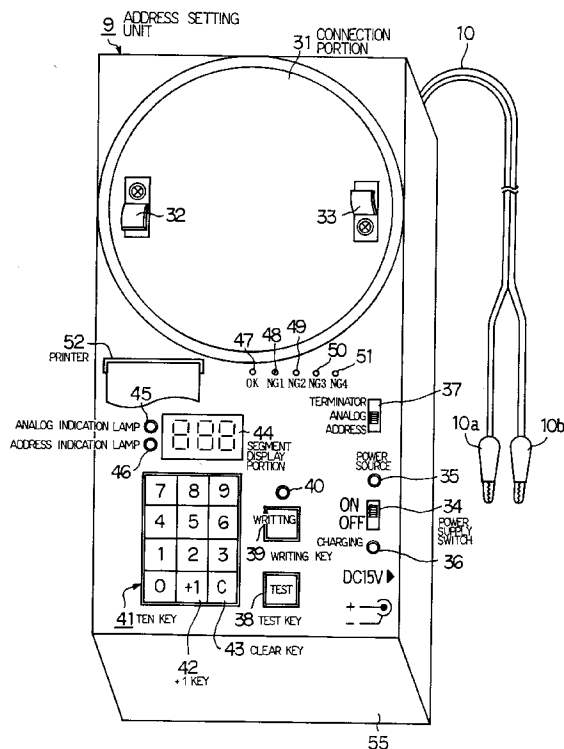
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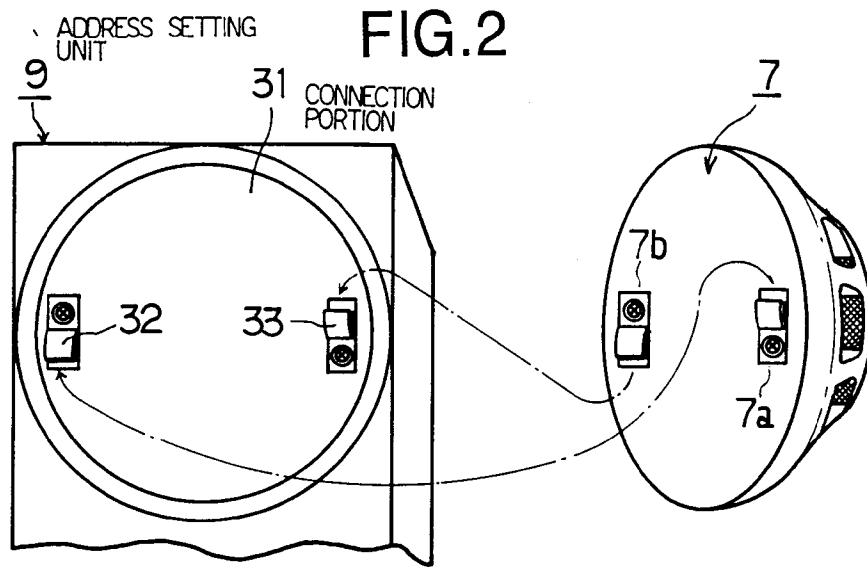
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CH-1211 Genève 12 (CH)(54) **Address setting unit for fire detector**

(57) The body of a detector is connected to a connection portion, a ten-key pad and a + 1 key are used to set the address, and a writing key is depressed to write the address on a memory. When a mode switch is set to an analog mode and then a test key is depressed, a test of the detector can be performed in such a manner that address information of the body of the detector is read and indicated through the connection portion. Furthermore, when a test cable is connected to a terminator of a circuit in the detector followed by switching the mode switch to a terminator side and depressing the test key, a test of the terminator can be performed. According to the present invention having the foregoing structure, a multiplicity of addresses can be set in a short time, satisfactory portability can be realized and a test of the detector and that of the terminator can be performed.

FIG.1



Description

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to an address setting unit for a detector that is capable of writing and reading address to and from a non-volatile memory in the body of the detector, indicating an analog value of the body of the detector and performing a test of a terminator of a circuit in the detector.

Prior Art

Hitherto, in a fire detection system including a control panel for receiving detection signals from a plurality of fire detectors, the detector of a type which detects a polling transmitted from the control panel to call the detector to discriminate the self-address, is arranged to set the address by using a dip switch thereof. That is, the dip switch is provided for a transmission control circuit comprising a CPU; the address is manually set; and the transmission control circuit discriminates the self-address in accordance with an output from a polling pulse detection circuit.

The manual operation for setting the address by using the dip switch sometimes encounters an error, and the dip switch having a large size requires a large space.

Accordingly, the detector is provided with an EEPROM in the form of a non-volatile memory so that the address is stored in the EEPROM to overcome the problems suffered from the dip switch. An invention of the foregoing type has been disclosed in U.S.P. No. 4,658,243.

In the case where the address is stored in the EEPROM, an apparatus for setting the address is required. Setting of the address is performed in such a manner that addresses of a multiplicity of detectors are collectively set when the detectors are delivered from a manufacturing plant or the address is set before the detector is installed in a desired place. In the former case, a function is required which is capable of setting a multiplicity of addresses in a short time. In the latter case, an apparatus that can easily be transported is required. In either case, setting of the address can reliably set. Moreover, if the address is set at a place where the detector is installed, an apparatus has been desired to have a multiplicity of functions, of course, capable of setting the address, and performing tests of the function of the detector and the terminator which is provided for a circuit in the detector.

However, the conventional address setting units have been considered to only have a function of directly writing the address on the EEPROM included in the detector by using a ROM writer. Thus, the conventional units cannot easily be used to set the address into the EEPROM included in the body of the manufactured de-

tor. Moreover, the conventional units have not been considered to be used in both cases where the addresses are set at the delivery from the manufacturing plant and where the addresses are set at the places where the detectors are installed. Thus, a satisfactory address setting unit has not been realized yet.

SUMMARY OF THE INVENTION

In view of the foregoing, an object of the present invention is to provide an address setting unit which is capable of setting a multiplicity of addresses in a short time, which can easily be transported, with which the set address can be confirmed and which enables tests of the detector and the terminator to be performed.

To achieve the foregoing object, according to one aspect of the present invention, there is provided an address setting unit capable of realizing a function of setting the address by a structure comprising a detector connection portion for connecting the body of the detector provided with a memory for storing address information; an address inputting portion for inputting the address information of the body of the detector; an indication portion for indicating the address information; and an address writing portion for writing the address information input from the address inputting portion on the memory of the body of the detector.

The address setting unit for a fire detector according to the present invention and having the foregoing structure only requires establishment of the connection between the body of the detector, the address of which is intended to be set, and a detector connection portion, inputs of the address numbers by using a ten-key pad and depression of a writing key to enable a transmission control function and a command execution function of the body of the detector to be used to automatically write the address on the memory in the body of the detector.

According to another aspect of the present invention, it is preferable that the detector connection portion is formed into an attaching substrate for use when the fire detectors are attached to a variety of portions in an architecture, the detector connection portion having metal connectors which can be received by metal connectors of the body of the detector.

Therefore, by only turning the body of the detector to be received by the detector connection portion in a similar manner in the case where installation to the surface of a ceiling is performed, the present invention enables the body of the detector to be received and connected to the detector connection portion. That is, the connection can be performed very easily. Furthermore, the connection can be established by the same structure as that required in the case where the installation to the surface of the ceiling or the like is performed. Thus, the operations can be unified and the metal connectors can be used commonly.

According to another aspect of the present invention, it is preferable that the address inputting portion

includes a ten-key pad for inputting the number to be given to the address information and a + 1 key for sequentially increasing the number to be given to the address.

According to the present invention, when addresses of a multiplicity of detectors are set, a simple operation of the + 1 key having an increment function is required after the address numbers have been input with the ten-key to give serial numbers to the addresses. Thus, an address input signal required whenever each address is input can be omitted. As a result, a multiplicity of addresses can be set in a short time.

According to another aspect of the present invention, it is preferable that the foregoing address setting unit for a fire detector further comprises: a printer for printing out the address information; and a printer control portion for causing the printer to print the address information if writing of the address information on the memory of the body of the detector by the address writing portion has been completed normally, wherein the printer prints the address information on a paper sheet having a separable adhesive seals, and the adhesive seal, on which the address information has been printed, is separated and applied to the body of the detector.

According to the present invention having the foregoing structure, the sheet having separable and adhesive seals on each of which the address information can be printed by the printer when the address has been written normally is used so that the seal having the address information printed thereto is easily separated and applied to the body of the detector. Therefore, an error occurring when the address information is written manually can be prevented.

According to another aspect of the present invention, it is preferable that the foregoing address setting unit for a fire detector further comprises: a test key for instructing confirmation of the address information written on the memory of the body of the detector; and an address reading portion for reading the address information from the memory of the body of the detector in accordance with the operation of the test key to indicate the read address information on the indication portion.

According to the present invention having the foregoing structure, depression of the test key in the address setting mode causes the address written on the memory of the body of the detector to be read and indicated. Thus, after new address has been set, whether or not the address has been set correctly can be confirmed.

According to another aspect of the present invention, it is preferable that the foregoing address setting unit for a fire detector further comprises: a mode switch for switching an address setting mode to a detector testing mode; and a detector testing portion for requiring the body of the detector to transmit detected information when the mode switch has switched the mode to the detector testing mode to indicate, on the indication portion, the detected information transmitted from the body of the detector; and that the body of the detector has an

analog detector circuit for receiving an A/D conversion command to transmit a detected analog value, and the detector testing portion transmits the A/D conversion command to the body of the detector when the mode switch has been switched to the detector testing mode.

According to the present invention having the foregoing structure, when the detector testing mode is set, the test of the function of the detector can be performed in such a manner that the A/D conversion command is transmitted to the body of the detector and causes the analog value to be returned and indicated.

According to another aspect of the present invention, it is preferable that the foregoing address setting unit for a fire detector further comprises: a test cable which can be connected to a terminator connected to a circuit in the detector; a mode switch for switching the address setting mode to a terminator testing mode; and a terminator discrimination portion for reading the voltage of the circuit in a state where predetermined test voltage is applied to the test cable when the mode switch has been switched to the terminator testing mode in a state where the test cable is connected to the terminator of the circuit in the detector; and that the terminator discrimination portion discriminates a normal state or an abnormal state, such as non-connection or erroneous connection of the terminator, in accordance with the voltage of the circuit to indicate a result of the discrimination.

According to the present invention having the foregoing structure, when the test cable having alligator clips is connected to the terminator of the circuit in the detector and the terminator testing mode is set, test voltage is applied to the circuit in the detector so that voltage of the circuit corresponding to the state of the terminator is obtained. By reading the voltage of the circuit, the test of the terminator can be performed in such a manner that whether or not a predetermined terminator is normally connected is discriminated. After the test of the terminator has been performed, the normal or abnormal state of the same, such as no terminator being connected or a terminator being erroneously connected, is discriminated and a corresponding indication lamp indicates the state. Therefore, the type of the abnormal state can immediately be recognized by a user.

Other and further objects, features and advantage of the invention will be appear more fully from the following description.

BRIEF DESCRIPTION OF THE DRAWINGS

- Fig. 1 is a schematic view showing an embodiment of an address setting unit for a fire detector according to the present invention;
 Fig. 2 is a perspective view showing the state of connection between the address setting unit for a fire detector and an analog detector;
 Fig. 3 is a side view showing the state of the connection;
 Fig. 4 is a block diagram showing the structure of a

circuit in the detector;

Fig. 5 is a diagram showing a sheet for use in the printer shown in Fig. 1;

Fig. 6 is a diagram showing a state of a test of a terminator;

Fig. 7 is a block diagram of a circuit in the address setting unit shown in Fig. 1;

Fig. 8 is a flow chart of the operation according to the present invention; and

Fig. 9 is a diagram showing the state of the terminator to be subjected to the test.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 1 is a schematic view of an embodiment of an address setting unit according to the present invention.

In the address setting unit 9 shown in Fig. 1, reference numeral 31 represents a connection portion for connecting the body of a detector. A pair of metal connectors 32 and 33 as well as serving as electrical contacts are, by screws, secured to the connection portion 31. The connecting structure has the same form as that of a base of a detector, the body of which is disposed on the surface of the ceiling or the like. As shown in Fig. 2, metal connectors 7a and 7b of the body of an analog detector (hereinafter called a "detector") 7 are turned and received by the metal connectors 32 and 33 so that the address setting unit 9 and the body of the detector 7 can be connected to each other. Namely, the body of the detector 7 can be attached and connected independently in such a manner that the body of the detector 7 is completely separated from the surface of a ceiling or the like to which the body of the detector 7 has been disposed. The foregoing state is shown in Fig. 3. The body of the detector 7 is exemplified by a photoelectric analog smoke detector 7 shown in Fig. 4.

Referring to Fig. 4, the detector 7 consists of a base 11 and a body 12. The base 11 of the detector 7 is directly attached to the ceiling, while the body 12 of the detector 7 is attached to the base 11 of the detector 7 through the metal connectors 7a and 7b as well as serving as electric contacts. The base 11 of the detector 7 is provided with an alarm issue indication circuit 13 so that a circuit in the body 12 is connected to a control panel 1 through the alarm issue indication circuit 13 and a transmission passage 2.

The body 12 of the detector 7 is provided with a rectifying circuit 14 for making the connection polarity to be non-polar, a noise absorption circuit 15, a transmission signal detection circuit 16 for detecting a signal transmitted, by the polling method, from the control panel 1, and a response signal transmitting circuit 17 for returning a response signal to the control panel 1. In the rear of the response signal transmitting circuit 17, there is disposed a constant-voltage circuit 20 for generating constant voltage of 3.2 V for operating the testing infrared LED 19, the constant-voltage circuit 20 as well as

generating constant voltage of 10 V for amplifying the received output.

In the rear of the constant-voltage circuit 20, a transmission control circuit 21 comprising a CPU for executing the transmission procedure with respect to the control panel 1 is disposed. The transmission control circuit 21 controls an LED operating circuit 22 to operate the smoke-detecting infrared LED 18 and the testing infrared LED 19. When smoke detection is performed, the transmission control circuit 21 causes the smoke-detecting infrared LED 18 to emit pulse beams. When a test is performed, the transmission control circuit 21 causes the testing infrared LED 19 to emit pulse beams.

Light emitted from the smoke-detecting infrared LED 18 and scattered by smoke is photoelectrically converted by a light receiving device 23 and then detected by a light receiving circuit 24. A detection signal from the light receiving circuit 24 is amplified by an amplifying circuit 25 and supplied to the transmission control circuit 21. The transmission control circuit 21 returns the level of an output from the amplifying circuit 25 and the address previously set in a non-volatile memory 26 to the control panel 1 through the response signal transmitting circuit 17.

The non-volatile memory 26 is an EEPROM on which address information is written by the address setting unit 9 according to the present invention and from which the previously set address information is read.

Referring back to Fig. 1, reference numeral 34 represents a power supply switch. When the power supply switch 34 is switched on, a power source lamp 35 is turned on. When the power supply switch 34 is switched off in a state where a DC jack of an AC adapter (not shown) is connected, a charging lamp 36 is turned on so that charging of electric power is commenced. If the voltage of an included battery is dropped to a predetermined level, the power source lamp 35, which has been turned on, is brought into a flash mode. When the power supply switch 34 is switched on, all of the indication portions emit light for a predetermined time so that self-diagnosis is performed.

Reference numeral 37 represents a slide switch for setting a mode selected from a group consisting of an address setting mode, a detector testing mode and a terminator testing mode. When the slide switch 37 is switched to "ADDRESS" and a writing key 39 is depressed, address information is written to the non-volatile memory 26 of the detector 7. When address information is being written, a writing lamp 40 is turned on.

When the slide switch 37 is switched to "ADDRESS" and a test key 38 is depressed, address information previously set in the non-volatile memory 26 of the detector 7 is read and then indicated on a segment indication portion 44. When the slide switch 37 is switched to "ANALOG" and the test key 38 is depressed, a test of the detector 7 is performed. When the slide switch 37 is switched to "TERMINATOR", a test of a terminator 8 is performed.

Reference numeral 41 represents a ten-key pad, the ten-key pad 41 being used to input address information. In a case where addresses information items of a multiplicity of detectors are given serial numbers and collectively set, an increment (+ 1) key 42 in the ten-key pad 41 is used so that the address inputting operation required at each operation is omitted. If writing or reading of the address information or reading of the analog value becomes a failure and, thus, occurrence of error is indicated, a clear key 43 is used to clear the indicated contents.

Reference numeral 44 represents a segment indication portion. The segment indication portion 44 indicates a read analog value after the test of the detector 7 has been performed. When address information has been written, the segment indication portion 44 indicates the new address. When address information has been read, it indicates the read address. Also the segment indication portion 44 indicates occurrence of an error in the test of the detector 7 and an error occurring in reading the analog value. When the test of the detector 7 is performed, an analog indication lamp 45 is turned on. During writing or reading of address information, an address indication lamp 46 is turned on.

If a predetermined terminator 8 is connected normally as a result of the test of the terminator 8, an OK lamp 47 is turned on. If no terminator is connected or an undesirable terminator is connected and, therefore, an abnormal state is realized, NG1 to NG4 lamps 48 to 51 are turned on. The OK lamp 47 indicates connection of one terminator 8, the NG1 lamp 48 indicates no terminator, the NG2 lamp 49 indicates connection of two or more terminators, the NG3 lamp 50 indicates connection of a resistor, and the NG4 lamp 51 indicates connections of a terminator and a resistor.

Reference numeral 52 represents a printer. The printer 52 prints the set address information. A seal sheet 53 having a plurality of seals 54 applied thereto as shown in Fig. 5 is used in the printer 52. Address information is, by the printer 52, printed on the seal 54 of the seal sheet 53 after setting of address to the body 12 of the detector 7 has been completed normally. The seal 54, on which the address information has been printed, is separated and applied to, for example, the reverse side of the body 12 of the detector 7. Thus, an error, which can be made in transferring the address information, can be prevented.

Furthermore, a test cable 10 for use in the test of the terminator 8 is extended from an upper portion of the address setting unit 9 shown in Fig. 1, the test cable 10 having, at the leading ends thereof, alligator clips 10a and 10b to be connected to a circuit in the detector 7 of the terminator 8 to be subjected to the test. The test cable 10 is prepared as an accessory and used when the test of the terminator 8 is performed in such a manner that the test cable 10 is connected to a jack terminal attached to the address setting unit 9.

Fig. 6 shows a state where the test of the terminator

8 is performed by using the address setting unit 9 shown in Fig. 1. Referring to Fig. 6, reference numeral 1 represents the control panel. The transmission passage 2 is extended from the control panel 1. A relay 3 for a detector and the analog detector 7 are connected to the transmission passage 2. A circuit in the analog detector 7, consisting of a signal line 5 and a common line 6, is extended from the relay 3 for a detector. Between lines of the circuit in the detector 7, there are connected an on/off detector 4 and the terminator 8 comprising two zener diodes.

The analog detector 7 has a function to serve as a relay so that it transmits, to the control panel 1, an analog signal detected by a heat sensor or a smoke density sensor thereof. A peculiar address has been previously set to each of the relay 3 for a detector and the analog detector 7. If the address communicated from the address coincides with the address of each of the relay 3 for a detector and the analog detector 7, a process is performed in accordance with a received command. When the test of the terminator 8 is performed by using the address setting unit 9 according to the present invention, the test cable 10 is connected between the line 5 and the line 6 in the analog detector 7 connected to the analog terminator 8.

Note that a body 55 of the address setting unit 9 is formed into an aluminum case exhibiting light weight, the body 55 having a battery therein so as to be formed into a handy unit which can easily be transported by a user.

Fig. 7 is a block diagram of a circuit in the address setting unit 9.

Referring to Fig. 7, reference numeral 61 represents an AC adapter. The AC adapter 61 is inserted into a commercial power source when used. In the case where the AC adapter 61 is connected, the included battery 62 is separated to use the power from the AC adapter 61. A DC output from the AC adapter 61 is, through a connection portion 63, supplied to a power supply circuit 64. When the power supply switch 34 is switched on, power is supplied from the power supply circuit 64 to each section so that the power source lamp 35 is turned on.

When the AC adapter 61 is connected and then the power supply switch 34 is switched off, the included battery 62 is charged by a battery charging circuit 66 so that the charging lamp 36 is turned on. By removing the AC adapter 61, the power source is switched to the included battery 62 so that, when the power supply switch 34 is switched on, power is supplied from the included battery 62 to each section through the power supply circuit 64.

Reference numeral 67 represents an indication unit consisting of the power source lamp 35, the writing lamp 40, the segment indication portion 44, the analog indication lamp 45, the address indication lamp 46, the OK lamp 47 and the NG1 to NG4 lamps 48 to 51 shown in Fig. 1. When a command of indication is supplied from

a CPU 68, each lamp indicates the corresponding content. When power is supplied, the CPU 68 issues a command of indication to each of the indication portions of the indication unit 67 so that each indication portion is turned on for a predetermined time to perform a self-test.

Reference numeral 69 represents an operation switch portion 69. The operation switch portion 69 consists of the slide switch 37, the power supply switch 34, the ten-key pad 41, the writing key 39 and the test key 38 shown in Fig. 1 and transmits a signal to the CPU 68. The slide switch 37 transmits a terminator testing mode signal, a detector testing mode signal and an address testing mode signal, the writing key 39 transmits an address writing signal and the test key 38 transmits a detector testing signal or an address reading signal to the CPU 68. A power source signal is supplied from the power supply switch 34 to the CPU 68.

Writing address information is supplied from the ten-key pad 41 to the CPU 68, while a signal for increasing by one from + 1 key 42 and a signal for clearing indication from the clear key 43 are supplied to the CPU 68. The CPU 68 has a function of an address writing portion 68A for commanding the CPU 21 of the body 12 of the detector 7 to write address information to the non-volatile memory 26 in accordance with the operations of the slide switch 37, the writing key 39 and the ten-key pad 41, and a function of an address reading portion 68B for commanding the CPU 21 of the body 12 of the detector 7 to read address information previously set to the non-volatile memory 26 in accordance with the operations of the slide switch 37 and the test key 38.

Furthermore, the CPU 68 has a function of a test signal transmitting portion 68C for transmitting terminator checking pulses, serving as a test signal of the terminator 8, in accordance with the operation of the slide switch 37; and a function of a detector testing portion 68D for transmitting, to the body 12 of the detector 7, an A/D conversion command and causing the body 12 to return an analog value in accordance with the operations of the slide switch 37 and the test key 38.

Reference numeral 70 represents a terminator discrimination circuit. When testing voltage is applied to a circuit in the detector 7 in response to the check pulses of the terminator 8 supplied from the CPU 68, the terminator discrimination circuit 70 reads the voltage between the lines of the circuit in the detector 7, the level of which depends upon the connected terminator 8 so as to discriminate the state of the terminator 8. At this time, the test cable 10 shown in Fig. 1 is connected to jack terminals 71 and 72 of the terminator 8 so as to test the terminator 8 as shown in Fig. 6.

Reference numeral 73 represents a circuit 73 for detecting a transmission signal and a response signal, the circuit 73 being arranged to detect a signal transmitted from the CPU 68 to transmit the signal to the body 12 of the detector 7 through connection terminals 74 and 75 and to detect a response signal from the body 12 of the detector 7 to transmit the signal to the CPU 68. That

is, the circuit 73, for detecting a transmission signal and a response signal, transmits, to the body 12 of the detector 7, a command signal to read address to receive the address information; transmits, to the body 12 of the detector 7, a command signal to write address to receive new address information; and transmits, to the body 12 of the detector 7, an A/D conversion command to receive an analog value.

The printer 52 receives a printing command from the CPU 68 to print address information on the seals 54 applied to the surface of the seal sheet 53.

With reference to a flow chart shown in Fig. 8, the operation will now be described.

Initially, in step S1 the AC adapter 61 is inserted into a 100 V AC power source and the power supply switch 34 is switched on. When the included battery 62 is used, the AC adapter 61 is removed and the power supply switch 34 is switched on. As a result, the indication unit 67 is turned on for a predetermined time in step S2 so that the self-diagnosis is performed.

When address information is written, the slide switch 37 is switched to "ADDRESS" in step S3. In step S4 the writing key 39 is depressed. In step S5 the ten-key pad 41 is used to input writing address information. At this time, the segment indication portion 44 flashes to perform indication. In step S6 the CPU 68 transmits, to the connected body 12 of the detector 7, an address response requirement signal through the circuit 73 for detecting a transmission signal and a response signal and the connection terminals 74 and 75 to detect the current address. In step S7 the CPU 68 discriminates as to whether a normal response has been performed.

After the current address has been responded from the connected body 12 of the detector 7, the operation proceeds to step S8. In step S8 the CPU 68 transmits, to the body 12 of the detector 7, a writing command signal through the circuit 73 for detecting a transmission signal and a response signal and the connection terminals 74 and 75 so that new address is written to the non-volatile memory 26 of the body 12 of the detector 7. In the case of a detector of a type using the dip switch, no command recognition signal in response to the writing command signal is returned in step S9. Therefore, occurrence of an error is indicated in step S14. In step S10 address is retrieved. If new address has been responded, the address function is indicated on the segment indication portion 44 in step S12. If new address is not responded after the retrieval of the address has been performed, the operation proceeds to step S11 so that the operation returns to step S8 so as to perform a retrieval. If the new address is not rewritten though the retrieval has been performed, occurrence of an error is indicated in step S14.

In the case where address information items of a multiplicity of detectors are collectively set with serial numbers to be given, the + 1 key 42 is depressed when input using the ten-key pad 41 is performed in step S5. As a result, the inputting operation can be omitted.

If address information has been indicated in step S12, the address information is printed by the printer 52 in step S13. An output from the printer 52, that is, address information from the same is, as shown in Fig. 5, printed on a plurality of the seals 54 applied to the seal sheet 53. Therefore, the seal 54, on which address information has been printed, can be separated and applied to, for example, the reverse surface of the body 12 of the detector 7. Thus, occurrence of an error in transference can be prevented.

Since the + 1 key 42 is provided to collectively set the addresses of a multiplicity of detectors with the serial numbers given to the addresses as described above, the inputting operation using the ten-key pad 41 required whenever the address is set can be omitted. Thus, a multiplicity of addresses can be set in a short time.

Since the included battery 62 is provided to make the address setting unit 9 into a handy unit, it can easily be transported to a desired place in which the address setting operation will be performed. Since new address information can be read after the new address information has been set, the set address information can be confirmed.

If writing or reading of the address information or measurement of the analog value becomes an error, occurrence of the error is indicated. The indication of the occurrence of the error is cleared by the clear key 43.

When the address information written on the non-volatile memory 26 of the body 12 of the detector 7 is read so as to be confirmed, the slide switch 37 is switched to "ADDRESS" in step S3. In step S4 the test key 38 is depressed. As a result, the CPU 68 transmits, to the detector 7, an address information reading command signal through the circuit 73 for detecting a transmission signal and a response signal in step S17. In step S18 the CPU 68 discriminates as to whether or not address has been responded normally.

If the address has been responded normally, the CPU 68 causes the segment indication portion 44 to indicate the address information in step S19. If address has not been responded normally, the CPU 68 causes the segment indication portion 44 to indicate occurrence of an error in step S14. If the occurrence of an error has been indicated, the clear key 43 is depressed in step S15. Then, the indication is cleared in step S16.

If the test key 38 is depressed, the operation returns to step S17 so that addresses are retrieved. If the clear key 43 is depressed, the address indicated on the segment indication portion 44 is cleared. If no operation is performed for one minute, the indication on the segment indication portion 44 is automatically cleared.

When the body 12 of the detector 7 is tested, the slide switch 37 is switched to "ANALOG" and the body 12 of the detector 7 is connected to the connection portion 31 in step S3. In step S20 the test key 38 is depressed. As a result, the CPU 68 transmits, to the body 12 of the detector 7, an A/D conversion command

through the circuit 73 for detecting a transmission signal and a response signal in step S21. In step S22 the CPU 68 requires response of the analog value by polling.

In step S23 the CPU 68 receives a response signal from the body 12 of the detector 7 through the circuit 73 for detecting a transmission signal and a response signal to discriminate whether or not the response is normal. If normal response has been performed, the CPU 68 causes the segment indication portion 44 to indicate an analog value in step S24. If the body 12 of the detector 7 is abnormal, occurrence of an error is indicated on the segment indication portion 44 in step S14. If the occurrence of the error has been indicated, the clear key 43 is depressed in step S15. Then, the indication is cleared in step S16.

The measurement of the analog value of the body 12 of the detector 7 is performed for 5 seconds. If the time for the measurement is intended to be elongated, depressing of the + 1 key 42 within 5 seconds enables the time to be elongated by one minute. If no key is depressed, the indication of the analog value on the segment indication portion 44 is automatically turned off one minute after.

When the test of the terminator 8 is performed, the test cable 10 is connected to the terminator 8, and the slide switch 37 is switched to "TERMINATOR" in step S3. When the CPU 68 receives a terminator testing signal from the slide switch 37 in step S25, the CPU 68, at intervals of 5 seconds, transmits pulses for checking the terminator 8 to the terminator 8 through the terminator discrimination circuit 70. The reason for performing the test at the intervals of 5 seconds is to as possible prevent consumption of the included battery 62.

In step S25 the terminator discrimination circuit 70 supplies the pulses for checking the terminator 8 which exceed the zener voltage of the terminator 8. In step S26 the terminator discrimination circuit 70 uses clip voltage to discriminate whether or not the terminator 8 exists and uses a circuit current to detect the number of the terminators 8 and whether or not a resistor is connected. Specifically, if one terminator 8 is connected as show in Fig. 9A, the terminator discrimination circuit 70 discriminates the state being normal and transmits a normal result of the discrimination to the CPU 68. In step S27 the CPU 68 turns the OK lamp 47 on.

If the checking pulse voltage is not clipped and no electric current flows as shown in Fig. 9B, the terminator discrimination circuit 70 discriminates that the terminator 8 does not exist. In step S28 the terminator discrimination circuit 70 turn the NG1 lamp 48 on. If the checking pulse voltage is normally clipped and a large electric current flows as shown in Fig. 9C, the terminator discrimination circuit 70 discriminates that two or more terminators 8 and 8A are connected and turns the NG2 lamp 49 on in step S28. If the checking pulse voltage is not clipped and a large electric current flows as shown in Fig. 9D, the terminator discrimination circuit 70 discriminates that the terminator 8 does not exist and a re-

sistor 74 is connected and turns the NG3 lamp 50 on in step S28. If the checking pulse voltage is clipped and a further large electric current flows as shown in Fig. 9E, the terminator discrimination circuit 70 discriminates that the terminator 8 and the resistor 74 are connected and turns the NG4 lamp 51 on in step S28.

Although the structure of foregoing embodiment has all of the address setting function, the detector testing function and the terminator testing function, either of the detector testing function or the terminator testing function may be provided in addition to the address setting function.

Although the invention has been described in its preferred form with a certain degree of particularity, it is understood that the present disclosure of the preferred form can be changed in the details of construction and in the combination and arrangement of parts without departing from the spirit and the scope of the invention as hereinafter claimed.

Claims

1. An address setting unit for a fire detector for setting address to the fire detector which detects a call polling transmitted from a control panel so as to discriminate the self-address, said address setting unit for a fire detector comprising:
 - a detector connection portion for connecting the body of said detector provided with a memory for storing address information;
 - an address inputting portion for inputting the address information of said body of said detector;
 - an indication portion for indicating the address information; and
 - an address writing portion for writing the address information input from said address inputting portion on said memory of said body of said detector.
2. An address setting unit for a fire detector according to claim 1, wherein said detector connection portion is formed into an attaching substrate for use when said fire detectors are attached to a variety of portions in an architecture, said detector connection portion having metal connectors which can be received by metal connectors of said body of said detector.
3. An address setting unit for a fire detector according to claim 1 or 2, wherein said address inputting portion includes a ten-key pad for inputting the number to be given to the address information and a + 1 key for sequentially increasing the number to be given to the address.
4. An address setting unit for a fire detector according to any one of claims 1 to 3 further comprising:
 - a printer for printing out the address information; and
 - a printer control portion for causing said printer to print the address information if writing of the address information on said memory of said body of said detector by said address writing portion has been completed normally, wherein said printer prints the address information on a paper sheet having separable adhesive seals, and said adhesive seal, on which the address information has been printed, is separated and applied to said body of said detector.
5. An address setting unit for a fire detector according to any one of claims 1 to 4 further comprising:
 - a test key for instructing confirmation of the address information written on said memory of said body of said detector; and
 - an address reading portion for reading the address information from said memory of said body of said detector in accordance with the operation of said test key to indicate the read address information on said indication portion.
6. An address setting unit for a fire detector according to any one of claims 1 to 5 further comprising:
 - a mode switch for switching an address setting mode to a detector testing mode; and
 - a detector testing portion for requiring said body of said detector to transmit detected information when said mode switch has switched the mode to said detector testing mode to indicate, on said indication portion, the detected information transmitted from said body of said detector.
7. An address setting unit for a fire detector according to claim 6, wherein said body of said detector has an analog detector circuit for receiving an A/D conversion command to transmit a detected analog value, and said detector testing portion transmits the A/D conversion command to said body of said detector when said mode switch has been switched to said detector testing mode.
8. An address setting unit for a fire detector according to any one of claims 1 to 7 further comprising:
 - a test cable which can be connected to a terminator connected to a circuit in said detector;
 - a mode switch for switching the address setting mode to a terminator testing mode; and
 - a terminator discrimination portion for reading

the voltage of said circuit in a state where pre-determined test voltage is applied to said test cable when said mode switch has been switched to said terminator testing mode in a state where said test cable is connected to said terminator of said circuit in said detector. 5

9. An address setting unit for a fire detector according to claim 8, wherein said terminator discrimination portion discriminates a normal state or an abnormal state, such as non-connection or erroneous connection of said terminator, in accordance with the voltage of said circuit to indicate a result of the discrimination. 10

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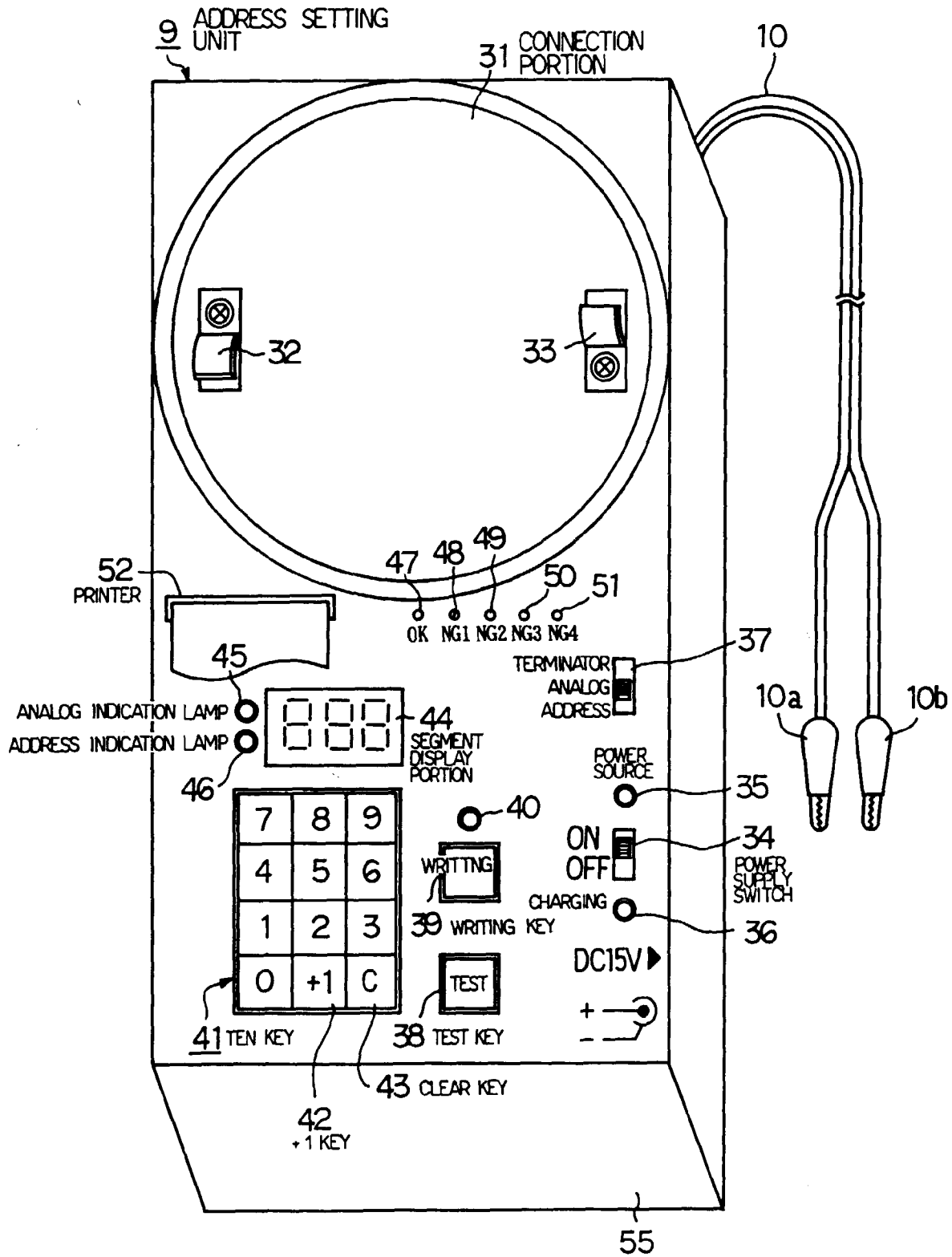
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FIG.1



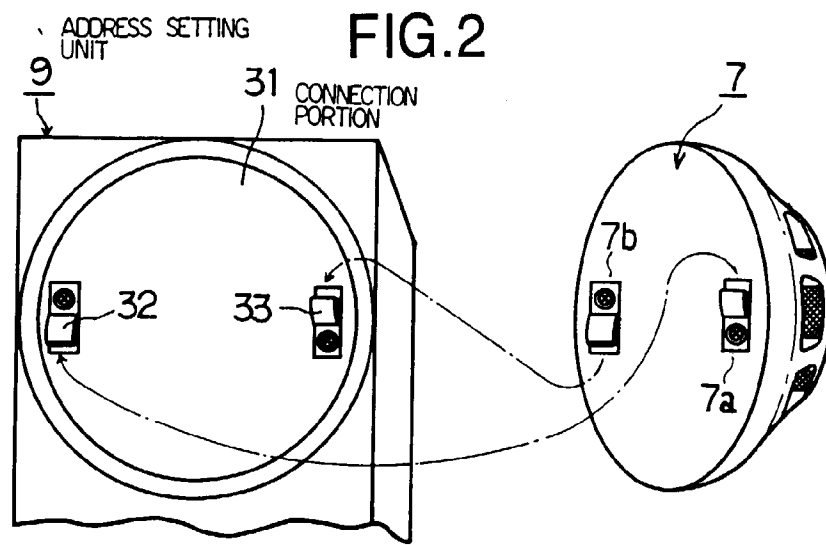


FIG.3

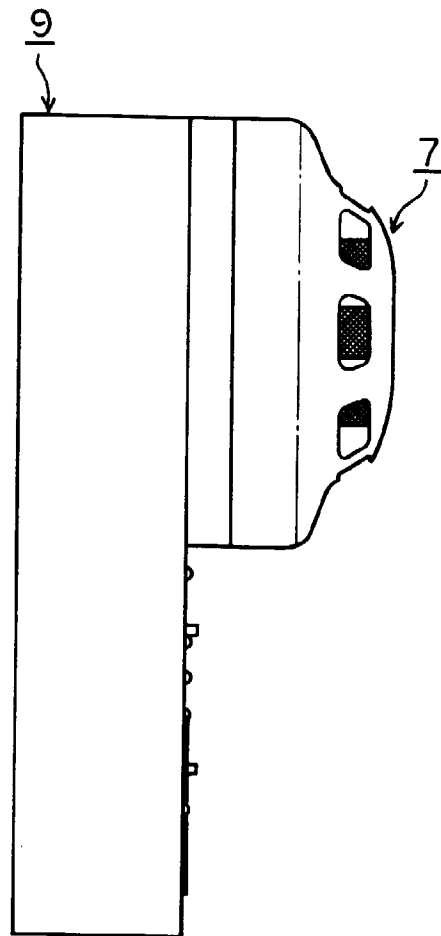


FIG. 4

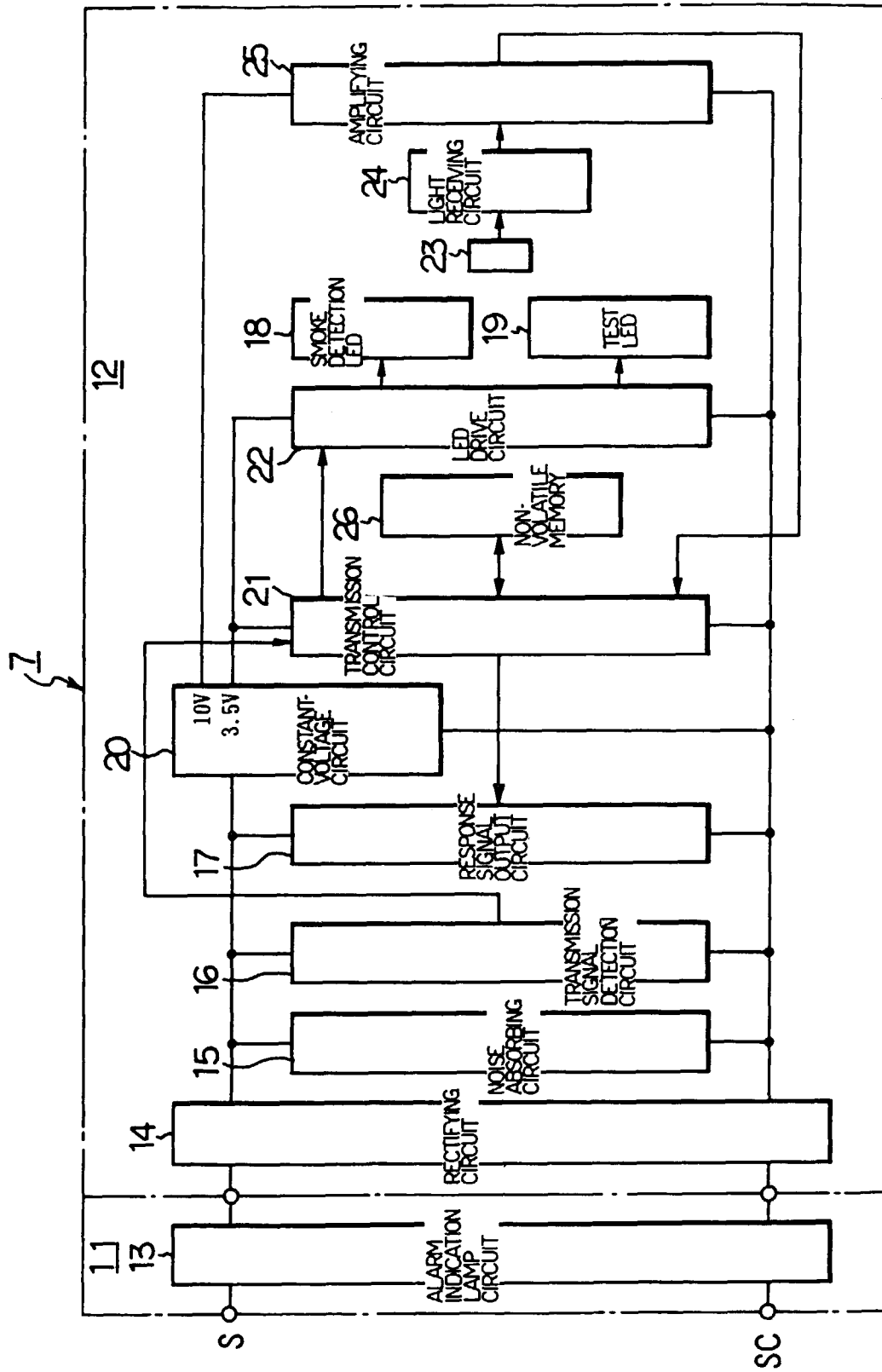


FIG.5

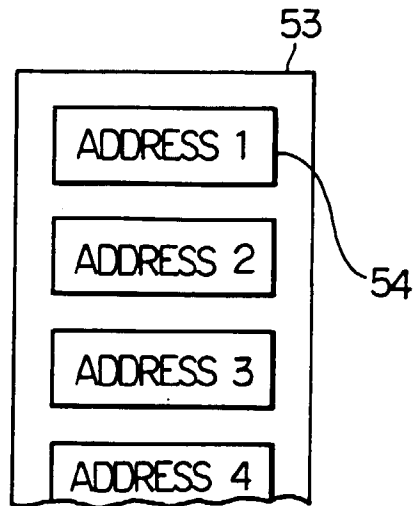


FIG.6

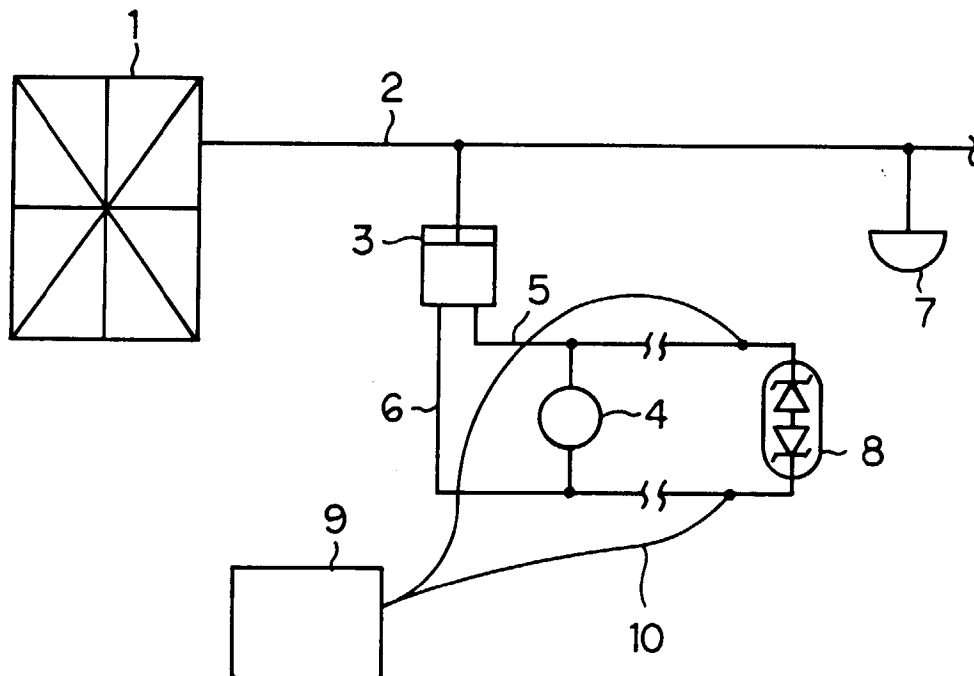


FIG. 7

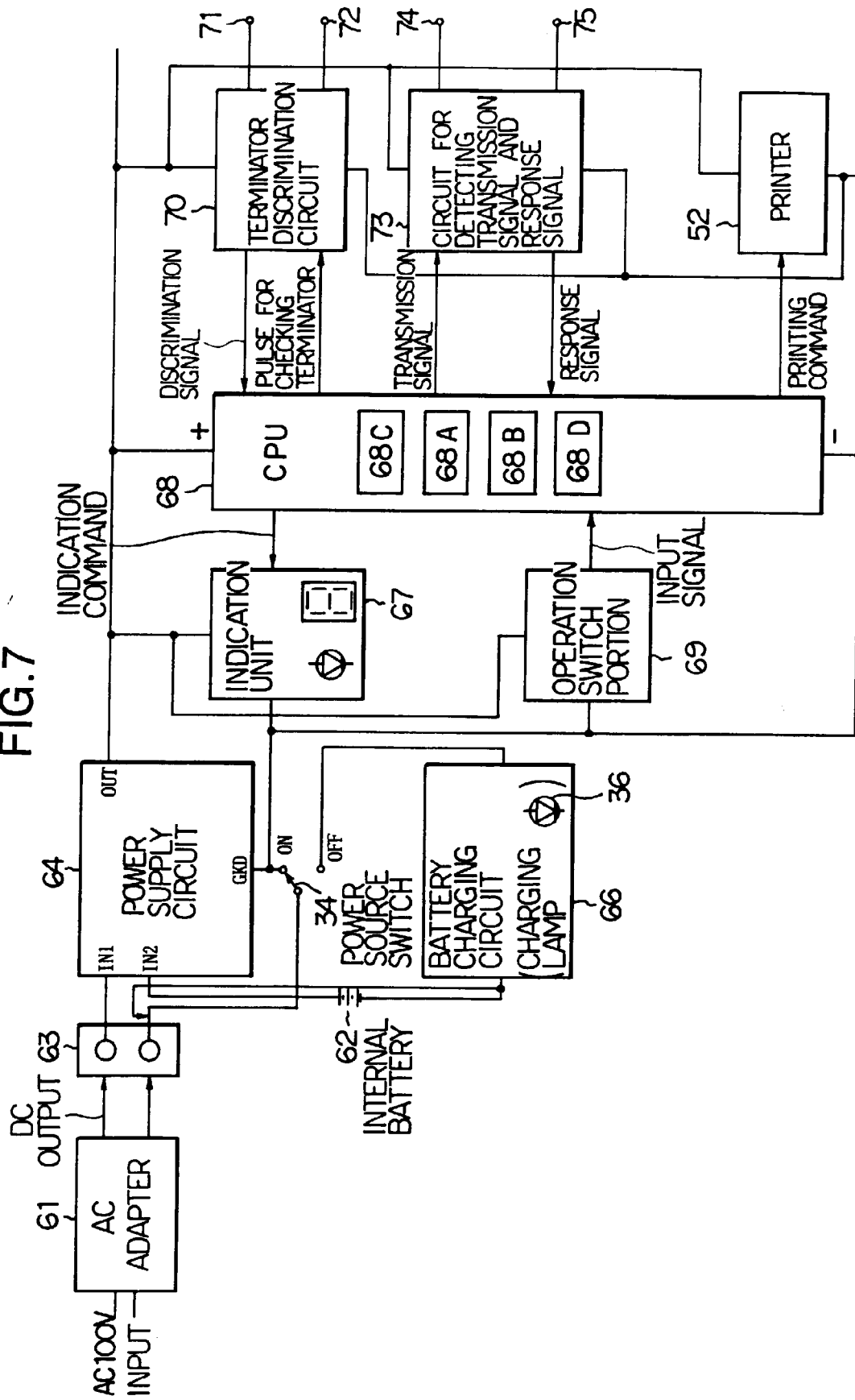


FIG.8

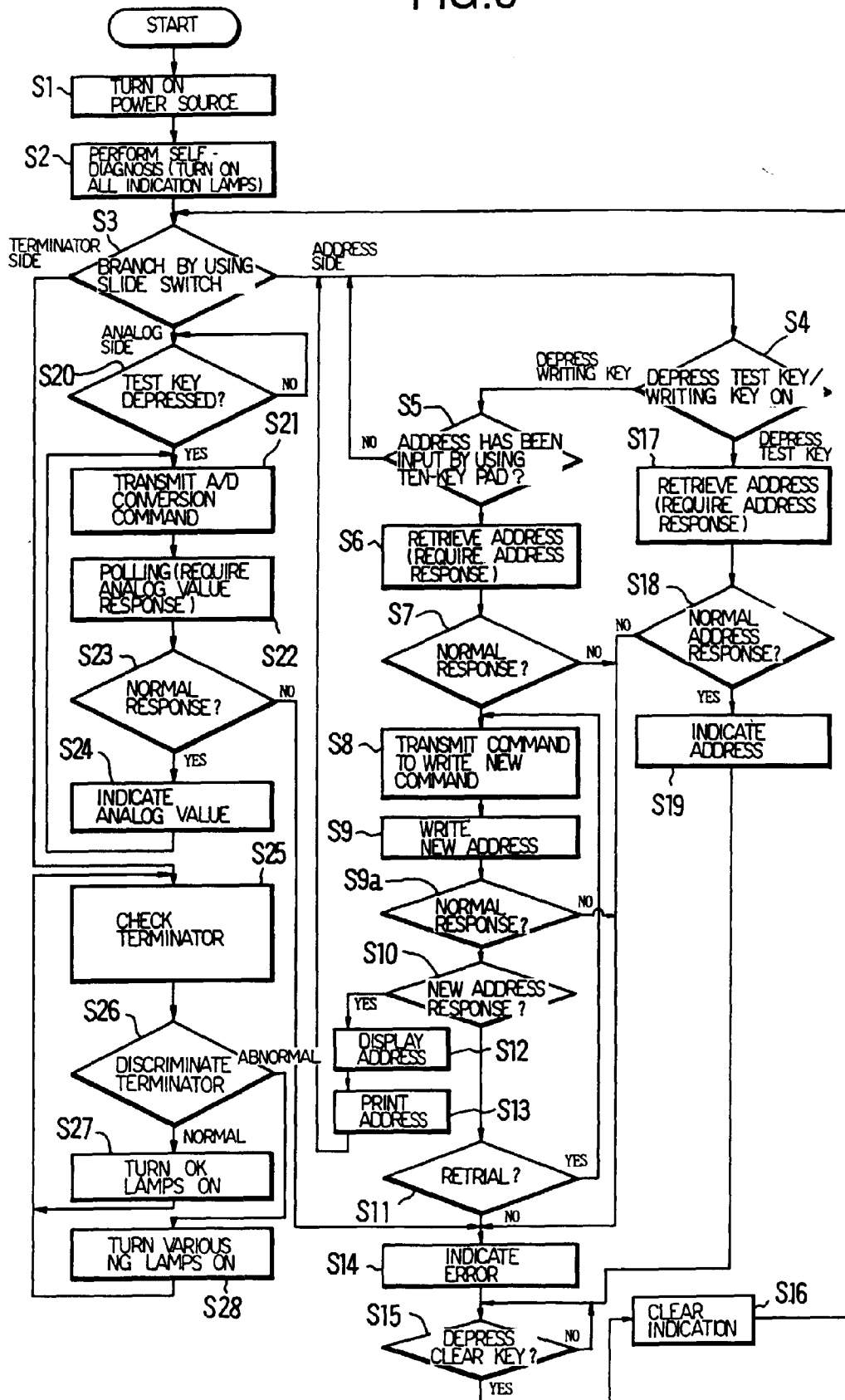


FIG.9

