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(54) A semiconductor substrate, devices having the same and a method of manufacturing the same

(57) A semiconductor substrate (1), devices comprising such a substrate, and a method of manufacturing them are disclosed. In particular, a method of processing the surface of a semiconductor substrate (1) comprises rotating the substrate (1), rotating a grinding wheel (6) about an axis (Z) which is substantially perpendicular to the axis of rotation of the substrate (X), and moving the axis of rotation of the wheel (Z) along an axis (Y) which is substantially perpendicular to the axis of rotation of the substrate (X) and the axis of rotation of the wheel (Z) to grind the substrate (1).

A processed substrate comprises a process-transformed layer having an undulated surface. The thickness of the process transformed layer at its minimum is in the range of 0.1 μm to 0.5 μm and/or the difference between the minimum and maximum height of the undulated surface is in the range of 0.3 μm to 3 μm.

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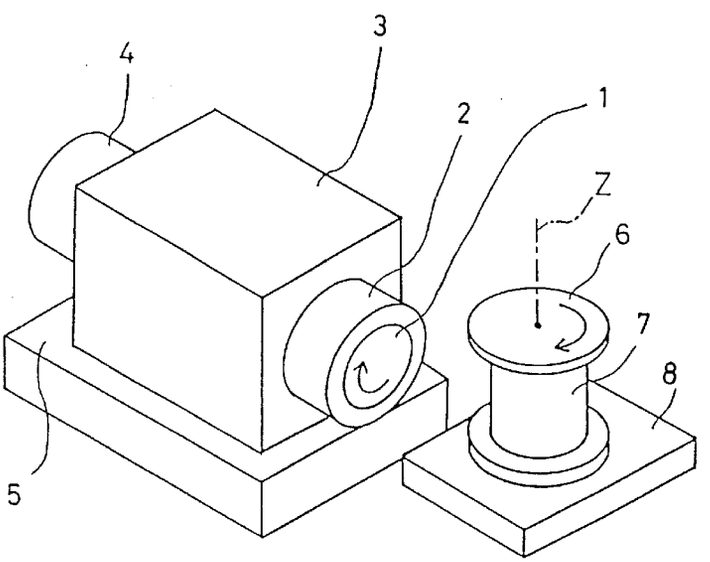

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Description

The present invention relates to semiconductor substrates and semiconductor devices utilizing the same, especially, semiconductor devices having a photoelectric conversion device, an MIS structure, or a Schottky diode structure, and a method of manufacturing the same.

There is a known method of processing the surface of a semiconductor substrate referred to as lapping wherein, as shown in Figure 12 of the accompanying drawings, a stool 30 and a semiconductor substrate 1 are put in a sun-and-planet motion in contact with each other with free abrasive grains provided therebetween.

Another possible method utilizes a cup grinding wheel. According to this method, as shown in Figure 13 of the accompanying drawings, a cup grinding wheel 31 and a semiconductor substrate 1 are positioned to face each other so that the outer circumference of the former and the rotational centre of the latter substantially coincide with each other, and a cup grinding wheel 31 is caused to cut into the semiconductor substrate 1 with the cup grinding wheel 31 and the semiconductor substrate 1 rotated in opposite directions.

With conventional methods, the following defects are encountered. When performed on a fragile material such as a semiconductor substrate, a lapping process results in breakage due to fragility which leaves innumerable cracks and a deep process-transformer layer. The method utilizing a cup grinding wheel wherein the contact area is large results in a heavy load, the fall of abrasive grains, and chips which lead to the generation of cracks and also leaves a deep process-transformed layer.

Figure 4 is a schematic sectional view showing the state of a surface of a semiconductor substrate obtained using a known processing method in which a deep process-transformed layer 36 is produced which extends from a surface 35 of the semiconductor substrate to the region indicated by the broken line. According to such known processing methods, the thickness of the process-transformed layer b is limited to about 1.5 μm and there will be irregularities (undulations) having an amplitude variation "a" of at least several micrometers.

In such known methods, therefore, a lapping process, acid washing, and polishing are repeated to perform mirror-finishing by removing the process-transformed layer as much as possible.

According to the present invention, a grinding process can be performed which involves less possibility of generation of a process transformed layer and reduces the thickness of a process-transformed layer to 0.1 μm without increasing the size of the device and without reducing processing efficiency, and such a processing method is applied especially to a semiconductor device having a photoelectric conversion device and an MIS structure to improve the efficiency of photoelectric conversion or to enhance the capacity of a capacitor.

According to one aspect of the present invention there is provided a method of processing the surface of a semiconductor substrate, comprising rotating the substrate; rotating a grinding wheel about an axis which is substantially perpendicular to the axis of rotation of the substrate; and moving the axis of rotation of the wheel along an axis which is substantially perpendicular to the axis of rotation of the substrate and the axis of rotation of the wheel to grind the substrate.

According to another aspect of the present invention there is provided a method of manufacturing a semiconductor device, comprising processing a semiconductor substrate according to the present invention and forming a semiconductor device utilising the processed semiconductor substrate.

According to a further aspect of the present invention there is provided a semiconductor substrate comprising a process-transformed layer having an undulated surface, characterised in that the thickness of the layer at its minimum is in the range of 0.1 μm to 0.5 μm.

According to a still further aspect of the present invention there is provided a semiconductor substrate having an undulated surface characterised in that the difference between the minimum and maximum surface height is in the range of 0.3 μm to 3 μm. According to yet another aspect of the present invention, there is provided an apparatus for processing the surface of a semiconductor substrate comprising means for rotating the substrate; a grinding wheel; means for rotating the grinding wheel about an axis which is substantially perpendicular to the axis of rotation of the substrate and means for moving the axis of rotation of the wheel along an axis which is substantially perpendicular to the axis of rotation of the substrate and the axis of rotation of the wheel to grind the substrate.

According to a preferred embodiment of the present invention, the thickness of a process-transformed layer on the surface of a semiconductor substrate is kept within the range from 0.1 μm to 0.5 μm as a first means.

As a second means, the amplitude of undulations of the surface of a semiconductor substrate is kept within the range from 0.3 μm to 3 μm.

As a third means, the amplitude of undulations of the surface of a substrate of a semiconductor device is kept within the range from 0.3 μm to 3 μm.

As a fourth means, the amplitude of undulations of the surface of a substrate of a semiconductor device having a photoelectric conversion device is kept within the range from 0.3 μm to 3 μm.

As a fifth means, the amplitude of undulations of the surface of a substrate of a semiconductor device having an MIS structure is kept within the range from 0.3 μm to 3 μm.

As a sixth means, the amplitude of undulations of the surface of a substrate of a semiconductor device having a separated-dielectric structure is kept within the range from 0.3 μm to 3 μm.

As a seventh means, the amplitude of undulations

of the surface of a substrate of a semiconductor device having a Schottky diode structure is kept within the range from 0.3 μm to 3 μm.

As an eighth means, the amplitude of undulations of the surface of an SO1 semiconductor substrate is kept within the range from 0.3 μm to 3 μm.

As a ninth means, the amplitude of undulations of the surface of a DW semiconductor substrate is kept within the range from 0.3 μm to 3 μm.

As a tenth means, the amplitude of undulations of the surface of an expitaxial semiconductor substrate is kept within the range from 0.3 μm to 3 μm.

As an eleventh means, a rotating semiconductor substrate is ground by the circumferential end face having a flat portion of a disc-shaped grinding wheel which is rotated about a moving rotational axis.

As a twelfth means, wet etching is performed using a solution after the above-described grinding.

As a thirteenth means, a semiconductor substrate of a photoelectric conversion device is processed using the above-described grinding method.

As a fourteenth means, a semiconductor substrate of a semiconductor device having a photodiode structure is processed using the above-described grinding method.

As a fifteenth means, a semiconductor substrate of a semiconductor device having an MIS structure is processed using the above-described grinding method.

As a sixteenth means, a semiconductor substrate of a semiconductor device having an MIS structure especially a charge-transfer device (CTD) is processed using the above-described grinding method.

As a seventeenth means, a semiconductor substrate of a semiconductor device having an MIS structure especially a DRAM is processed using the above-described grinding method.

As an eighteenth means, a separated-dielectric structure is formed by processing a semiconductor substrate using the above-described grinding method.

As a nineteenth means, a separated-dielectric structure is formed using the above-described grinding method in a semiconductor device especially a photodiode array such as an optical relay which has been subjected to dielectric separation.

As a twentieth means, a semiconductor substrate of a semiconductor device having a Schottky diode structure is processed using the above-described grinding method.

As a 21st means, an SOI substrate is particularly processed using the above-described grinding method.

As a 22nd means, a semiconductor substrate is processed using the above-described grinding method in a semiconductor device having an MIS structure especially a semiconductor device having a boosting circuit.

As a 23rd means, a semiconductor substrate is processed using the above-described grinding method in a photoelectric conversion semiconductor device having a light-receiving device portion constituted by a semiconductor substrate of a first conductivity type and an impurity region of a second conductivity type provided on the surface of said substrate and an electrode for applying a reverse voltage to the junction of a capacitor connected to said light-receiving device portion and said light-receiving device portion.

As a 24th means, a semiconductor device is manufactured using a semiconductor substrate wherein the thickness of a process-transformed layer on the surface thereof is 0.1 μm to 0.5 μm.

As a 25th means, a DW substrate is particularly used in the above-described grinding method.

As a 26th means, an epitaxial substrate is particularly processed using the above-described grinding method.

Embodiments of the present invention will now be described with reference to the accompanying drawings, of which:

Figure 1 is a schematic perspective view showing an embodiment of a method of grinding a semiconductor substrate according to the present invention;
Figure 2 is a conceptual diagram showing positional relationship between a semiconductor substrate 1 and a disc-shaped grinding wheel 6;
Figure 3 is a schematic sectional view showing the state of the surface of a semiconductor substrate processed according to the method of the invention;
Figure 4 is a schematic sectional view showing the state of the surface of a semiconductor substrate processed according to a known method;
Figure 5 is a schematic sectional view showing the state of the surface of a semiconductor substrate processed according to the method of the invention after a process-transformed layer thereon is removed;
Figure 6 is a schematic sectional view of a PIN photodiode which is a first embodiment of the present invention;
Figure 7 is a schematic sectional view of a solar battery which is a second embodiment of the present invention;
Figure 8 is a schematic sectional view of a solid-state camera device which is a third embodiment of the present invention;
Figure 9 is a schematic sectional view of a charge coupled device which is a fifth embodiment of the present invention;
Figure 10 is a schematic sectional view of a DRAM (dynamic random access memory) which is a fifth embodiment of the present invention;
Figure 11 is a circuit diagram of a DRAM which is a fifth embodiment of the present invention;
Figure 12 is a schematic perspective view showing a method of grinding a semiconductor substrate utilizing a lapping process;
Figure 13 is a schematic perspective view showing

a method of grinding a semiconductor substrate using a cup grinding wheel;

Figure 14 is a circuit diagram of an optical relay which is a sixth embodiment of the present invention;

Figures 15A-15C illustrate steps for manufacturing a photodiode array structure which has been subjected to dielectric separation according to the processing method of the invention;

Figure 16 illustrates steps for manufacturing a photodiode array structure which has been subjected to dielectric separation according to the processing method of the invention;

Figures 17A-17C illustrate manufacturing steps in a case wherein the grinding method according to the present invention is used for an SOI (silicon on insulator) substrate;

Figures 18A-18C illustrate manufacturing steps in a case wherein the grinding method according to the present invention is used for an SOI substrate to perform device separation thereon;

Figure 19 is a schematic sectional view showing a Schottky diode which is a seventh embodiment of the present invention;

Figure 20 is a circuit diagram of a semiconductor device having a boosting circuit;

Figure 21 is a schematic sectional view of a semiconductor device having a boosting circuit which is an eighth embodiment of the present invention;

Figure 22 is a schematic sectional view of a semiconductor device having a boosting circuit which is a ninth embodiment of the present invention;

Figure 23 is a schematic sectional view of a semiconductor device having a boosting circuit which is a tenth embodiment of the present invention;

Figure 24 is a schematic sectional view of a photoelectric conversion semiconductor device used for purposes such as the detection of radiation which is an eleventh embodiment of the present invention;

Figures 25A-25B illustrate manufacturing steps in a case wherein the grinding method of the invention is used for a DW (diffusion wafer) substrate; and

Figures 26A-26B illustrate manufacturing steps in a case wherein the grinding method of the invention is used for an epitaxial substrate.

An embodiment of the present invention will now be described in detail with reference to the drawings.

Figure 1 is a schematic perspective view showing a method of grinding a semiconductor substrate according to an embodiment of the present invention.

A semiconductor substrate 1 is fixed on a main spindle 3 of a machine tool by a chuck 2, and the main spindle 3 of the machine tool is rotated by a motor 4.

The main spindle 3 of the machine tool is provided on a head stock 5 and is moved along an X-axis by a servo motor or the like together with the head stock 5.

A disc-shaped grinding wheel 6 is rotated by a grinding wheel spindle 7 about a Z-axis by means of a motor, and a grinding wheel head 8 on which this grinding wheel spindle 7 is fixed is reciprocated by a servo motor or the like in the direction of a Y-axis which is orthogonal to the X-axis and Z-axis.

Figure 2 is a conceptual diagram illustrating the positional relationship between the semiconductor substrate 1 and the disc-shaped grinding wheel 6 wherein the semiconductor substrate 1 is brought into contact with the outer circumferential end face of the disc-shaped grinding wheel 6 as a result of the movement of the head stock 5 along the X-axis.

The rotation of the machine tool main spindle 3 caused by the motor 4 results in the rotation of the semiconductor substrate 1, and the rotation of the grinding wheel spindle 7 causes the disc-shaped grinding wheel 6 to rotate.

When the disc-shaped grinding wheel 6 reciprocates along the Y-axis along with the grinding wheel spindle and the disc-shaped grinding wheel 6 moves along the X-axis together with the head stock 5, the semiconductor substrate 1 is ground in accordance with the movement in the direction of the X-axis.

According to the present invention, the thickness of the disc-shaped grinding wheel is 15 - 20 mm which substantially corresponds to one chip (device) on a semiconductor substrate. Since grinding is performed at line contact of such a width, the processing load is smaller than that in grinding on a surface contact basis.

Processing efficiency is very low when the width of the disc-shaped grinding wheel is 10 mm or less while a width of 20 mm or more results in problems such as an increase in the size of the device due to an increase in the processing load.

The method according to the present invention suppresses the generation of cracks and the like because the contact time per one abrasive grain of the grinding wheel is short and hence chips are effectively ejected.

Further, since the cut-in angle of the grinding wheel is small, it is possible to perform grinding with reduced possibility of breakage due to fragility.

In conventional processing methods wherein a process-transformed layer of several micrometers is produced, mirror finishing is performed through repeated acid washing and polishing to remove the process-transformed layer as much as possible.

A semiconductor substrate processed according to a process of the invention was subjected to angle lapping and selective etching using a wet type chemical etchant which is a mixture of $HN0_3$ HF_1 and CH_3COOH or water and was examined for the presence of micro cracks and defects using a sectional transmission electron microscope. As in the schematic sectional view of Figure 3 showing the state of the surface of the semiconductor substrate processed according to a method of the present invention, appropriate processing conditions allowed the thickness b of a process-transformed layer 36 (i.e. the region damaged by shaping) in the re-

gion indicated by the broken line from the surface 35 of the semiconductor substrate to be reduced to 0.1 μm and allowed an amplitude variation a of irregularities (undulations) to be reduced to 0.3 μm.

Although a process-transformed layer is a region having micro cracks and defects produced by angle lapping and selective etching as described above, it is preferable that the presence of micro cracks and defects is further observed using a sectional transmission electron microscope.

For example, angle lapping and selective etching are described in American Society for Testing and Materials (ASTM) F 950 in detail and reference can be made also to Japanese Industrial Standard (JIS) H 0609.

Irregularities (undulations) having a long period on the surface are normally referred to TTV (total thickness variation), are at a level which can be measured using methods on a mechanical contact basis, and are described in detail in ASTM F 533, JIS H 0611, etc.

A process-transformer layer up to 0.5 μm is on a level which can be easily removed by oxidation followed by etching of the oxide film. In this case, the irregularities (undulations) having a long period on the surface can be maintained almost as they are, unlike polishing, and a semiconductor substrate having a process-transformed layer of 0.1 μm to 0.5 μm thickness is very useful.

Irregularities having a long period on the surface can be varied up to about 3 μm depending on the size of the abrasive grains and processing speed.

Figure 5 is a schematic section showing the state of the surface of a semiconductor substrate processed according to a method of the present invention which has been etched or oxidized and the process-transformed layer of which has been removed by etching the oxide layer. As illustrated, a semiconductor substrate having a large surface area without any process-transformed layer has been obtained.

However, since a process-transformed layer can be expanded as a result of oxidation when the etching of the oxide layer is performed in an attempt to remove the process-transformed layer, it is preferable that the process-transformed layer is removed or made thinner in advance by means of wet type chemical etching.

While comparable methods for improving the efficiency of a solar battery by forming irregularities on the surface thereof include the use of anisotropic etching or the like, the present method makes it possible to form irregularities on the surface quite easily.

Such a semiconductor substrate is very useful because a photoelectric conversion device having high conversion efficiency or a semiconductor device having a large apparent MIS (metal insulator semiconductor) capacitor per unit area can be obtained from it.

For example, in photoelectric conversion devices such as photodiodes, phototransistors, and solar batteries, apparent conversion efficiency is improved as a result of an increase in the surface area (when the chip size is kept constant).

Figure 6 is a schematic sectional view of a PIN photodiode, which is excellent especially in linearity and response speed among photodiodes, according to a first embodiment of the present invention relating to photoelectric transfer devices. A P^+ type impurity region 11 and an N^+ type impurity region 12 are formed on an N^- type semiconductor substrate 10 of a low resistivity index, and an N^+ type impurity region 13 is formed also on the rear side. The width of the depletion layer can be greatly varied depending on the reverse voltage, and the use of the N- type semiconductor substrate processed according to the method of the invention improves the conversion efficiency.

Figure 7 is a schematic sectional view of a solar battery which is a second embodiment of the present invention relating to photoelectric transfer devices. A P^+ type impurity region 11 and an N^+ type impurity region 12 are formed on an N type semiconductor substrate 13, and the use of the N type semiconductor substrate processed according to the method of the invention improves the conversion efficiency.

Figure 8 is a schematic sectional view of a solid-state camera device having a MOS IC (metal-oxide-semiconductor integrated circuit) and a photodiode as a light-receiving portion and consisting of an N^+ type impurity region 16, a P^+ type impurity region 17, an X gate 18, a Y gate 19, a P^+ type impurity region 20, and a drain 21 provided on an N type semiconductor substrate 15. The use of the N type semiconductor substrate 15 processed according to the method of the invention improves the conversion efficiency of the light-receiving portion constituted by the photodiode in which the P^+ type impurity region 17 is formed.

While an N type semiconductor substrate is used in the above-described examples, it goes without saying that a P type semiconductor substrate provides the same effect.

In a semiconductor device having an MIS structure, an MIS capacitor per unit area can be improved by the use of a semiconductor substrate processed according to a method of the invention.

Figure 9 is a schematic sectional view of one type of charge-transfer device according to a fifth embodiment of the present invention. A semiconductor substrate 25 processed according to a method of the invention is used; an oxide film 26 is formed thereon, and a polysilicon electrode 27 and a metal electrode 28 are further formed thereon. The use of the semiconductor substrate processed according to a method of the invention allows the amount of accumulated electric charge to be increased.

Figure 10 is a schematic sectional view of an example of a DRAM according to a fifth embodiment of the present invention. It includes a metal data line 47 and a polysilicon ward line 46 provided on a P^- type semiconductor substrate 40, and a capacitor is formed by a polysilicon plate electrode 43, an oxide film 44, and an in-

version layer 45.

Figure 11 is a circuit diagram of the above-described DRAM wherein a one-transistor type cell is constituted by one MOS transistor and one MOS capacitor (electrostatic capacity). The greater the signal obtained, the larger the capacity of the capacitor. In order to allow finer configurations, the capacity per unit area of the capacitor must be increased.

For the capacitor which utilizes a P^- type semiconductor substrate processed according to a method of the invention and which is formed by the polysilicon plate electrode 43, oxide film 44, and inversion layer 45, the capacity per unit area can be increased to obtain a large signal amount.

Although a MOS capacitor utilizing thermally oxidized $Si0_2$ having excellent characteristics is normally used as a dielectric for an MIS capacitor, it goes without saying that other substances having a high dielectric constant such as CVD $Si0_2$ and Si_3N_4 or multi-layer structures such as $Si0_2$-Si_3N_4-$Si0_2$ are also effective.

Figure 14 is a circuit diagram of an optically driven semiconductor relay (optical relay) constituted by an LED 75, a photoelectric conversion device 76, and a MOSFET 77. The photoelectric conversion device has a separated-dielectric photodiode array structure.

Performance can be improved by forming the separation of the dielectric using a processing method according to the present invention.

Figure 15A-15C illustrate steps for manufacturing a separated-dielectric photodiode array structure according to a processing method of the invention.

As shown in Figure 15A, a groove 52 is formed on a silicon substrate 50 having a N^+ type impurity region 51 formed thereon by means of anisotropic etching, RIE (reactive ion etching) or the like; an insulation film 53 is formed by means of thermal oxidation, and a polysilicon layer 54 is formed thereon using CVD.

Alternatively, as shown in Figure 16, a $Si0_2$ layer is formed on the thermally oxidized insulation film 53 using spin-on glass or CVD; etching (etch-back) is performed thereafter to form a flattening layer 55; and a silicon substrate 57 is laminated thereon.

Next as shown in Figure 15B, the initial silicon substrate 50 is ground using the method of the invention to form a single crystal silicon island 56 which has been subjected to dielectric separation. Then, predetermined devices, for example with impurity regions 11 and 12, are formed as shown in Figure 15C.

At this time, since the process-transformed layer is small, there is no need for polishing and the efficiency (capacity in the case of an MIS capacitor) of the photodiode thus formed is improved.

Figures 17A-17C illustrate steps for manufacturing in a case wherein the grinding method according to the present invention is used for an SOI substrate.

As shown in Figure 17A, an insulation film 53 is formed on a silicon substrate 57 using thermal oxidation; a silicon substrate 50 manufactured using an FZ (floating zone) process or the like is laminated thereon to fabricate an S0I substrate; and, thereafter, the laminated silicon substrate 57 is ground according to the grinding method of the invention to a predetermined thickness as shown in Figure 17B.

Next, as shown in Figure 17C, a LOCOS (local oxidation) oxide film 58 for separating devices is formed so that it reaches the insulation film 53, thereby performing dielectric separation to form predetermined devices having, for example, a semiconductor substrate 10 and impurity region 11.

Figures 18A-18C illustrate steps for manufacturing in a case in which device separation is performed on an SOI substrate using a grinding method according to the present invention.

As shown in Figure 18A, a single crystal silicon island 60 is formed on an S01 substrate 59 by means of etching or the like, and an oxide film 61 is formed on the surface thereof.

Next, as shown in Figure 18B, a polysilicon layer 62 is deposited using CVD (chemical vapour deposition).

Thereafter, as shown in Figure 18C, separation is carried out by grinding according to the grinding method of the invention.

Then, predetermined devices may be formed as shown in Figure 15C for example.

Figure 19 is a schematic sectional view showing a Schottky diode according to a seventh embodiment of the present invention, in which an N^+ type impurity region 71 is formed on a surface of an N^- type semiconductor substrate 70 ground according to the grinding method of the invention, an N^+ type impurity region 72 is formed also on the opposite side, a Schottky electrode 73 of a Schottky metal such as Al, W, Pt, etc. is formed in direct contact with the N^- type semiconductor substrate, an ohmic electrode 74 is formed in contact with the N^+ type impurity region 72, and a Schottky junction is formed by a Schottky electrode 73.

The use of a semiconductor substrate ground according to a grinding method of the invention increases the bonding area of the Schottky junction, thereby allowing the forward voltage V_F (a forward voltage required to obtain a predetermined forward current) to be decreased.

Such a Schottky diode having a small forward voltage V_F is quite useful as a switching device, a bi-directional gate circuit which is a combination of four Schottky diodes, a balance modulator, a double-balance modulator, or a ring modulator.

Figure 20 is a circuit diagram of a semiconductor device having a boosting circuit which is essentially constituted by a rectifying device 88 and a capacitor 89. Although Figure 20 shows a diode as the rectifying device, it may be replaced by a transistor. The diode may be either PN junction or Schottky junction type.

Figure 21 is a schematic sectional view of a semiconductor device having a boosting circuit according to an eighth embodiment of the present invention, in which

a PN junction is provided as a rectifying device. The PN junction as a rectifying device and a capacitor are formed on separate islands utilizing silicon islands 80 which are P type impurity regions made of silicon and which have been subjected to device-separation according to a method as shown in any of Figures 15 through 18, and a capacitor electrode 81 and a capacitor insulation film 82 are formed in the capacitor portion. For example, the structure may have been manufactured according to a method such as that shown in Figure 17, in which the structure is provided with a silicon substrate 218 and an insulator film 219 and in which device separation is achieved by the provision of a LOCOS oxide film 217. In the structure shown, the rectifying portion has P^+ impurity regions 211 and 213 and an $N^{\pm}$ impurity region 212, and the capacitor has P^+ impurity regions 214 and 216 and a P^+ impurity region which isolates the P^+ impurity region 214 from the P^+ impurity region 216 ($P^{\pm}$ indicates an impurity concentration P greater than P^- and less than P^+). Device separation according to an inventive method, such as any of those shown in Figures 15 through 18, allows the capacity to be increased, thereby increasing the boosting voltage.

Figure 22 is a schematic sectional view of a semiconductor device having a boosting circuit according to a ninth embodiment of the present invention and in which a PN junction and a capacitor are fabricated on a single silicon island 80 which is an N type impurity region. In the structure shown, a PN junction is formed by anode electrode 221, which contacts a P^+ type impurity region 224, and cathode electrode 223, which contacts an N^+ type impurity region 225. A capacitor is formed by capacitor electrode 81, capacitor insulation film 82 and N^+ type impurity region 222. The cathode electrode 223 is also used as a capacitor electrode for contacting the N^+ type impurity region 222.

Figure 23 is a schematic sectional view of a semiconductor device having a boosting circuit according to a tenth embodiment of the present invention and in which transistors are used as rectifying devices, P^- type wells 86 are formed on an N type semiconductor substrate 85 ground according to a grinding method of the invention, the transistors are fabricated therein, and a capacitor insulation film 82 is formed on a LOCOS oxide film 87 between the wells with capacitor electrodes 81 interposed therebetween.

Even in such a case, the shape of the surface of the LOCOS oxide film 87 is well reproduced on the capacitor electrode 81 and capacitor insulation film 82 to increase the capacity.

Figure 24 is a schematic sectional view of a photoelectric conversion semiconductor device mainly used for purposes such as the detection of radiation according to an eleventh embodiment of the present invention and in which a multiplicity of P^+ type impurity regions 92 as impurity regions of a second conductivity type in the form of strips are formed on a surface of an N^- type semiconductor substrate 91 ground according to a grinding method of the invention as a semiconductor substrate of a first conductivity type, and an N^+ type impurity region 93 is formed on the opposite side.

In this case, a two-dimensional configuration can be provided by forming a multiplicity of N^+ type impurity regions in the form of strips like the P^+ type impurity regions so that they are orthogonal to the P^+ type impurity regions.

On the P^+ type impurity regions 92, a capacitor insulation film consisting of three layers, i.e. a $Si0_2$ layer 94, a Si_3N_4 layer 95, and a $Si0_2$ layer 96, and a capacitor electrode 97 made of polysilicon are formed to perform capacitive reading (the structure on the N^+ type impurity region will be the same as that on the P^+ type impurity regions if the N^+ type impurity region is provided in the form of strips).

Further, an Al electrode 98 for applying a reverse voltage is formed on the P^+ type impurity regions. it applies the reverse voltage to expand the depletion layer through a high resistance portion 99 made of silicon, thereby allowing the efficiency of the detection of radiation and the like to be improved.

The capacity of a capacitor portion for reading can be increased by processing a semiconductor substrate to be used for such a semiconductor device using a grinding method of the invention.

Since a substrate processed using a grinding method of the invention has an improved heat dissipation capacity, such a substrate is advantageous when used in a bipolar transistor or diode which is a vertical device (a current is applied to the substrate surface vertically) consuming high power referred to as a power semiconductor device.

Such a semiconductor device utilizes a substrate having a high resistance portion formed on a low resistance portion. Such a substrates include DW (diffusion wafer) substrates and epitaxial substrates to which the present invention can be applied.

Figures 25A-25B illustrate manufacturing steps in a case wherein a grinding method of the invention is used for a DW substrate.

As shown in Figure 25A, a high impurity region 101 having low resistance is formed on a high resistance substrate 100. In this case, since the high impurity region 101 is formed on both sides, the high impurity region on one side is removed as shown in Figure 25B. The use of a grinding method of the invention leaves a surface having irregularities of 0.3 μm to 1 μm formed thereon, and a power semiconductor device formed on such a DW substrate will exhibit an excellent heat dissipation capacity.

Figures 26A-26B illustrate manufacturing steps in a case wherein a grinding method of the invention is used for an epitaxial substrate. As shown in Figure 26A, a high resistance epitaxial layer 106 is formed on a low resistance substrate 105 on an epitaxial growth basis.

In this case, a projection referred to as a hillock 107 grows on the surface of the epitaxial layer 106.

According to the present invention, the epitaxial layer is ground to a predetermined thickness using a grinding method of the invention, which also results in removal of the hillock as shown in Figure 26A. A power semiconductor device formed on such an epitaxial substrate will exhibit an excellent heat dissipation capacity.

As described above, the present invention makes it possible to provide a semiconductor substrate having a small process-transformed layer which can be used, amongst other things, to obtain a photoelectric conversion device of high conversion efficiency or a semiconductor device having a large apparent MIS capacitor per unit area and a power semiconductor device having an excellent heat dissipation capacity.

In particular, the invention provides a photoelectric conversion device of high conversion efficiency and a semiconductor device having a large capacitor capacity in the thickness of a process-transformed layer which is small. Further, a rotating semiconductor substrate is ground by the circumferential end face of a disc-shaped grinding wheel which is rotated about a moving rotational axis.

The aforegoing description has been given by way of example only and it will be appreciated by a person skilled in the art that modifications can be made without departing from the scope of the present invention.

Claims

1. A method of processing the surface of a semiconductor substrate (1) comprising:

   rotating the substrate (1);
   rotating a grinding wheel (6) about an axis (Z) which is substantially perpendicular to the axis of rotation of the substrate (X); and
   moving the axis of rotation of the wheel (Z) along an axis (Y) which is substantially perpendicular to the axis of rotation of the substrate (X) and the axis of rotation of the wheel (Z) to grind the substrate (1).

2. A method as claimed in claim 1, wherein the substrate is processed to comprise a layer (36) having an undulated surface (35), and thickness (b) at its minimum in the range of 0.1 μm to 0.5 μm.

3. A method as claimed in claim 1, wherein the substrate is processed to have an undulated surface (35), the difference (a) between the minimum and maximum height of which is in the range of 0.3 μm to 3 μm.

4. A method as claimed in claim 2, wherein the substrate is processed such that the difference (a) between the minimum and maximum heights of the undulated surface (35) is in the range of 0.3 μm to 3 μm.

5. A method as claimed in any preceding claim further comprising etching the substrate subsequent to grinding.

6. A method of manufacturing a semiconductor device, comprising:

   processing a semiconductor substrate (1) according to the method of any preceding claim; and
   forming a semiconductor device utilising the processed semiconductor substrate (1).

7. A method as claimed in claim 6, wherein a photoelectric conversion device is formed.

8. A method as claimed in claim 7, wherein the photoelectric conversion device has a photodiode structure.

9. A method as claimed in claim 7, wherein the photoelectric conversion device is a solar battery.

10. A method as claimed in any of claims 7 to 9, wherein the photoelectric conversion device has a light-receiving portion constituted by a semiconductor substrate of a first conductivity type and an impurity region of a second conductivity type provided on a surface of the substrate and an electrode for applying a reverse voltage to the junction of a capacitor connected to the light-receiving device portion, and to the light-receiving device portion.

11. A method as claimed in any of claims 6 to 10 wherein the semiconductor device formed comprises a Schottky diode.

12. A method as claimed in any of claims 6 to 11, wherein t he semiconductor device formed has an MIS structure.

13. A method as claimed in any of claims 6 to 12, wherein the semiconductor device formed comprises a charge-transfer device.

14. A method as claimed in any of claims 6 to 13, wherein the semiconductor device formed comprises a DRAM.

15. A method as claimed in any of claims 6 to 14, wherein the semiconductor device formed comprises a photodiode array which has been subjected to dielectric separation.

16. A method as claimed in any of claims 6 to 15, wherein the semiconductor device formed comprises a

boosting circuit.

17. A method as claimed in any preceding claim, wherein the substrate processed is a DW substrate.

18. A method as claimed in any of claims 1 to 16, wherein the substrate processed is an epitaxial substrate.

19. A method as claimed in any of claims 1 to 16, wherein the substrate processed is an SOI substrate.

20. A semiconductor substrate comprising a process-transformed layer (36) having an undulated surface (35), characterised in that the thickness (b) of the layer at the minimum is in the range of 0.1 μm to 0.5 μm.

21. A semiconductor substrate (36) having an undulated surface (35) characterised in that the difference (a) between the minimum and maximum surface heights is in the range of 0.3 μm to 3 μm.

22. A semiconductor substrate as claimed in claim 20, wherein the difference (a) between the minimum and maximum height of the undulated surface (35) is in the range of 0.3 μm to 3 μm.

23. An apparatus for processing the surface of a semiconductor substrate (1), comprising:

means (3,4) for rotating the substrate (1);
a grinding wheel (6);
means (7) for rotating the grinding wheel (6) about an axis (Z) which is substantially perpendicular to the axis of rotation of the substrate (X); and
means for moving the axis of rotation of the wheel (17) along an axis (Y) which is substantially perpendicular to the axis of rotation of the substrate (X) and the axis of rotation of the wheel (Z) to grind the substrate (1).

24. A semiconductor substrate comprising a semiconductor substrate (1) and a process-transformed layer (36) on the surface of the semiconductor substrate (1) wherein a thickness (b) having micro cracks thereon is 0.1 μm to 0.5 μm.

25. A semiconductor substrate comprising a semiconductor substrate (1) and a surface (35) on the semiconductor substrate wherein an amplitude (a) of undulations of the surface thereof as total thickness variation is 0.3 μm to 3 μm.

26. A semiconductor device comprising a semiconductor substrate (1) and an amplitude (a) of undulations of the semiconductor substrate thereof as total thickness variation is in the range from 0.3 μm to 3 μm.

27. A method of manufacturing a semiconductor device comprising the steps of rotating a disc-shaped grinding wheel (6) having a flat portion at a circumference thereof, rotating a semiconductor substrate (1), moving the rotational axis (Z) of said grinding wheel (6), and grinding said semiconductor substrate (1) by an end face of the grinding wheel (6).

28. A method of manufacturing a semiconductor device characterized in that a separated-dielectric structure is formed by grinding a rotating semiconductor substrate (1) using an end face having flat portion at the circumference of a disc-shaped grinding wheel (6) which is rotated about a moving rotational axis (Z).

FIG. 1

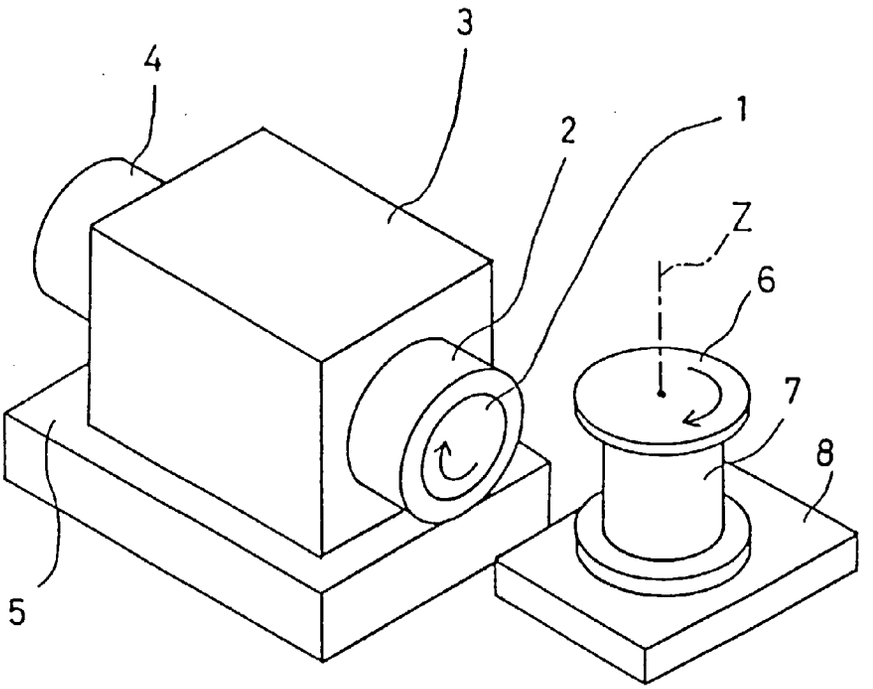

FIG. 2

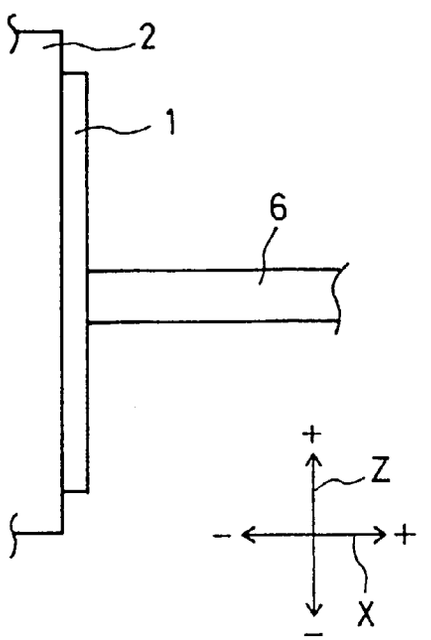

FIG. 3

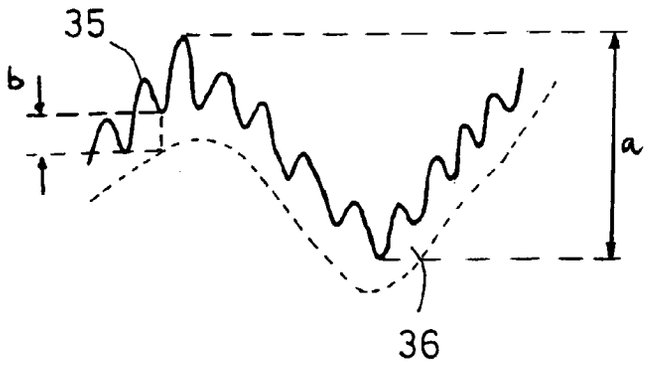

FIG. 4

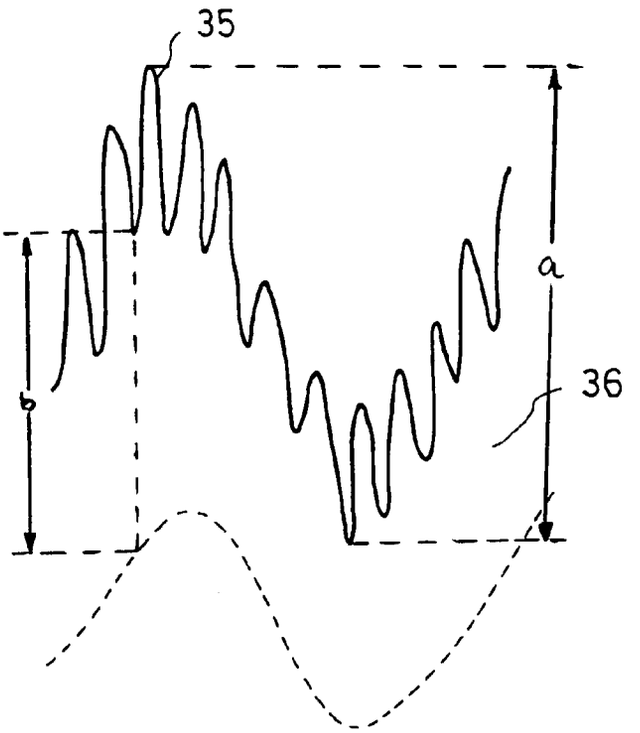

FIG. 5

FIG. 6

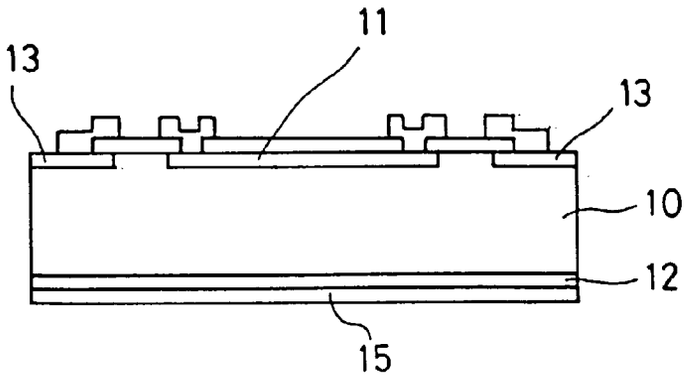

FIG. 7

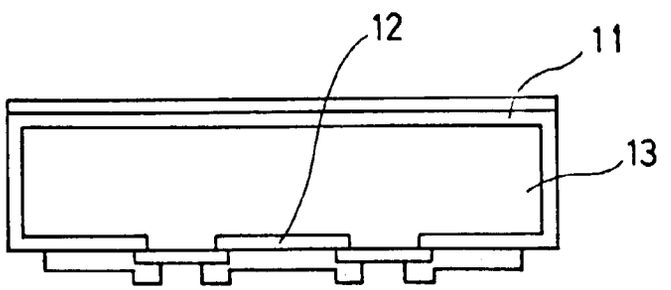

FIG. 8

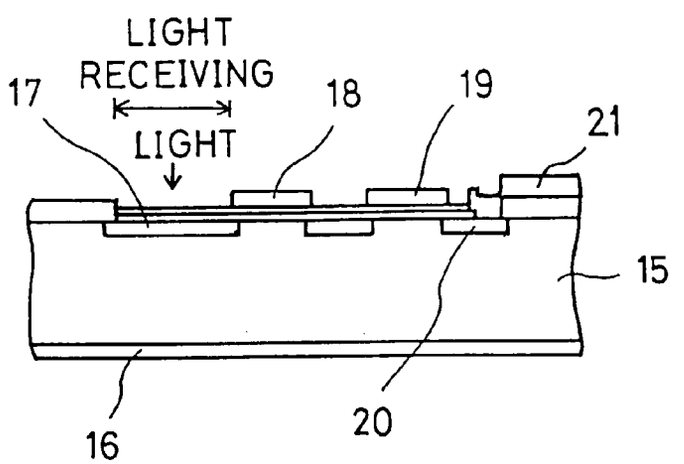

FIG. 9

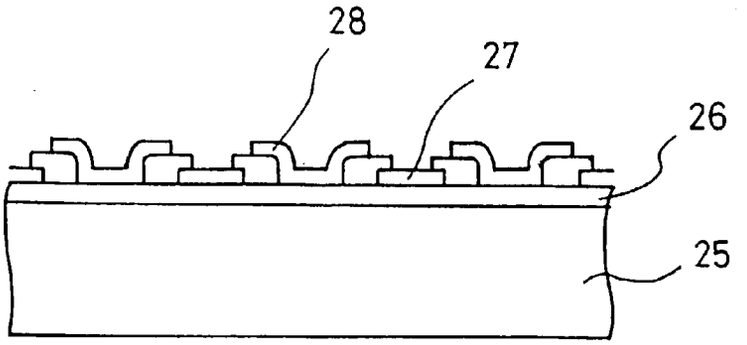

FIG. 10

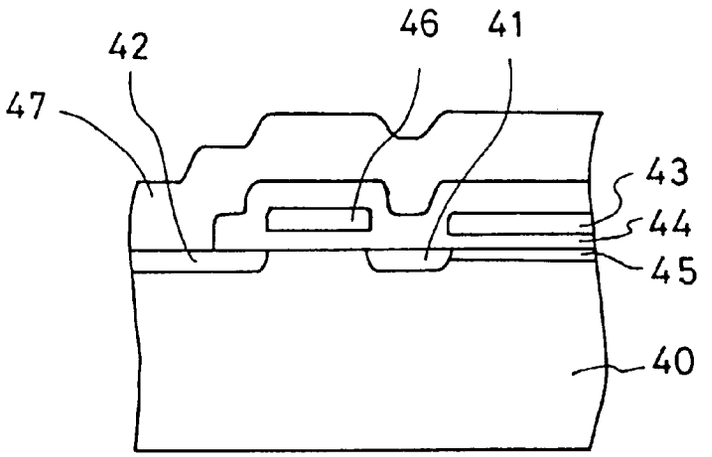

FIG. 11

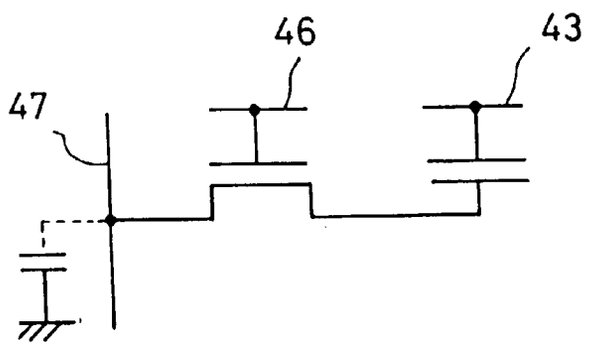

FIG. 12

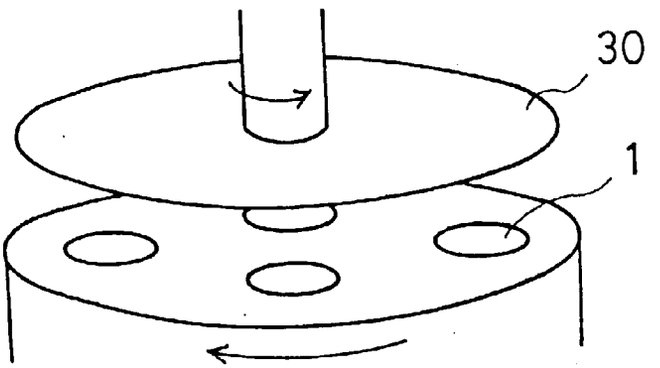

FIG. 13

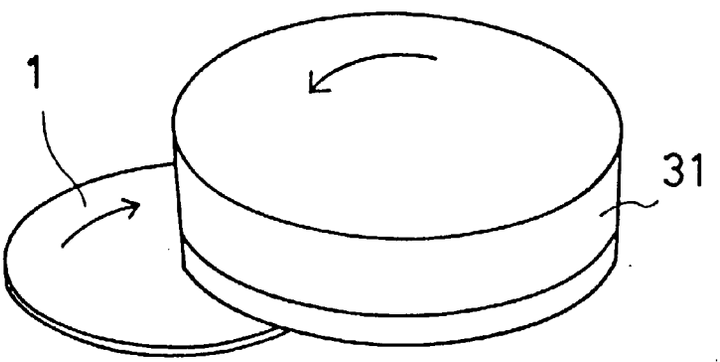

FIG. 14

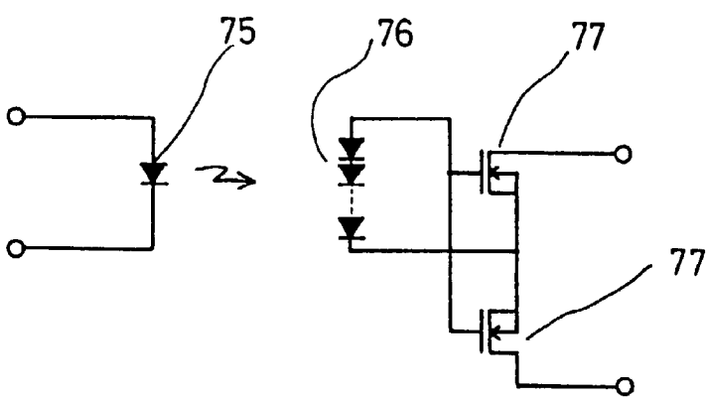

FIG. 15A

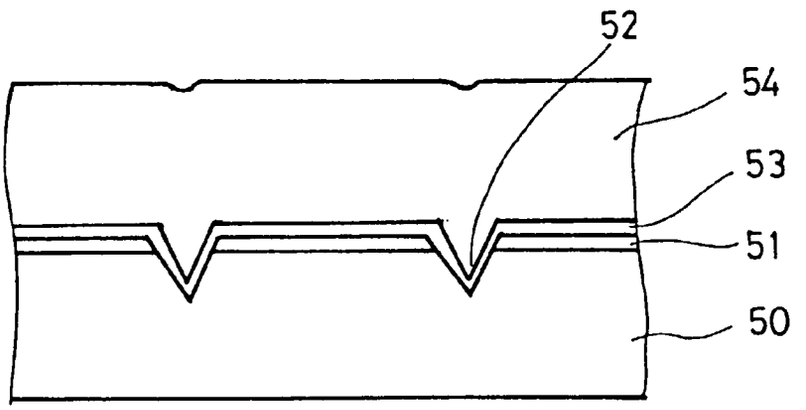

FIG. 15B

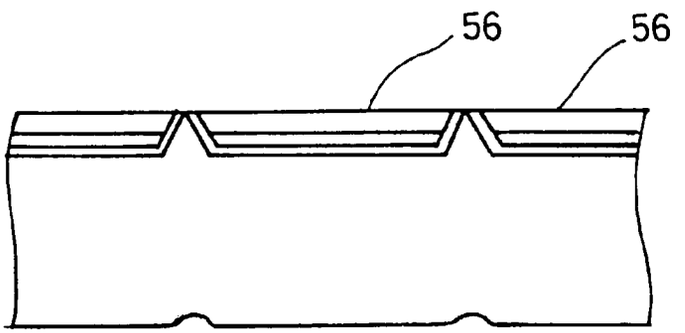

FIG. 15C

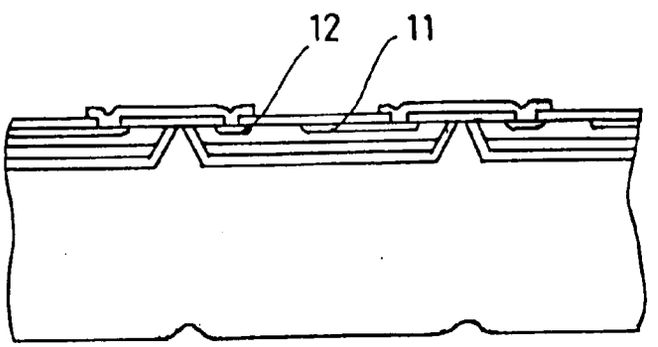

FIG. 16

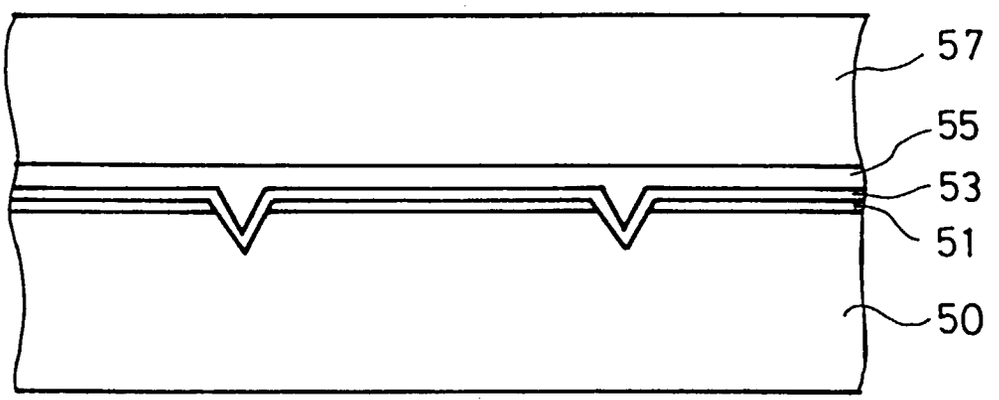

FIG. 17A

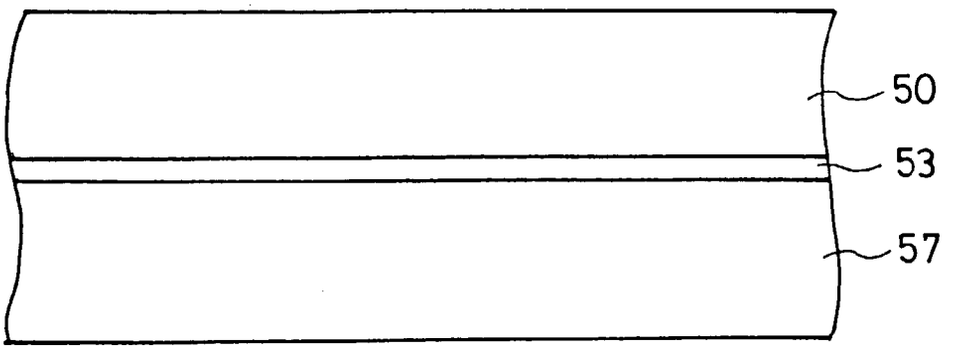

FIG. 17B

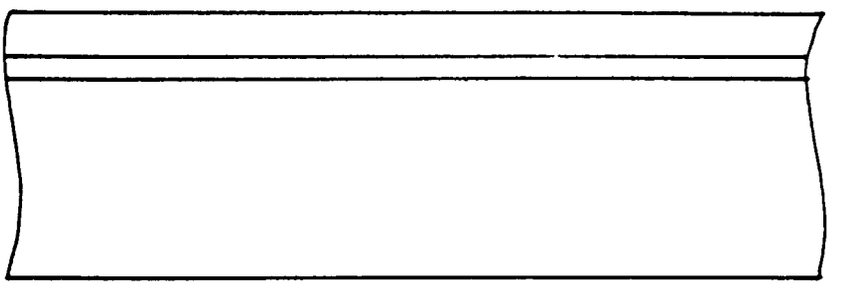

FIG. 17C

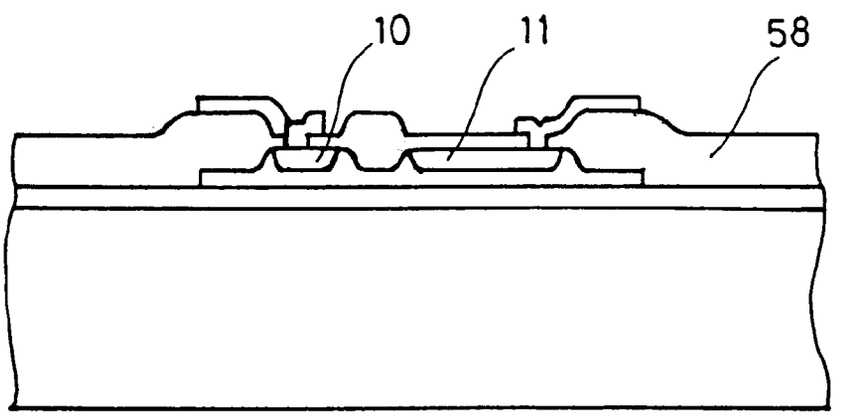

FIG. 18A

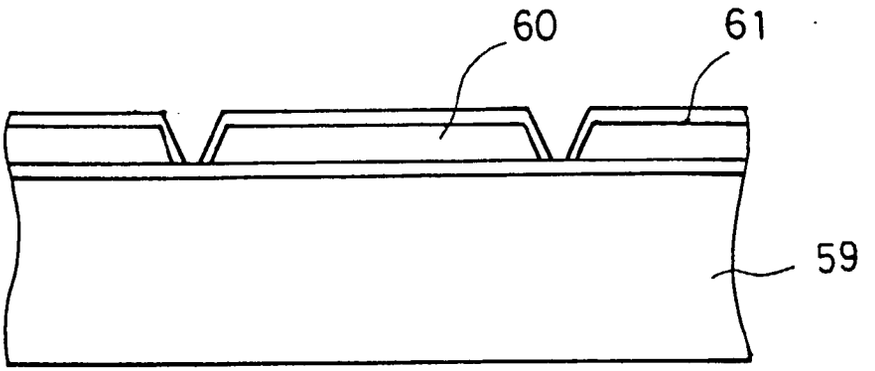

FIG. 18B

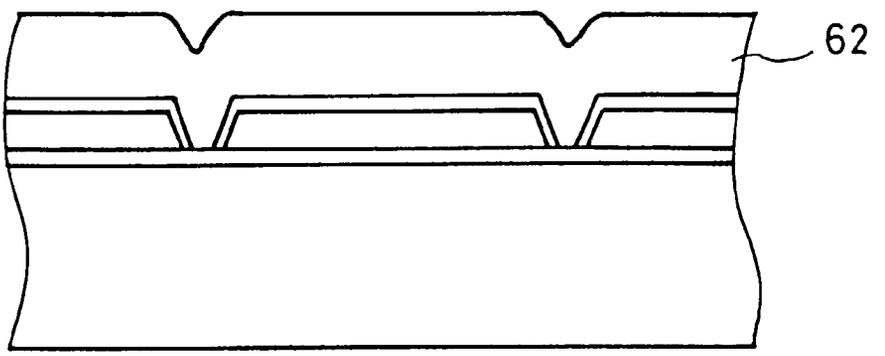

FIG. 18C

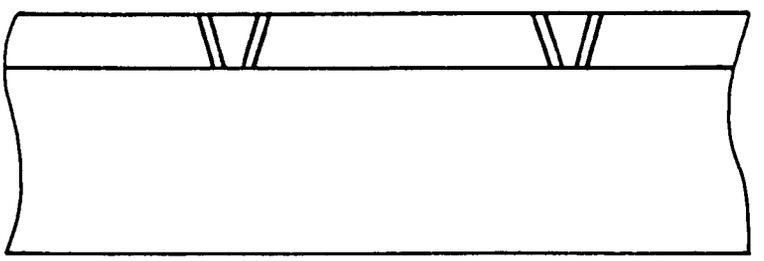

FIG. 19

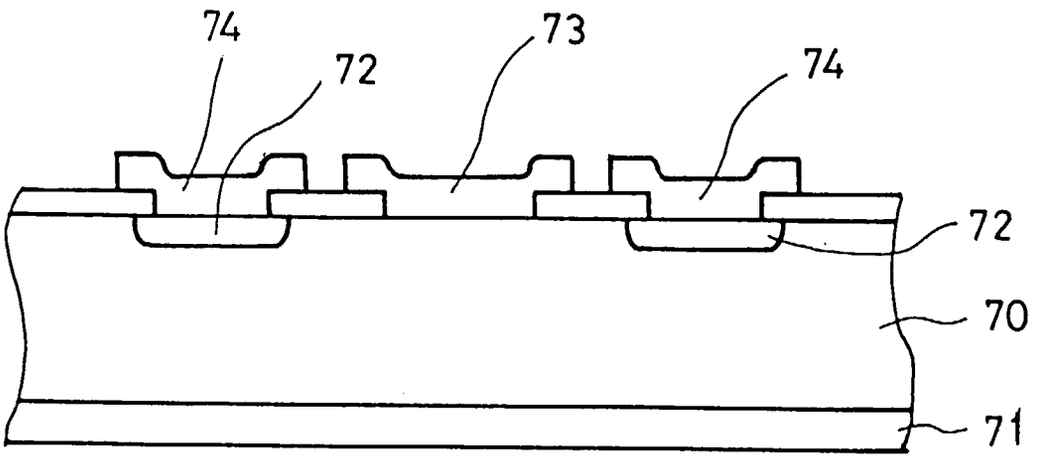

FIG. 20

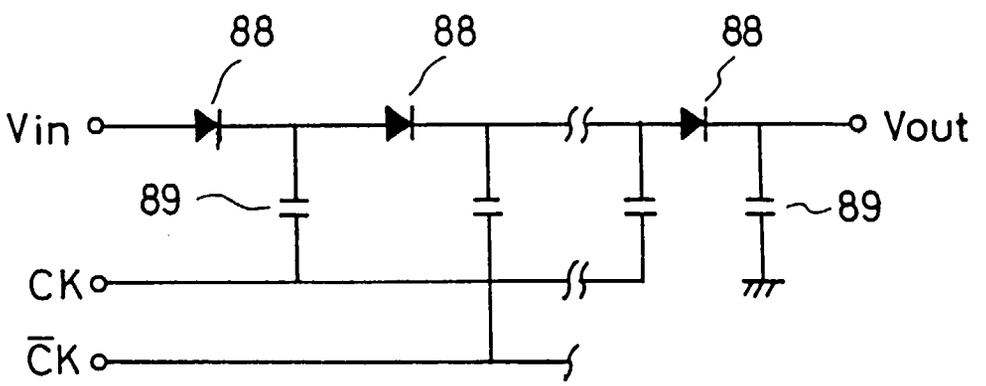

FIG. 21

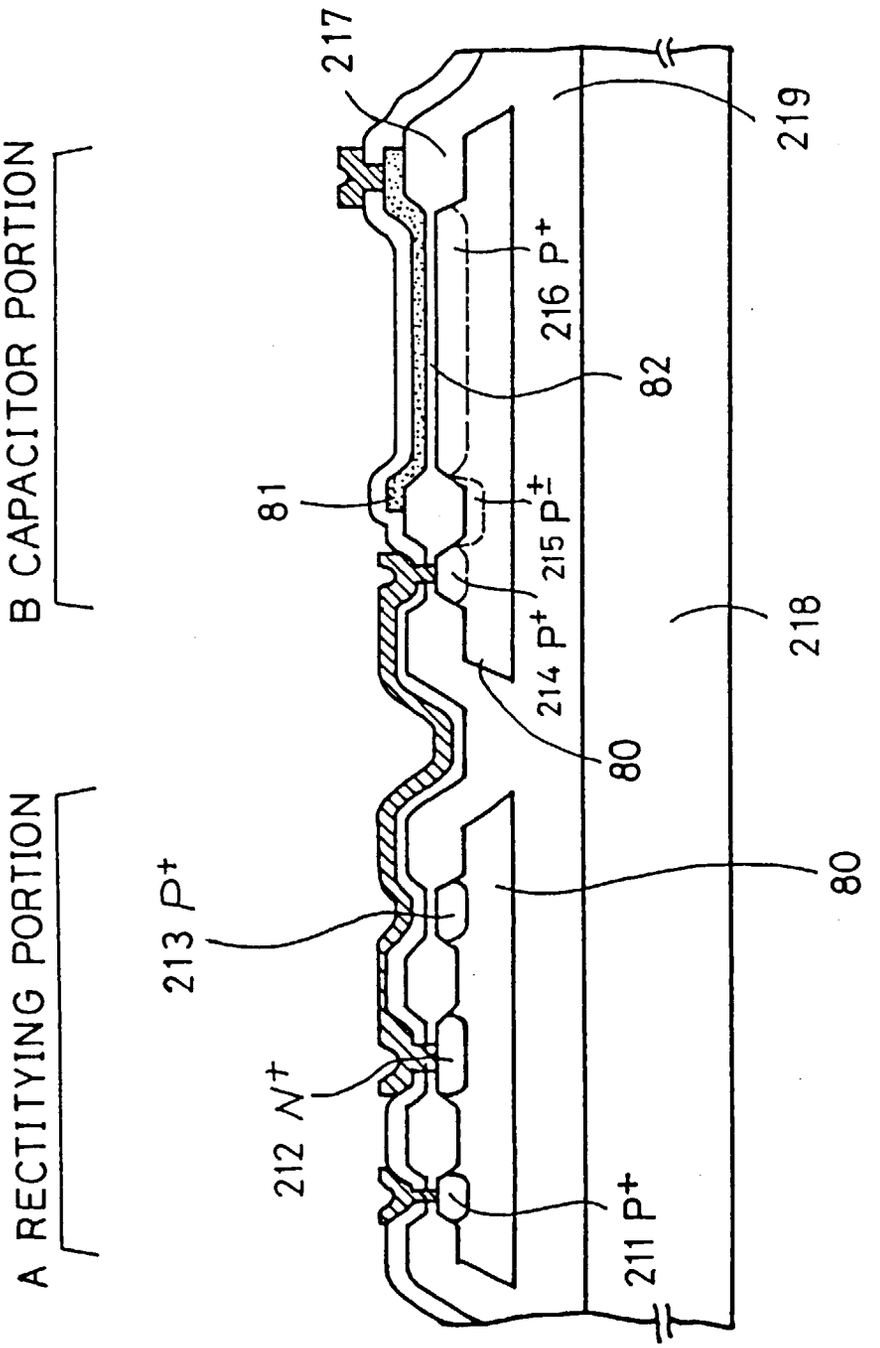
A RECTITYING PORTION
B CAPACITOR PORTION
213 P+
212 N+
211 P+
81
214 P+
215 P±
216 P+
217
82
80
80
218
219

FIG. 22

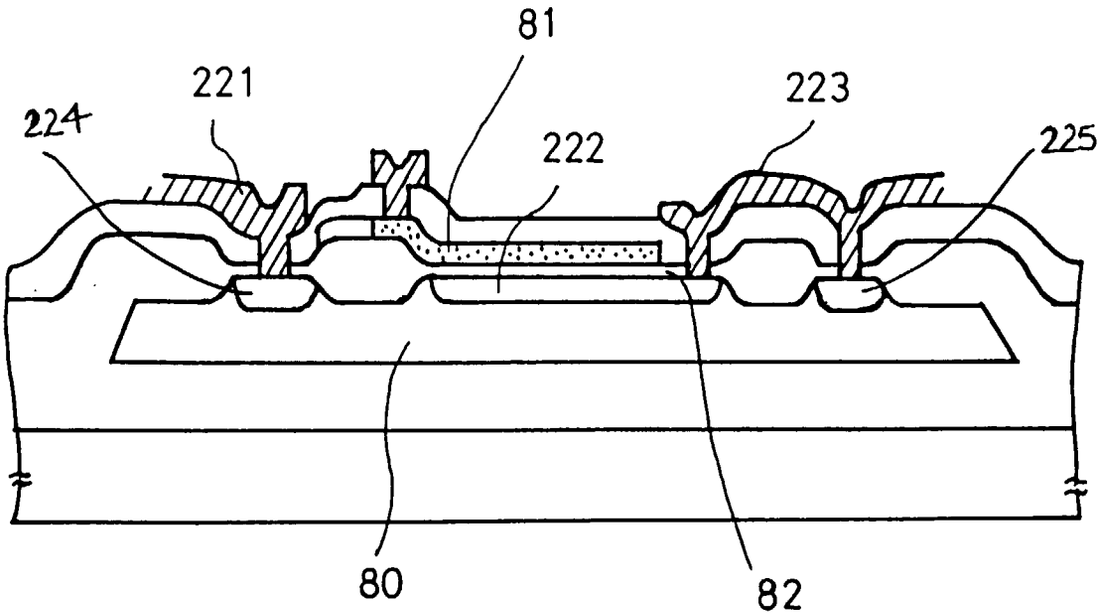
81
221
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FIG. 23

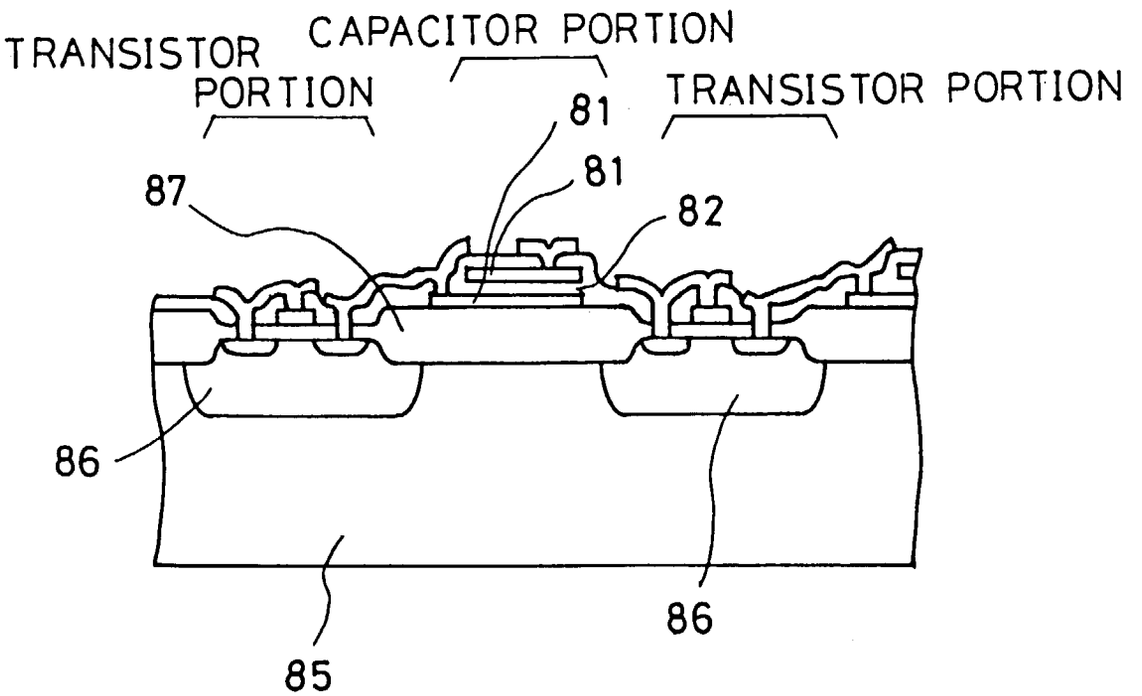

TRANSISTOR PORTION
CAPACITOR PORTION
TRANSISTOR PORTION
81
81
87
82
86
86
85

FIG. 24

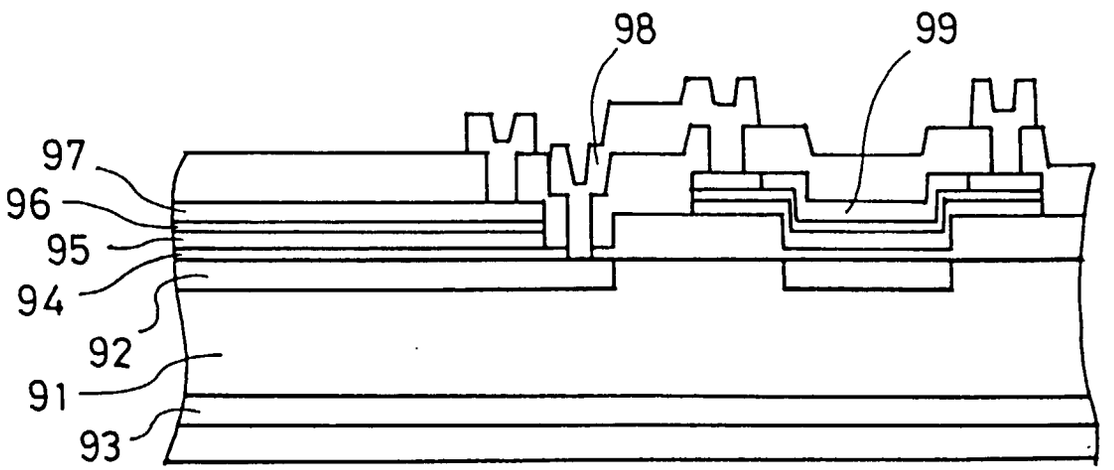


FIG. 25A

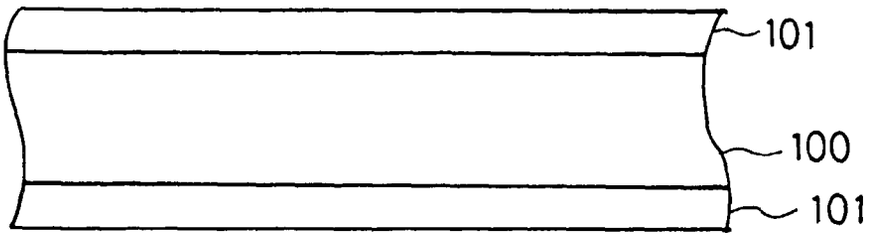


FIG. 25B

FIG. 26A

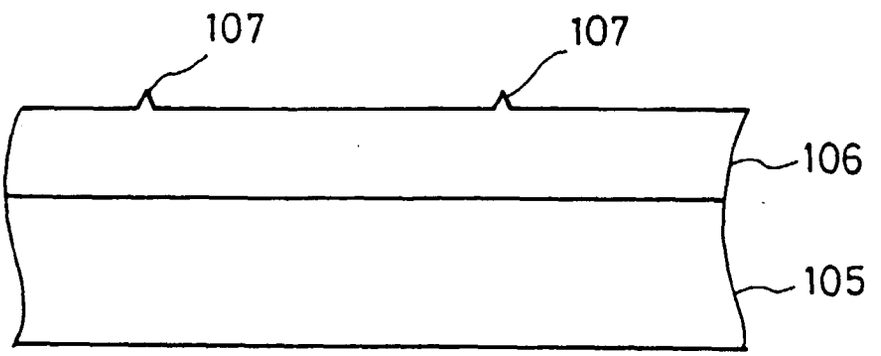
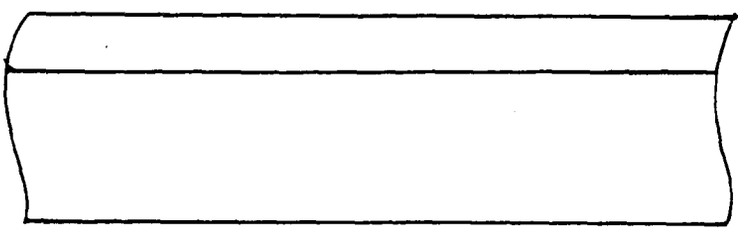


FIG. 26B



European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 96 30 0388

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X A	EP-A-0 362 516 (IBM) 11 April 1990 * claim 1; figures 1,2 *	1,6,23 27,28	B24B7/16 B24B7/22 B24B7/04
A	JAPAN NEW MATERIALS LETTER, vol. 8, no. 24, 26 December 1989, XP000105978 "ANNOUNCEMENT" * the whole document *	2-4, 20-22, 24-26	B24B1/00
A	FR-A-2 505 709 (OD POLT INSTITUT) 19 November 1982 * page 4, line 9 - page 6, line 37; figures; table 18 *	1-4, 20-28	
A	US-A-5 083 401 (YAMASHITA MIKIO ET AL) 28 January 1992 * abstract *	1	
A	EP-A-0 588 055 (MITSUBISHI MATERIALS CORP ;MITSUBISHI MATERIAL SILICON (JP)) 23 March 1994 * abstract *	5	
			TECHNICAL FIELDS SEARCHED (Int.Cl.6)
A	PATENT ABSTRACTS OF JAPAN vol. 007, no. 047 (M-196), 24 February 1983 & JP-A-57 194866 (SHINETSU KAGAKU KOGYO KK), 30 November 1982, * abstract *	1	B24B
A	US-A-3 943 666 (DION C NORMAN ET AL) 16 March 1976		

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	24 May 1996	Eschbach, D

CATEGORY OF CITED DOCUMENTS

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D : document cited in the application
L : document cited for other reasons

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