

(19)



Europäisches Patentamt

European Patent Office

Office européen des brevets



(11)

EP 0 742 660 A1

(12)

EUROPEAN PATENT APPLICATION

(43) Date of publication:
13.11.1996 Bulletin 1996/46

(51) Int Cl.⁶: **H04L 12/54**, H03M 7/00,
G06E 1/02

(21) Application number: **96201266.2**

(22) Date of filing: **08.05.1996**

(84) Designated Contracting States:
**AT BE CH DE DK ES FI FR GB GR IE IT LI LU NL
PT SE**

(71) Applicant: **Koninklijke PTT Nederland N.V.**
2509 CH Den Haag (NL)

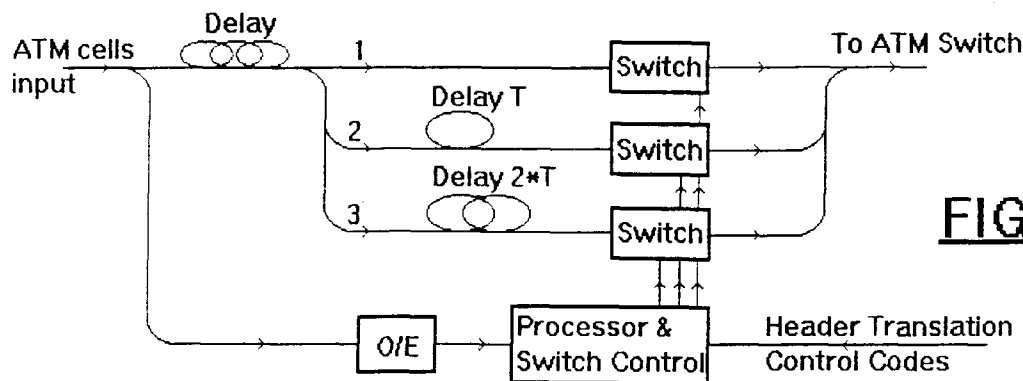
(30) Priority: **09.05.1995 NL 1000326**
28.06.1995 NL 1000682

(72) Inventors:
• **Bochove, Aart Cornelis**
2806 EL Gouda (NL)
• **Rijnders, Jan Marcel**
7523 ZT Enschede (NL)

(54) Signal processor for data conversion

(57) Signal processor for the processing of digital signals in the physical (for example, optical) domain. This is inter alia relevant for ATM systems in which control codes such as VPIs and VCIs at the inputs of sub-systems have to be changed. A symbol stream is lead through different delay branches. The number of delay branches is of such magnitude that at each moment, in

at least one of the branches, both a "1" symbol and a "0" symbol is available. By the controlled opening and closing of the switches the symbol values can be changed. Moreover, no additional source of energy (light source) is necessary and the signal processor is completely transparent, that is to say, symbols at the output of the processor have exactly the same physical properties as those at the input of the processor.

**FIG.1****EP 0 742 660 A1**

Description

A. BACKGROUND OF THE INVENTION

The invention relates to a signal processor. In particular, the invention relates to the conversion of digital signals in the physical, for example optical, domain. This is, inter alia, relevant in optical ATM systems in which at the inputs of sub-systems, such as switches, control codes such as VPIs and VCIs (Virtual Path and Channel Identifiers respectively) have to be changed. This matter is discussed, inter alia, in the Netherlands patent application NL94.02141 in the name of the applicant. Therein the conversion of logical codes is discussed. The present application concerns the conversion of logical codes, represented by optical physical codes, by means of physical manipulation of said physical codes, namely the conversion of physical "1" bits into "0" bits and vice versa. The problem in that case is simplicity and optical transparency, without making use of (auxiliary) lasers. The present invention can also be applied in "add-drop" multiplexers in optical networks, for example.

B. SUMMARY OF THE INVENTION

The invention is based on the insight that by a suitable time shift (forwards or backwards) of physical optical bits originating from the input signal, which represent certain logical codes, other logical codes can be formed without a light source being necessary for that purpose. The time for which the signal must be shifted is dependent upon the properties of the bit stream and thus of the physical code words. In general it holds that the shift must be such that in each time slot in which a bit is to be changed, a physical bit of the desired other physical kind (desired physical value or property) is present. If in a certain time slot, for example, a (physical) "0" is to be converted into a "1", a "1" must, by shifting of the bit stream, be available, or, if a "1" is to be converted into a "0", a "0" must be available.

If the logical codes are represented by amplitude-modulated bits, use can be made of the fact that a physical "0" can always be obtained by means of signal interruption during one time slot; in those cases the presence of a "0" bit need not be provided for by shifting of the bit stream. If on the other hand use is made of angularly modulated (frequency- or phase-modulated) physical bits, a physical "0" must in fact always be present. If the signal consists of more than two kinds of symbols (digits), a representative of each of those symbols must be present in the time slot. For the time being, a signal with two kinds of (binary) symbols, called "bits", will hereinafter be taken as point of departure.

According to the present invention, the signal processor comprises a bit-shifting device which, under the control of a control device, shifts the bit stream -- or a part thereof -- in such a way that, whenever a bit selected by that control device is to be converted, a bit with

the desired value, which can replace the original bit, is always present at the right moment.

If use is made of amplitude-modulated bits it holds that, if a signal is coded with bit codes in which the number of directly consecutive 0's in the bit stream never exceeds a certain value of $d_{\max}(1)$, a delay device can be successfully used from which, besides the undelayed signal, a signal can be derived which is delayed by 1, 2, ..., $d_{\max}(1)$ bit times (time slots).

A notation for such codes derived from reference 2 is (d,k)-codes, where d is the minimum number of directly consecutive 0's between two 1's, and k (hereinafter referred to as $d_{\max}(1)$) is the maximum number of consecutive 0's. In particular, the specification of codes according to such a point of view is known from the magnetic and optical recording and reproduction techniques (tape recorders, optical discs, etc.).

If use is made of non-amplitude modulated bits, in which therefore not only the presence of "1" bits must be provided for, but also that of "0" bits (which of course cannot be obtained by simple interruption of the bit stream), it holds that, if a signal is coded with codes in which the number of directly consecutive 0's does not exceed a certain maximum $d_{\max}(1)$ and furthermore the number of directly consecutive 1's does not exceed a certain maximum $d_{\max}(2)$, successful use can be made of a delay device from which, besides the undelayed signal, a signal can be derived which is delayed by 1, 2 D bit times (time slots). D is here equal to $d_{\max}(1)$ or $d_{\max}(2)$, whichever of the two is the largest. As a matter of fact, this formulation not only holds for non-amplitude modulated bits, but also for indeed amplitude-modulated bits. After all, although amplitude-modulated "0" bits can be obtained by interruption of the signal, it is not at all forbidden or impossible to generate those "0" bits in the same way as the "1" bits. For angularly modulated bits, however, this is a necessity.

If it is a requirement that the bits right at the beginning and right at the end of a bit stream also have to be capable of being converted, it must be added thereto that, if the sum ($S_{\text{begin/end}}$) of the number of identical bits (1's or 0's) at the beginning of the bit stream and the number of identical bits (1's or 0's) at the end of the bit stream is greater than $d_{\max}(1)$ or $d_{\max}(2)$, then the value of D is equal to the said sum. Notated in a shorter form, D is then therefore equal to $\text{Max}\{S_{\text{begin/end}}, d_{\max}(1), d_{\max}(2)\}$. This additional requirement in regard to the convertibility of the start and end bits can be relinquished by taking into account, in the logical domain, that the first and the last bits of the bit stream cannot be converted.

According to the invention, not only binary symbols (bits) but also non-binary physical symbols can be processed by means of symbol shifting. For the conversion of a symbol P into a symbol Q a shift is necessary which is derived from a number of time slots in which neither P nor Q is present. This generic rule, which is further discussed below, also holds for symbols which are in-

deed binary, both amplitude-modulated and angularly modulated.

In the claims formulated hereinafter, Claim 5 pertains to the processing of binary or non-binary symbols, Claim 6 to that of amplitude-modulated or non-amplitude modulated bits, and Claim 7 to that of amplitude-modulated bits.

Hereinafter the invention will be further discussed on the basis of a number of examples.

C. EXAMPLES OF EMBODIMENT

Below a number of examples of character strings are discussed which are presented to a signal processor as diagrammatically shown in Fig. 1. The examples are illustrated in Fig. 2. Fig. 3 shows an alternative embodiment of a device according to the invention; likewise Fig. 4. Fig. 5 shows the similarity and the difference between two processing rules and Fig. 6 illustrates the processing of a non-binary symbol string.

The device of Fig. 1 is formed by a number of parallel optical paths 1 ... 3, optical fibres or other waveguides, of different length or at any rate with a different delay time, in each of which an optical switch is included. Each switch is controlled by a control device which on the one hand -- via an optical receiver (O/E converter) -- receives information about the bits which are presented to the device (digits, symbols), and on the other hand receives information about which bits are to be passed on by the device unchanged and which bits are to be changed, either from "1" to "0" or from "0" to "1", from the logical domain (the system control). The Figure visualises that the device serves for the processing, in the optical domain, of the headers of presented ATM cells. Of course this is only a noncommittal example which in no regard whatsoever restricts the invention. At the time the invention was made, the processing of ATM cells and other optical wide-band applications in particular was indeed held in mind.

In the first example (2/1), two logical characters A and B (which as a matter of fact can also represent logical bits with the value of "1" or "0") are encoded according to a so-called bi-phase level code. In this code, the logical symbol A is physically represented by "10", which in Fig. 2 is represented as amplitude-modulated bits "1_0", and the logical symbol B is physically represented by "01", represented as the amplitude-modulated bits "_01". Such code (like other bi-phase codes) has the property that the signal has a constant DC level, which prevents undesirable offset arising, while at the same time the bit times ("bit clock") are recognisable. A disadvantage is that a larger bandwidth is necessary.

A code string "B A A B A A B B A" is received by the device in the form "_01_01_01_01_01_01_01_01_01" (N. B.: the transmission direction shown is, as in Fig. 1, from left to right, so that the rightmost bit is read first; the time slot sequence is therefore 1234567890123...). If it is assumed that the code string received forms part of the

header of the ATM cell and that some of the bits of that header are to be changed (which is controlled by the Header Translation Control Codes shown in the Figure), then it is clear that, if a "1" ("1_") has to be changed into a "0" ("_0"), that can be simply carried out by opening all switches in the right time slot, as a result of which the bit stream is interrupted. To change a "0" into a "1" (without supplying external (laser) power), however, measures according to the invention are necessary.

In an arbitrary bit stream with bit codes which represent logical As and Bs, the maximal distance $d_{\max}(1)$ between two consecutive "0" bits is 2 (namely in the logical code word AB: "1_0_"). To the end of always having a "1" available, the bits must always be delayed by both one bit time as well as by two bit times (time slots).

If, for example, the "A" ("1_") in slot 7/8 is to be changed into a "B" ("_01"), then the undelayed path 1, and path 2, delayed by 1 bit time (T), must be opened by the control device during slot time 7, and path 3, delayed by 2 bit times ($2 \cdot T$), must be closed, as a result of which only the signal delayed by 2 bit times ($2 \cdot T$) ("1_0", see Fig. 2) is allowed to pass. In slot 8 all switches are opened, resulting in a "_0". If in time slot 11/12 the "B" is to be changed into an "A", then all switches in slot 11 are opened, resulting in a "_0" at the output of the device, while in slot 12 the switch of path 2 or of path 3 is closed, resulting in a "1_0" at the output. If in slot time 15/16 the "A" is to be converted into a "B", then in slot 15 only the switch of path 2 is closed, while in slot 16 all switches are open.

It can be seen that if not path 1 but path 2 were to be used as default path, the whole bit stream would be delayed by 1 time slot, but that as of time slot 2 (in which then the first bit of the bit stream is present) both a "_0" and a "1_0" are available, either from path 1 which is relatively leading by 1 bit or from path 3, which is lagging by 1 bit.

In example 2/2, the two characters A and B are encoded differently. The coding of the "A" is the same as in the previous example, but the "B" is encoded by "11" ("11"). The run-length specification (see reference 2) of this coding is (0,1), since in an arbitrary character string the number of "_0"s between two consecutive "1"s is 0 (minimally) or 1 (maximally). The present invention prescribes that for amplitude-modulated bits the number of delay paths does not need to be greater than the maximum number of consecutive "_0"s, so that for this coding the number of delay paths can be restricted to 1 (in Fig. 1, path 3 may therefore be cancelled). In Table 2/2 it can be seen that in each time slot a "1_0" can be derived from the device, either from path 1 or from path 2.

Example 2/3 illustrates the case in which two logical characters A and B are each represented by two angularly modulated (angularly encoded) bits. P and Q represent the phases or frequencies of physical "1" and "0" bits respectively. Since in this case a physical "0" bit cannot be obtained by interrupting the bit stream, as in the case of amplitude modulation, the number of delay

paths in which both a P bit and a Q bit is always available is equal to 2, since $d_{\max}(1)(d_{\max}("Q"))$ is equal to 2 (namely for the logical word AB, physically represented by PQQP) and $d_{\max}(2)(d_{\max}("P"))$ is also equal to 2 (namely for the logical word BA, represented by QPPQ). It can be seen that if in an undelayed bit stream a P bit is to be converted into a Q bit, or a Q bit is to be converted into a P bit, said bit can be derived from at least one of the two delayed bit streams and can be inserted through control of the switches in the bit stream.

Example 2/4 illustrates the case in which, for angularly modulated bits, $d_{\max}(1)(d_{\max}("Q"))$ is not equal to $d_{\max}(2)(d_{\max}("P"))$, wherein it can be seen that, if the number of paths is (minimally) equal to the largest of $d_{\max}(1)$ or $d_{\max}(2)$, in each time slot P can be converted into Q or Q can be converted into P with the aid of the bits which are present in the delay paths. The value of $d_{\max}(1)$ (the maximum number of consecutive Q bits) is 1, since in each combination of the logical characters A and B the number of physical Q bits is never more than 1 (see the undelayed bits shown). The value of $d_{\max}(2)$ (the maximum number of consecutive P bits), however, is 3. By a number of delay paths equal to the largest of $d_{\max}(1)$ (=1) and $d_{\max}(2)$ (=3) the specified condition is satisfied, which is evident from Example 4.

It is noted that, when encoding character sets which are suitable for application in a processor according to the invention, attention must be paid to minimising the value of $d_{\max}(1)$ and, for angular modulation in any case, of $d_{\max}(2)$ as well. An elegant manner of encoding is that in which logical characters of m logical bits are represented by n physical bits, where $n \geq m$. In reference 2, a string of 377 12-bit characters is given in which the number of consecutive physical "0" bits (AM-modulated "0" bits) is never more than 1, in other words $d_{\max}(1) = 1$.

Under consideration of the examples in Fig. 2 the following is noted:

a. When deriving physical bits one can, as it were, reach forward or backward. If in example 2/1, for instance, the bits which are not to be converted are passed on by the undelayed path (path 1), a bit stream which is delayed with respect to the default path 1 (path 2 or 3) is used on the conversion of a "0" bit into a "1" bit, which would result in a problem should the first bit (time slot 1) already have to be converted. One can also, in a default manner, give the bit stream a maximum delay by passing the bits which do not have to be converted on via path 3; the output bit stream is then delayed by 2 time slots. Thus the bit stream through the other paths (1 and 2) leads, as a result of which it is possible to reach forward to one of the relatively leading bit streams through path 1 or 2 when deriving "1" bits. In general, the invention is therefore not based on and restricted to "delaying" the bit stream, but on its "shifting", either forward in time or backward. In the above, it was already suggested to have the bit stream pass through path 2 by default, as a result of which conversion bits can be obtained from the leading bit stream through path 1, or from the lagging

bit stream through path 3.

In the claims formulated hereinafter, Claim 3 pertains to the case that bit derivation takes place by bit delay; Claim 4 pertains to the case where the bits are derived from a bit stream which is leading with respect to the main bit stream.

b. It is not absolutely necessary to shift the whole bit stream. It is minimally necessary, in the case, for example, that a "0" bit is to be converted into a "1" bit, to shift only one "1" bit in the bit stream (for example the most proximate "1" bit) over a distance (in time slots) equal to the distance between the slot ("receptor slot") of that "0" bit which is to be converted and the slot ("donor slot") of that "1" bit which is to be used for the conversion. That "1" bit is, as it were, buffered for a short time and subsequently injected into the slot of the "0" bit which is to be converted.

c. Beside the processing of a bit stream with amplitude-modulated or angularly modulated "0" and "1" bits, the invention lends itself just as well to the processing of a bit stream with more than two kinds (thus non-binary) symbols (digits). During the treatment* of the examples 2/3 and 2/4, the optical bits manifested themselves through time slots with an optical signal having the phase, frequency or wavelength P and Q respectively. It is clear that use could also be made of non-binary symbols, represented by time slots having more (more than two) different amplitudes, phases, frequencies of wavelengths R, S, T, etc. In that manner, a first symbol (a symbol of a first kind) can always be converted into a second symbol (a symbol of a second kind): the first symbol has phase Q, for example, and is converted by shifting into a second symbol having phase T, or a first symbol having frequency S is converted into a second symbol having frequency P, etc.

Fig. 5 shows the processing of two symbol strings in different ways. For both strings in succession, per symbol (P, Q), the numbers of consecutive time slots with equal symbols (P, Q) are determined, and for both strings, per symbol (P, Q), the numbers of consecutive time slots with unequal symbols (non-P, non-Q). Per string, per processing manner, the maximum of those numbers of time slots is determined.

The symbol string of example 5/1 comprises two symbols, P and Q, and can therefore represent a string of bits. The number of consecutive P symbols (P bits) is 8 and 9; the number of Q symbols (Q bits) is 5 and 7. The maximum is therefore 9. For the conversion of P bits in this string into Q bits or vice versa in a processor according to the invention, a device is therefore necessary which can provide a lead or lag of 9 time slots. The numbers of consecutive non-P bits are 5 and 7 respectively, and the numbers of consecutive non-Q bits 8 and 9. The maximum is therefore again 9. The result is actually the same as the foregoing, since of course in each string with P and Q bits each non-P bit is a Q bit, and each non-Q bit is a P bit. Thus both methods produce the same result, namely a required lead or lag of 9 time

slots. The symbol string of example 5/2 is the same as that of example 5/1, although in some places the P or Q symbols have been replaced by a third symbol X. The detection of consecutive identical P and Q symbols now results in strings of 2, 2, 3 and 1 consecutive P symbols and 2, 1, 2 and 2 consecutive Q symbols; the maximum is 3. It is clear that should, for example, the first (left-most) P symbol have to be changed into a Q symbol -- making use of a donor symbol -- a delay of 8 time slots would be necessary for that purpose, since the next Q symbol does not appear until 8 time slots after the P symbol. It is clear that the maximum of 3 which was calculated according to the first method now does not signify the correct number of required leading or lagging time slots. The detection of the numbers of non-P and non-Q symbols (and also non-X symbols) produces a correct result however, namely 9 time slots.

Fig. 6 shows the complete elaboration of an arbitrary string of symbols P, Q, R and S, in which all numbers of directly consecutive non-P, non-Q, non-R and non-S symbols were determined, resulting in a maximum value thereof of 15. On checking, it becomes evident that, in the case shown, the calculated maximum shift of 15 time slots is necessary if the Q symbol in time slot 28 should have to be replaced by a P symbol, which takes place by delaying a P symbol which was presented to the processor 15 time slots earlier (in time slot 13) for 15 time slots, and injecting it into time slot 28 in the symbol string instead of the original Q symbol.

It is noted that, in order to prevent longer shifting times, it is of importance that the numbers of directly consecutive equal "non-symbols" (non-P symbols, non-Q symbols, etc.) are restricted as much as possible when drawing up encoding tables.

In the claims formulated hereinafter, Claim 8 pertains to a processor of an architecture as shown in Fig. 1.

An alternative exemplary embodiment for the implementation of the invention is diagrammatically shown in Fig. 3. The device of Fig. 3 comprises an undelayed path with a switch as in Fig. 1, and a delay path with a controllable delay. The switch in that delay path is of the type which in a first position is capable of excluding from the main circuit a connected delay circuit having a delay time of one slot (T) (and simultaneously closing the delay circuit in itself) or, in a second position, of including it; such switches are known as cross-bar switches. A fixed delay circuit is further included. If the switch is in the first position, the signal is delayed by the fixed delay circuit for 1 time slot. If the switch is in the second position the delay, by both delay circuits, is 2 time slots. As in Fig. 1 the switch is controlled by a control device which calculates the positions of the switch on the basis of the incoming bit stream and the (header) translation codes. By including more cross-bar switches with delay circuits, more delay times, 3*T, 4*T, etc. can be realised, just as in the configuration of Fig. 1 more delay paths with delays of 3*T, 4*T, etc. can be added.

In the claims formulated hereinafter, Claim 9 per-

tains to a processor of an architecture as shown in Fig. 3.

Finally, Fig. 4 shows another exemplary embodiment of a processor which, besides a control device, comprises one controllable delay device, in the form of a cross-bar switch. Such a processor is well applicable for the permutation of bits in bit words with only very few consecutive equivalent bits.

D. REFERENCES

1. Netherlands patent application NL94.02141, in the name of the applicant. IEEE,
2. Schouhamer Immink, K.A., "Runlength-limited sequences", Proc. IEEE, V.78.11 (Nov. 1990)

Claims

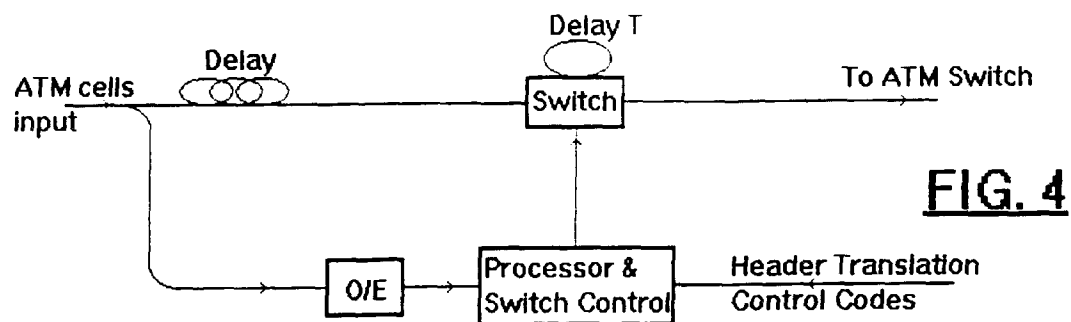
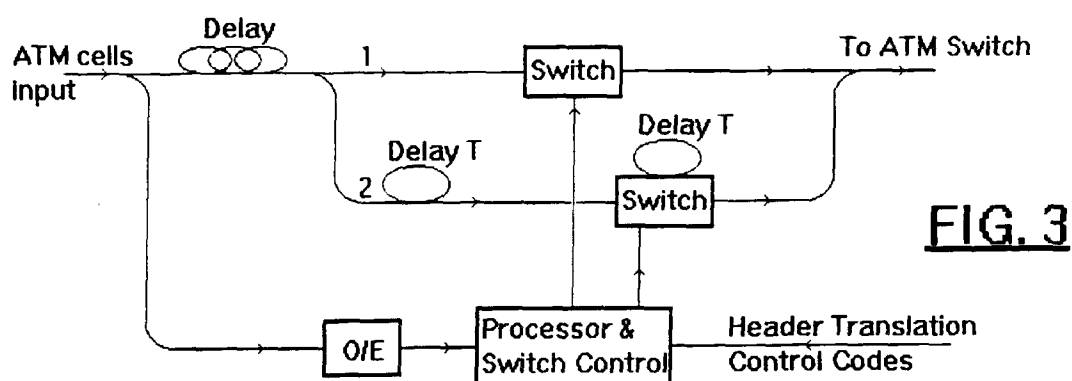
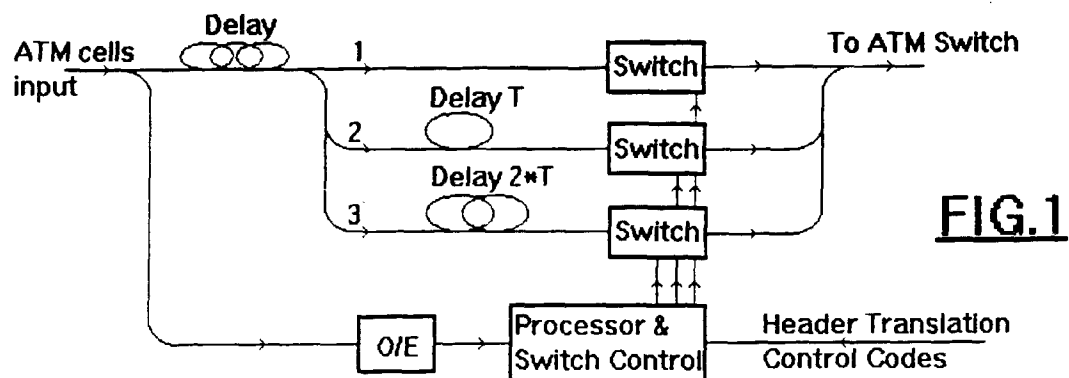
1. Signal processor for processing a stream of binary or non-binary symbols (P, Q, R, S, ...) presented to that processor, namely the conversion of first symbols (P), that is to say symbols of a first physical kind or having a first physical value, into second symbols (Q), that is to say symbols of a second physical kind or having a second physical value, characterised by a symbol-shifting device which, for the conversion of a first symbol (P) into a second symbol (Q), selects from the symbol stream such a second symbol and shifts it in time over a number of time slots equal to the number of time slots between the first symbol to be converted and the selected second symbol, and subsequently puts the selected and shifted second symbol in the place of the first symbol which was to be converted.
2. Signal processor according to Claim 1, characterised in that the shifting device is formed by a system of one or more transmission paths, in at least one of which the symbol stream, or at least one second symbol (Q) from that symbol stream, necessary for said symbol conversion, is shifted in time over the said number of time slots with respect to the symbols presented to the processor.
3. Signal processor according to Claim 2, characterised in that the symbol stream, except for the first signal (P) which is to be converted into a second symbol (Q), is transferred by the signal processor via a path (path 1) in which the symbol stream is not deliberately delayed, and that the second symbol which is required for the conversion is transferred via a delay path (path 2, 3,...) of which the delay is equal to the time slot distance between the first symbol which is to be converted and the second symbol which is to be used for that conversion.
4. Signal processor according to Claim 2, characterised in that the symbol stream, with the exception

of the first symbol (P) which is to be converted into a second symbol (Q), is transferred by the signal processor via a delay path (path 2, 3, ...) in which the symbol stream is deliberately delayed and that the second symbol, necessary for the conversion, is transferred via a path (path 1, 2, 3, ...) in which the symbol stream either leads or lags, in which the delay is equal to the time slot distance between the first symbol which is to be converted and the second symbol which is to be used for that conversion.

5. Signal processor according to Claim 2, characterised by a shifting device in which the symbols presented to the processor are shiftable in time from 1 to D time slots, where D is equal to the maximum number of directly consecutive symbols unequal to the second symbol (Q), appearing in the presented symbol stream.
6. Signal processor according to Claim 2, in which the number of different symbols is restricted to two (P, Q) characterised by a shifting device in which the symbols presented to the processor are shiftable in time from 1 to D time slots, where D is equal to the maximum number of directly consecutive symbols equal to the first symbol (P), appearing in the presented symbol stream.
7. Signal processor according to Claim 2, suitable for the processing of symbol streams with binary, amplitude-modulated symbols ("_", "∩"), characterised by a shifting device in which the symbols presented to the processor are shiftable in time from 1 to D time slots, where D is equal to the maximum number of directly consecutive physical "0" symbols ("_") appearing in the presented symbol stream.
8. Signal processor according to Claim 5, 6 or 7, characterised by D separately switchable symbol delay paths (path 2, 3, ...) with delay times from 1 to D time slots.
9. Signal processor according to Claim 5, 6 or 7, characterised by a symbol delay path with D shifting units of which at least D-1 are switchable, each with a delay time of one time slot.

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EXAMPLE 2/1:

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A=n_ B=n_ ----->
Code word..... B A A B A A B B A
Time slots.....09876543210987654321
Path 1: undelayed bits....._n_n_n_n_n_n_n_
Path 2: delay is 1 bit time....._n_n_n_n_n_n_n_
Path 3: delay is 2 bit times...._n_n_n_n_n_n_n_..

```

EXAMPLE 2/2:

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A=n_ B=nn ----->
Code word..... B A A B A A B B A
Time slots.....9876543210987654321
Path 1: undelayed bits.....nnn_n_nnn_n_nnnnn_
Path 2: delay is 1 bit time.....nnn_n_nnn_n_nnnnn_

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EXAMPLE 2/3:

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A=PQ B=QP ----->
Code word..... B A A B A A B B A
Time slots.....09876543210987654321
Path 1: undelayed bits.....QPPQPQPQPQPQPQPQP
Path 2: delay is 1 bit time.....QPPQPQPQPQPQPQPQP.
Path 3: delay is 2 bit times....QPPQPQPQPQPQPQPQP..

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EXAMPLE 2/4:

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A=PQP B=QPP ----->
Code word..... B A A B A A B B A
Time slots.....098765432109876543210987654321
Path 1: undelayed bits.....QPPQPQPQPQPQPQPQPQPQPQP
Path 2: delay is 1 bit time.....QPPQPQPQPQPQPQPQPQPQPQP.
Path 3: delay is 2 bit times....QPPQPQPQPQPQPQPQPQPQPQP..
Path 4: delay is 3 bit times....QPPQPQPQPQPQPQPQPQPQPQP...

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FIG. 2

EXAMPLE 5/1

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Symbolstring: P P P P P P P P Q Q Q Q P P P P P P P P Q Q Q Q Q Q
Consecutive 'P'-symbols: 8 9
Consecutive 'Q'-symbols: 5 7 Maximum value: 9
Consec. 'NON-P'-symbols: 5 7
Consec. 'NON-Q'-symbols: 8 9 Maximum value: 9

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EXAMPLE 5/2

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Symbolstring: P P P P X P P P Q Q X Q P P P P X P P P Q Q X X Q Q
Consecutive 'P'-symbols: 4 3 4 3
Consecutive 'Q'-symbols: 2 2 3 2 Maximum value: 4
Consec. 'NON-P'-symbols: 1 5 2 7
Consec. 'NON-Q'-symbols: 8 1 9 2 Maximum value: 9

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FIG. 5

EXAMPLE 6/1:

Time slots.....543210987654321098765432109876543210987654321
 Symbolstream.....QSRQSRQPQPQRRRRSPQRRPQRRRRSSQSRSPQPSRSPPPQRS

Path 1: undelayed symbol.....QSRQSRQPQPQRRRRSPQRRPQRRRRSSQSRSPQPSRSPPPQRS
 Path 2: delay is 1 symbol time.....QSRQSRQPQPQRRRRSPQRRPQRRRRSSQSRSPQPSRSPPPQRS
 Path 3: delay is 2 symbol times.....QSRQSRQPQPQRRRRSPQRRPQRRRRSSQSRSPQPSRSPPPQRS
 Path 4: delay is 3 symbol times.....QSRQSRQPQPQRRRRSPQRRPQRRRRSSQSRSPQPSRSPPPQRS
 Path 5: delay is 4 symbol times.....QSRQSRQPQPQRRRRSPQRRPQRRRRSSQSRSPQPSRSPPPQRS
 Path 6: delay is 5 symbol times.....QSRQSRQPQPQRRRRSPQRRPQRRRRSSQSRSPQPSRSPPPQRS
 Path 7: delay is 6 symbol times.....QSRQSRQPQPQRRRRSPQRRPQRRRRSSQSRSPQPSRSPPPQRS
 Path 8: delay is 7 symbol times.....QSRQSRQPQPQRRRRSPQRRPQRRRRSSQSRSPQPSRSPPPQRS
 Path 9: delay is 8 symbol times.....QSRQSRQPQPQRRRRSPQRRPQRRRRSSQSRSPQPSRSPPPQRS
 Path 10: delay is 9 symbol times.....QSRQSRQPQPQRRRRSPQRRPQRRRRSSQSRSPQPSRSPPPQRS
 Path 11: delay is 10 symbol times.....QSRQSRQPQPQRRRRSPQRRPQRRRRSSQSRSPQPSRSPPPQRS
 Path 12: delay is 11 symbol times.....QSRQSRQPQPQRRRRSPQRRPQRRRRSSQSRSPQPSRSPPPQRS
 Path 13: delay is 12 symbol times.....QSRQSRQPQPQRRRRSPQRRPQRRRRSSQSRSPQPSRSPPPQRS
 Path 14: delay is 13 symbol times.....QSRQSRQPQPQRRRRSPQRRPQRRRRSSQSRSPQPSRSPPPQRS
 Path 15: delay is 14 symbol times.....QSRQSRQPQPQRRRRSPQRRPQRRRRSSQSRSPQPSRSPPPQRS
 Path 16: delay is 15 symbol times.....QSRQSRQPQPQRRRRSPQRRPQRRRRSSQSRSPQPSRSPPPQRS

Check symbolstrings over paths 1-16:

Timeslot 16 'RRSPQPSRSPPPQRS' 4 diff. symbols: OK
 Timeslot 17 'SRRSPQPSRSPPPQR' 4 diff. symbols: OK
 Timeslot 18 'QSRSPQPSRSPPPQP' 4 diff. symbols: OK
 Timeslot 19 'SQSRSPQPSRSPPP' 4 diff. symbols: OK
 Timeslot 20 'SSQSRSPQPSRSP' 4 diff. symbols: OK
 Timeslot 21 'RSSQSRSPQPSR' 4 diff. symbols: OK
 Timeslot 22 'RRSSQSRSPQPSR' 4 diff. symbols: OK
 Timeslot 23 'RRSSQSRSPQPS' 4 diff. symbols: OK
 Timeslot 24 'RRSSQSRSPQPS' 4 diff. symbols: OK
 Timeslot 25 'RRSSQSRSPQPS' 4 diff. symbols: OK
 Timeslot 26 'RRSSQSRSPQPS' 4 diff. symbols: OK
 Timeslot 27 'RRSSQSRSPQPS' 4 diff. symbols: OK
 Timeslot 28 'RRSSQSRSPQPS' 4 diff. symbols: OK
 Timeslot 29 'RRSSQSRSPQPS' 4 diff. symbols: OK
 Timeslot 30 'RRSSQSRSPQPS' 4 diff. symbols: OK
 Timeslot 31 'RRSSQSRSPQPS' 4 diff. symbols: OK
 Timeslot 32 'RRSSQSRSPQPS' 4 diff. symbols: OK
 Timeslot 33 'RRSSQSRSPQPS' 4 diff. symbols: OK
 Timeslot 34 'RRSSQSRSPQPS' 4 diff. symbols: OK

Timeslot 35 'RSPQRRPQRRRRRR' 4 diff. symbols: OK
 Timeslot 36 'RRSPQRRPQRRRRRR' 4 diff. symbols: OK
 Timeslot 37 'RRSPQRRPQRRRRRR' 4 diff. symbols: OK
 Timeslot 38 'RRSPQRRPQRRRRRR' 4 diff. symbols: OK
 Timeslot 39 'RRSPQRRPQRRRRRR' 4 diff. symbols: OK
 Timeslot 40 'RRSPQRRPQRRRRRR' 4 diff. symbols: OK
 Timeslot 41 'RRSPQRRPQRRRRRR' 4 diff. symbols: OK
 Timeslot 42 'RRSPQRRPQRRRRRR' 4 diff. symbols: OK
 Timeslot 43 'RRSPQRRPQRRRRRR' 4 diff. symbols: OK
 Timeslot 44 'RRSPQRRPQRRRRRR' 4 diff. symbols: OK
 Timeslot 45 'RRSPQRRPQRRRRRR' 4 diff. symbols: OK
 Timeslot 46 'RRSPQRRPQRRRRRR' 4 diff. symbols: OK
 Timeslot 47 'RRSPQRRPQRRRRRR' 4 diff. symbols: OK
 Timeslot 48 'RRSPQRRPQRRRRRR' 4 diff. symbols: OK
 Timeslot 49 'RRSPQRRPQRRRRRR' 4 diff. symbols: OK
 Timeslot 50 'RRSPQRRPQRRRRRR' 4 diff. symbols: OK

FIG. 6



European Patent
Office

EUROPEAN SEARCH REPORT

Application Number
EP 96 20 1266

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	WO-A-94 21088 (BRITISH TELECOM) 15 September 1994	1,2	H04L12/54 H03M7/00 G06E1/02
A	* page 5, line 27 - page 6, line 12 * * page 11, line 3 - line 28; figure 6 *	3-9	
A	EP-A-0 541 855 (SIEMENS) 19 May 1993 * abstract; figure 1 *	1	
			TECHNICAL FIELDS SEARCHED (Int.Cl.6)
			G06E H03M
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 10 July 1996	Examiner Cohen, B
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document			

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