(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 744 683 B1

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention of the grant of the patent:
03.03.1999 Bulletin 1999/09

(51) Int Cl.[6]: **G05F 1/00**, G05F 1/56

(21) Application number: **95830216.8**

(22) Date of filing: **22.05.1995**

(54) **A constant voltage drop voltage regulator**

Konstantspannungsabfall-Spannungsregler

Régulateur de tension à chute de tension constante

(84) Designated Contracting States:
DE FR GB IT

(43) Date of publication of application:
27.11.1996 Bulletin 1996/48

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EP 0 744 683 B1

Description

[0001] The present invention relates to a constant voltage drop voltage regulator, and in particular to a regulator for obtaining from a regulated supply voltage, whose regulation accuracy is retained, a voltage a fraction of a volt below the regulated voltage.

[0002] The technology of integrated circuits for data processing systems, in particular personal computers, is living a transition period in which, to provide high performance and increasingly higher operating frequencies, operating voltages are used which are set at non-standard values, in general operating voltages below 5V, which has long been standard for the supply voltage to integrated circuits with bipolar and CMOS technology.

[0003] This in order to reduce the power dissipated by integrated circuits and, therefore, power requirements.

[0004] Particularly for microprocessor systems, a mixed solution is gaining acceptance wherein some components are supplied a first voltage and others are supplied a second voltage differring by fractions of a volt from the first.

[0005] In some cases, the same component may be supplied two distinct voltages.

[0006] A typical value of the supply voltage in use today is 3.3V, but it is not infrequent for a voltage of 3.6V or 3.0V to be also used.

[0007] Applications at 2.7V and even 2.5V have been developed of late.

[0008] Quite often, the power to be supplied at this voltage is small, and the use of a central supply to output several voltages is economically impractical.

[0009] Thus, solutions are making their inroads wherein a first regulated voltage, e.g. 5V, generated by a central supply, is supplied to local DC/DC converters which generate the desired voltages of 3.6V, 3.3V, or else according to necessity.

[0010] Switching post regulators have also been proposed fed by a pulsed voltage.

[0011] An example of such regulators is provided by the document: "Electronique" N°41, page 82; October 1994, Paris (UTILISER LA POST-REGULATION SYNCHRONE).

[0012] In this document a switching post regulator is suggested which is fed by a pulsed, alternate voltage of 5 V, obtained from a preregulator.

[0013] The voltage is fed to an LC network through a MOSFET transistor controlled to perform as pulse width modulation switch, synchronous with the supply voltage pulses.

[0014] This circuit cannot operate with a supply voltage lesser than 5 V because otherwise the MOSFET cannot be brought into saturation.

[0015] Alternatively, linear or more properly "series" regulators have been used where the primary supply voltage exceeds by at least one volt the secondary voltage sought.

[0016] The use of a MOSFET as a series regulator allows to design nearly zero drop linear regulators, as disclosed in the document: Radio Fernschen Electronik (40,1991) N°7 pag 389 (ZERO DROP SPANNUNGSREGLER) but still requires a supply voltage no lesser than 5 V, unless a voltage multiplier is provided as disclosed in the document Electronic Design 42(1994) March 7 N°5 pages 45,46 48,49 (TINY IC PLUS FET BUILDS "SUPER LDO" REGULATOR).

[0017] These solutions have several drawbacks:

- The conversion efficiency is, both for linear regulators and DC/DC converters, comparatively low, perhaps of less than 70%.
- Since all the devised regulators provide a fixed output voltage, independently of changes in the supply voltage, no justification operations, or operations to check the functionality of the electronic system, can be carried out at different supply voltages within a range of the nominal working voltage, except by altering all the supply voltages to some extent.
- It is neither easy nor economical to provide linear regulators for generating secondary voltages a fraction of a volt less than the primary voltage.

[0018] These limitations are overcome by the constant voltage drop voltage regulator whereby, from a regulated primary voltage, for example of 5V or 3.6V, a secondary voltage can be obtained which may be just a fraction of a volt lower, e.g. of 4.5V from 5V and 3.3V from 3.6V, and has the same characteristics of absolute precision of regulation and ripple as the primary voltage through broad ranges of load variation and without introducing any appreciable regulation errors and noise into the output voltage.

[0019] These results are obtained by a constant voltage drop voltage regulator where a MOSFET device connected in series between the primary voltage and the load to be supplied a secondary voltage, is controlled to produce a predetermined constant voltage drop which is independent of the load and the primary supply voltage.

[0020] The MOSFET device is controlled by means detecting the voltage drop across the MOSFET (in practice, a fed-back differential amplifier) to generate a voltage signal related to the voltage drop and means comparing the voltage signal to a reference voltage (in practice, a second differential amplifier) to generate a control error signal applied to the control gate of the MOS device.

[0021] A voltage multiplier provides the voltage required to power the control circuits and bias the control gate of the MOSFET, even if the primary voltage available is on the order of few volts (2-5V). MOSFETs require, in fact, a bias voltage on the order of several volts.

[0022] A voltage regulator so constructed attains, even under a low load, a high conversion efficiency which is substantially equal to the ratio of the secondary voltage to the primary voltage, the power requirements

of the control circuits being negligible.

[0023] Furthermore, compared to switching regulators, it has no minimum and maximum load restrictions, beyond which the regulating function fails, the maximum power supplied being only limited by problems of thermal dissipation.

[0024] Further advantages over regulators of the switching type are:

- intrinsic following of the input voltage for both quasi-static variations and fast dynamic load, which makes the justifying operations feasible and simple;
- possibility of regulating the voltage drop by varying the value of a resistor;
- no generation of noise on the output voltage as caused by the voltage regulator.

[0025] The features and advantages of the invention will be more clearly apparent from the following description of a preferred embodiment and the accompanying drawings, in which:

- Figure 1 shows, in block diagram form, a voltage regulator embodying the present invention;
- Figure 2 shows a circuit diagram of a preferred embodiment of the regulator according to the present invention;
- Figure 3 shows a modified embodiment of the regulator in Figure 2.

[0026] Referring to Figure 1, the voltage regulator according to the present invention basically comprises:

- a field-effect power transistor or MOSFET 1, having an N-type channel, its drain electrode connected to the positive terminal 2 of a first DC voltage source V1 having a second terminal 3 connected to a reference ground, and source electrode connected to an output terminal 4 of the regulator;
- a control circuit 5 with two signal inputs 6, 7 respectively connected to the terminals 2 and 4 to receive a voltage signal equal to the voltage drop across the drain and source of the MOSFET 1, and with a third signal input 8 for receiving a constant reference voltage VREF relative to the output voltage V2 of the regulator and generated by a reference voltage generating circuit 9 connected to the terminal 4; and
- a voltage multiplier.

[0027] The control circuit 5 amplifies the voltage received across the inputs 6, 7 and compares it to the reference voltage applied to the input 8 (and related to the output terminal 4).

[0028] The variation between the two voltages, as suitably amplified, is presented as an error signal on an output 10.

[0029] The voltage present on the output 10 is applied, via an output current limiter resistor 11, to the control gate of the MOSFET 1 and modulates the conductivity of the same according to the error.

[0030] Unlike bipolar transistors, the voltage drop across a MOSFET is resistive in nature and has a virtually null lower limit corresponding to an internal resistance (in MOSFETs for low voltages) on the order of ten milliohms.

[0031] Therefore, it is possible to obtain a voltage drop across the MOSFET on the order of a fraction of a volt even with loads which vary virtually between 0A and tens of A, simply by controlling its conductivity.

[0032] The power supply of the control circuit, which is to produce a control signal to the MOSFET at a level of positive voltage on the order of some volts (6-7), relative to the source electrode voltage of the MOSFET, is ensured by a conventional voltage multiplier circuit 12 being supplied the voltage V1.

[0033] The most appropriate multiplication ratio depends on the voltage V1; for example, if V1 is on the order of 3V (3.6 to 3V), a tripler is needed; if the voltage V1 is less than 3V, a quadrupler may be better.

[0034] An input capacitance 13 and output capacitance 14 of suitable value act as input and output voltage surge damping filters, contributing toward the regulating loop stability.

[0035] A diode 15 with the anode connected to the terminal 2 and the cathode connected to the terminal 4 provides power supply to the terminal 4 at a voltage equal to V1-VD (where, VD is the forward voltage drop across the diode 15) and precharge to the capacitance 14 during the starting up phase (Startup) of the supply system and the regulator.

[0036] This type of regulator allows a voltage V2 to be obtained between the terminal 4 and the conventional reference ground which is independent of the load, even with large variations of the same, between a minimum, practically of zero, and a maximum which is only limited by the power dissipable through the MOSFET 1.

[0037] The voltage V2 differs from the supply voltage V1 by a predetermined value enforced by the regulating circuit.

[0038] It, therefore, is apparent that V2 has, in absolute value, the same precision characteristics as the voltage V1, and any variation in V1 reflects in V2.

[0039] It, therefore, is possible to carry out in an easy manner operations of justification of an electronic system being supplied the combined voltages V1 and V2.

[0040] Figure 2 shows in detail a wiring diagram of a preferred embodiment of the constant voltage drop voltage regulator.

[0041] The components of FIgure 2 which are functionally equivalent to those of Figure 1 are denoted by the same reference numerals.

[0042] In Figure 2, the voltage multiplier 12 comprises am integrated circuit 23 commercially available as part MAX 861, four capacitances 16, 17, 18, 19, and three diodes 20, 21, 22, connected as shown in the Figure.

[0043] The integrated circuit, which may be powered at a low voltage on the order of 3V, is supplied the voltage V1 and functions intrinsecally as a switch which periodically connects and disconnects one of its terminals, 24, from ground.

[0044] When the switch is closed, the two capacitances 16 and 18 are connected in parallel between the voltage V1 and ground and are charged at the voltage V1 (the capacitance 18 through the diode 21).

[0045] When the switch is open, the two capacitances 16 and 18 are connected in series to each other and to the voltage V1 and a voltage of 3∗V1 is present on the anode of the diode 22.

[0046] This voltage is applied to the capacitance 19 through the diode 22.

[0047] The capacitance 19 is then charged, by several close/open cycles of the switch to a value +VT very close to 3∗V1 and available at an output terminal 25 of the voltage multiplier 12, as the auxiliary supply voltage of the control circuit 5.

[0048] The control circuit 5 comprises two differential amplifiers 26, 27, the resistors 28, 29, 30, 32 and two capacitances 33, 34.

[0049] The two amplifiers 26, 27 available in the form of a single integrated circuit as part LM 358 are supplied the voltage +VT generated by the voltage mulltiplier 12.

[0050] The non-inverting input of the amplifier 26 is connected to the terminal 2 via the resistor 28.

[0051] The inverting input is connected to the output terminal 4 of the constant voltage drop regulator via the resistor 29.

[0052] The resistor 30 connected between the inverting input and the output of the amplifier 26 defines together with the resistor 29 the gain of the amplifier, which functions as a voltage follower with a gain A defined by equation Eo=(RF+R1)/R1.AV=A.ΔV , where Eo is the output voltage from the amplifier as referred to the voltage (V1-ΔV) applied to the inverting input through the resistor 29.

[0053] ΔV is the voltage applied to the inputs through the input resistors 28, 29, and corresponding to the drain-source voltage drop of the MOSFET 1, RF is the value of the resistor 30 and R1 is the value of the resistor 29.

[0054] The capacitance 33 in parallel with the resistor 30 defines the amplifier cut off frequency and together with the capacitance 34, connected between the non-inverting input of the amplifier and ground ensures the regulating loop stability.

[0055] The output of the amplifier 26 is connected to the non-inverting input of the amplifier 27, which receives a reference voltage VREF on the inverting input.

[0056] The voltage VREF is generated by a Zener diode 9 with the anode connected to the source terminal of the MOSFET 1 and the cathode connected to the auxiliary supply voltage +VT through a resistor 31.

[0057] The closing of the Zener current back toward ground, independently of the load, is ensured by a resistor 35 connected between the output terminal 4 and ground.

[0058] Calling VZ the Zener voltage evidently is with reference to the voltage (V1-ΔV): VREF=VZ.

[0059] At the output of the amplifier 27, not inversely fed back and hence with a very high intrinsic gain A1, there is a voltage E1=A1(AΔV-VZ) which is applied to the control gate of the MOSFET 1 via the resistor 32.

[0060] By suitably selecting the gain A, it becomes possible to obtain a suitable value AΔV comparable to the Zener voltage of a Zener diode or equivalent device stable in temperature and on the order of 2.5-3V.

[0061] The error signal E1 can then vary practically between 0 and VT, as a function of very small variations of ΔV above or below a desired value, jointly defined by VZ/A.

[0062] The voltage of the error signal has adequate levels to control in a continuous manner the conductivity of the MOSFET such that the voltage drop ΔV is constant.

[0063] In addition, the regulating circuit described lends itself for an easy match of the voltage drop of the regulator to fill a variety of demands.

[0064] In fact, since ΔV=VZ/A and the gain A is defined by (RF+R1)/R1
by varying the value of RF (resistor 30) or R1 (resistor 29) it becomes possible to set ΔV without the reference voltage generator requiring alteration or replacement.

[0065] In particular, it becomes possible to use resistors R1 with a different value according to necessity and in the extreme to substitute an adjustable resistance potentiometer for a fixed value resistor (selected from R1 and RF).

[0066] Figure 2 only illustrates a preferred embodiment and it is apparent that many changes may be made.

[0067] For example, the MOSFET 1 may be replaced by a plurality of MOSFET devices in parallel to increase the maximum power from the voltage regulator. In this case it may be best to control the gate electrode of the MOSFETs with the intermediary of a bipolar transistor of the PNP type in an emitter follower configuration with the emitter connected to the voltage source +VT through a resistor of suitable value, the collector connected to the output terminal 4 (or to ground) and the base connected to the output of the amplfier 27 through a resistor of suitable value.

[0068] The gate electrodes of the MOSFETs are then connected to the emitter of the transistor, through a resistor of suitable value.

[0069] In this case to ensure a current circulation path from the collector of the transistor toward ground, also in the absence of a load on the regulator output it is necessary that the terminal 4 be connected to ground through a resistor of suitable value (possibly the same resistor 35 which ensures circulation of the zener current).

[0070] As a further modification, the Zener diode 9

may be replaced by a plurality of diodes in series, forward biased or by a reference voltage generating integrated circuit, such as the circuit known commercially as part TL431.

[0071] It would also be possible to use a transistor of the NPN type, again in an emitter follower configuration.

[0072] In this case the collector is connected to the voltage source +VT and the emitter connected to ground and to the gate electrode of the MOSFETs through suitable resistors.

[0073] Figure 3 shows by way of example a regulator which is similar to that shown in Figure 2 and incorporates some of the various modifications previously described, namely:

- two MOSFETs 1A, 1B instead of one MOSFET,
- a plurality of forward biased diodes 91, 92, 93,
- a transistor 50 of the PNP type, in an emitter follower configuration, with the emitter connected to the voltage +VT through a resistor 51 and to the gate electrode of the MOSFETs through a resistor 52.

[0074] The collector is connected to the output terminal 4.

[0075] The base is connected to the output of the amplifier 27 via a resistor 54.

[0076] The other circuit elements are functionally identical with those in Figure 2 and denoted by the same reference numerals.

Claims

1. A constant voltage drop voltage regulator for obtaining, from a first regulated voltage (V1) applied to an input (2) of said regulator, a second voltage (V2) lower than said first voltage (V1) and differring by a predetermined value therefrom, said second voltage (V2) being available at an output (4) of said regulator, comprising:

   - a MOSFET transistor (1) with an N-type channel and the drain electrode connected to said input (2) and the source electrode connected to said output (4),
   - a first means (11,32,54,50,52) for applying an error signal to the gate electrode of said MOSFET (1),
   - a second means (26) connected to said input (2) and said output (4) to generate a voltage signal proportional to the voltage drop across said input and said output,
   - a generator of reference voltage (9) relative to the voltage at said output (4), and
   - a third means (27) connected to said second means (26) and said reference voltage generator (9) to generate said error signal having a voltage related to the error between said voltage signal and said reference voltage (VREF) .

2. The voltage regulator of Claim 1, wherein said first regulated voltage is on the order of some volts and said second voltage differs with said first voltage by fractional volts, comprising a voltage multiplier (12) which is supplied said first voltage (V1) to generate an auxiliary voltage (VT) being a multiple of said first voltage (V1), said second and third means (26,27) and said reference voltage generator (9) being supplied said auxiliary voltage (VT).

3. The voltage regulator of Claim 2, wherein said second means (26) comprises an operational amplifier operated as a voltage follower with gain, being input said voltage drop across said input (2) and output (4), and said third means (27) comprises a differential amplifier having an inverting input connected to said reference voltage generator (9) to receive said reference voltage (VREF) and a non-inverting input connected to the output of said operational amplifier.

4. The voltage regulator of Claim 3, wherein said first means (11,32,54,50,52) comprises a current limiting resistor for connecting the output of said differential amplifier to the gate electrode of said MOSFET (1).

5. The voltage regulator of Claim 3, wherein said first means (11,32,54,50,52) comprises a transistor of the PNP type in an emitter follower configuration with the emitter being connected to said auxiliary voltage (VT) via a first resistor (51), the collector connected to the output (4) of said regulator and the base connected, via a second resistor, to the output of said differential amplifier, the emitter being also connected, via a third resistor, to the gate electrode of said MOSFET (1).

6. The voltage regulator of Claim 3, wherein said first means comprises a transistor of the NPN type in an emitter follower configuration with the collector connected to said auxiliary voltage (VT), the emitter connected to ground via a first resistor, and the base connected, via a second resistor, to the output of said differential amplifier, the emitter being also connected, via a third resistor, to the gate electrode of said MOSFET.

Patentansprüche

1. Konstantspannungsabfall-Spannungsregler, um ausgehend von einer an einen Eingang (2) des Reglers angelegten ersten geregelten Spannung (V1) eine zweite Spannung (V2) zu erhalten, die kleiner als die erste Spannung (V1) ist und sich da-

von um einen bestimmten Wert unterscheidet und an einem Ausgang (4) des Reglers abgreifbar ist, umfassend:

- einen MOSFET-Transistor (1) mit einem n-Kanal und einer an den Eingang (2) angeschlossenen Drainelektrode und einer an den Ausgang (4) angeschlossenen Sourceelektrode,
- erste Mittel (11, 32, 54, 50,52) zum Anlegen eines Fehlersignals an die Gateelektrode des MOSFET (1),
- an den Eingang (2) und den Ausgang (4) angeschlossene zweite Mittel (26) zur Erzeugung eines zu dem Spannungsabfall zwischen dem Eingang und dem Ausgang proportionalen Spannungssignals,
- einen Generator einer auf die Spannung an dem Ausgang (4) bezogenen Referenzspannung (9), und
- an die zweiten Mittel (26) und den Referenzspannungsgenerator (9) angeschlossene dritte Mittel (27) zur Erzeugung des Fehlersignals, welches eine dem Fehler zwischen dem Spannungssignal und der Referenzspannung (VREF) entsprechende Spannung aufweist.

2. Spannungsregler nach Anspruch 1,

wobei die erste geregelte Spannung in der Größenordnung von einigen Volt liegt und sich die zweite Spannung von der ersten Spannung um einen Bruchteil von einem Volt unterscheidet, mit einem Spannungsvervielfacher (12), an den eine erste Spannung (V1) angelegt ist, um eine einem Vielfachen der ersten Spannung (V1) entsprechende Hilfsspannung (VT) zu erzeugen, wobei die Hilfsspannung (VT) an die zweiten und dritten Mittel (26, 27) und den Referenzspannungsgenerator (9) angelegt ist.

3. Spannungsregler nach Anspruch 2,

wobei die zweiten Mittel (26) einen Operationsverstärker umfassen, der als Spannungsfolger mit Verstärkung betrieben wird und den Spannungsabfall zwischen dem Eingang (2) und dem Ausgang (4) empfängt, und
wobei die dritten Mittel (27) einen Differenzverstärker umfassen, der einen an den Referenzspannungsgenerator (9) angeschlossenen invertierenden Eingang zum Empfang der Referenzspannung (VREF) und einen an den Ausgang des Operationsverstärkers angeschlossenen nicht - invertierenden Eingang aufweist.

4. Spannungsregler nach Anspruch 3,

wobei die ersten Mittel (11, 32, 54, 50, 52) einen strombegrenzenden Widerstand zur Verbindung des Ausgangs des Differenzverstärkers mit der Gateelektrode des MOSFET (1) umfassen.

5. Spannungsregler nach Anspruch 3,

wobei die ersten Mittel (11, 32, 54, 50, 52) einen pnp-Transistor in einer Emitterfolgeranordnung umfassen, wobei der Emitter über einen ersten Widerstand (51) an die Hilfsspannung (VT), der Kollektor an den Ausgang (4) des Reglers und die Basis über einen zweiten Widerstand an den Ausgang des Differenzverstärkers angeschlossen ist, und wobei der Emitter zudem über einen dritten Widerstand an die Gateelektrode des MOSFET (1) angeschlossen ist.

6. Spannungsregler nach Anspruch 3,

wobei die ersten Mittel einen npn-Transistor in einer Emitterfolgeranordnung umfassen, wobei der Kollektor an die Hilfsspannung (VT), der Emitter über einen ersten Widerstand an Erde und die Basis über einen zweiten Widerstand an den Ausgang des Differenzverstärkers angeschlossen ist, und wobei der Emitter zudem über einen dritten Widerstand an die Gateelektrode des MOSFET angeschlossen ist.

Revendications

1. Régulateur de tension à chute de tension constante pour l'obtention, à partir d'une première tension régulée (V1) appliquée à une entrée (2) du régulateur, d'une deuxième tension (V2) inférieure à la première (V1) et qui en diffère d'une valeur prédéterminée, cette deuxième tension (V2) étant disponible à une sortie (4) du régulateur, comprenant :

- un transistor MOS (1) à canal du type N dont le drain est relié à l'entrée (2) et la source reliée à la sortie (4),
- un premier moyen (11, 32, 54, 50, 52) pour l'application d'un signal d'erreur à la grille du transistor MOS (1),
- un deuxième moyen (26) relié à l'entrée (2) et à la sortie (4) et produisant un signal de tension proportionnel à la chute de tension entre l'entrée et la sortie,
- un générateur de tension de référence (9) relative à la tension à la sortie (4), et
- un troisième moyen (27) relié au deuxième moyen (26) et au générateur de tension de référence (9) et produisant le signal d'erreur ayant une tension en relation avec l'erreur entre le signal de tension et la tension de référence

(VREF).

2. Régulateur de tension selon la revendication 1, dans lequel la première tension régulée est de l'ordre de quelques volts et la deuxième tension diffère de la première d'une fraction de volt, comprenant un multiplicateur de tension (12) qui est alimenté par la première tension (V1) et produit une tension auxiliaire (VT) multiple de celle-ci, le deuxième moyen (26), le troisième moyen (27) et le générateur de tension de référence (9) étant alimentés par cette tension auxiliaire (VT).

3. Régulateur de tension selon la revendication 2, dans lequel le deuxième moyen (26) comprend un amplificateur opérationnel qui fonctionne en suiveur de tension à gain et à une entrée duquel est appliquée la chute de tension entre l'entrée (2) et la sortie (4), et le troisième moyen (27) comprend un amplificateur différentiel qui a une entrée inverseuse reliée au générateur de tension de référence (9) pour recevoir la tension de référence (VREF) et une entrée non inverseuse reliée à la sortie de l'amplificateur opérationnel.

4. Régulateur de tension selon la revendication 3, dans lequel le premier moyen (11, 32, 54, 50, 52) comprend une résistance de limitation de courant qui relie la sortie de l'amplificateur différentiel à la grille du transistor MOS (1).

5. Régulateur de tension selon la revendication 3, dans lequel le premier moyen (11, 32, 54, 50, 52) comprend un transistor du type PNP en montage émetteur-suiveur avec l'émetteur relié à la tension auxiliaire (VT) par l'intermédiaire d'une première résistance (51), le collecteur relié à la sortie (4) du régulateur et la base reliée par l'intermédiaire d'une deuxième résistance à la sortie de l'amplificateur différentiel, l'émetteur étant aussi relié par l'intermédiaire d'une troisième résistance à la grille du transistor MOS (1).

6. Régulateur de tension selon la revendication 3, dans lequel le premier moyen comprend un transistor du type NPN en montage émetteur-suiveur avec le collecteur relié à la tension auxiliaire (VT), l'émetteur relié à la masse par l'intermédiaire d'une première résistance et la base reliée par l'intermédiaire d'une deuxième résistance à la sortie de l'amplificateur différentiel, l'émetteur étant aussi relié par l'intermédiaire d'une troisième résistance à la grille du transistor MOS.

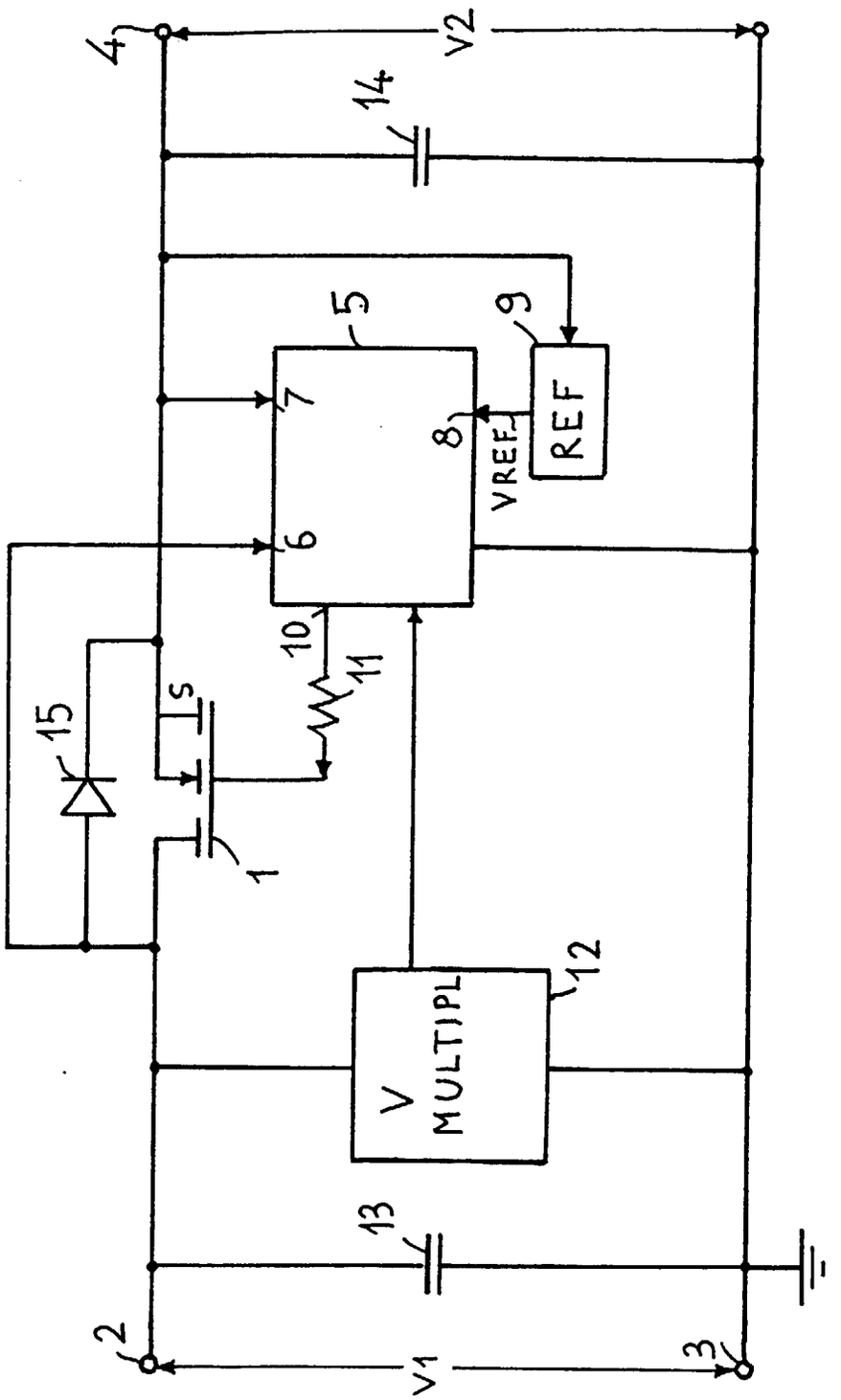
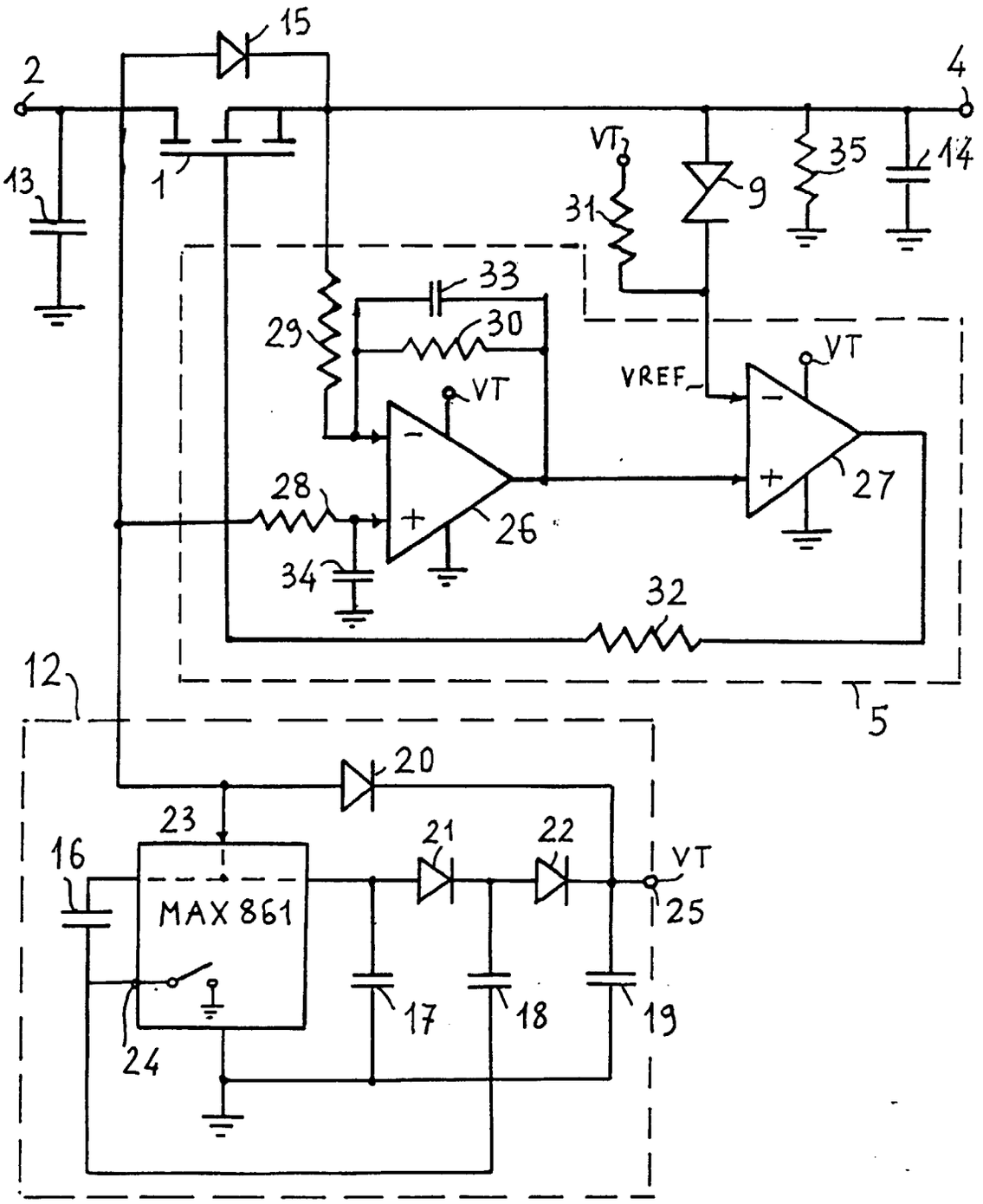


FIG. 1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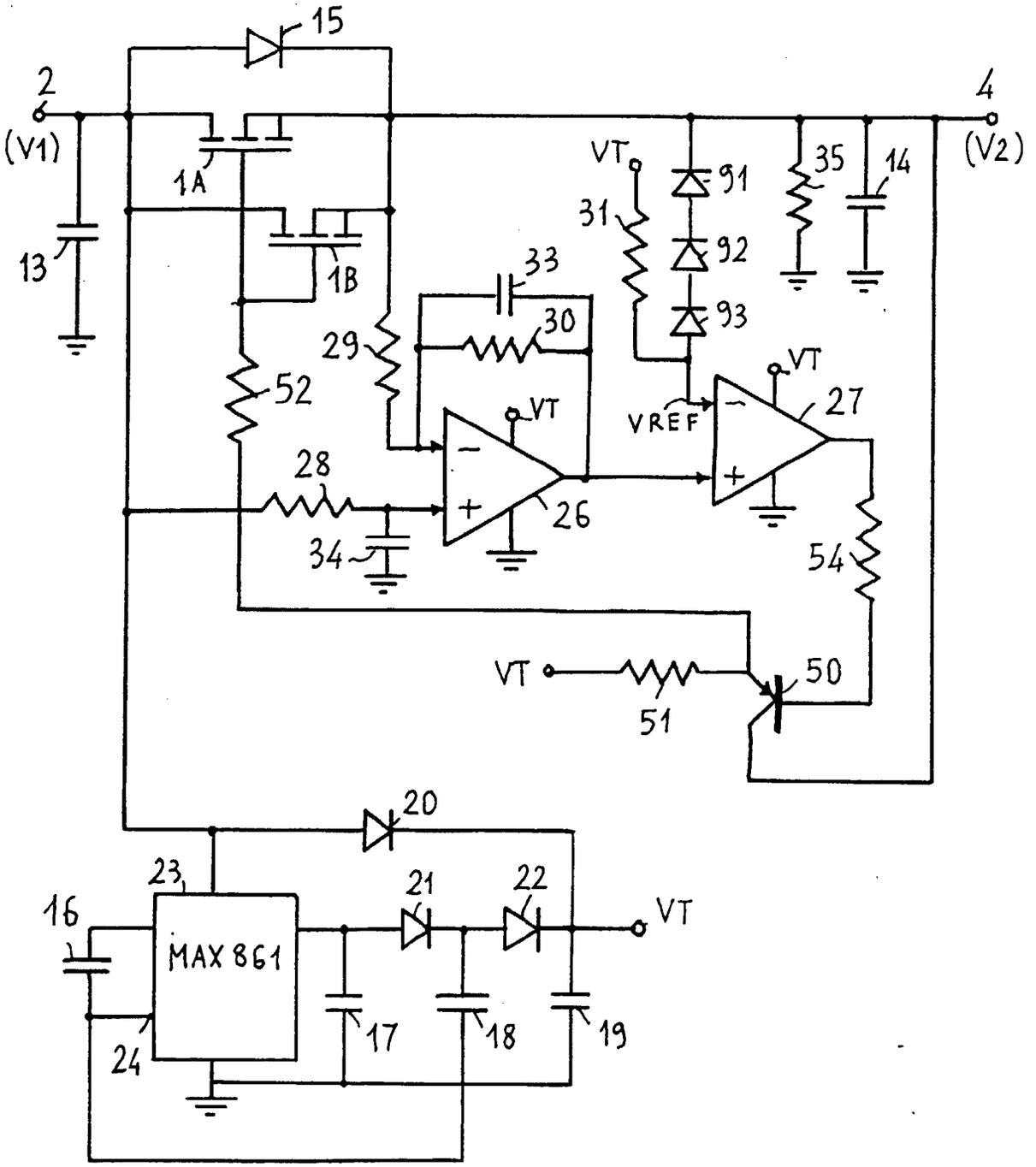
12
5
20
23
16
MAX 861
21
22
VT
25
17
18
19
24

FIG. 2


15
2
(V1)
4
(V2)
1A
1B
13
VT
91
92
93
31
35
14
33
30
29
52
VT
VREF
27
28
26
34
54
VT
51
50
20
23
16
MAX 861
21
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VT
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19
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FIG.3