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(54) Voltage-clamped power accumulation-mode MOSFET

Spannungsbegrenzter Leistungs-Anreicherungs-MOSFET

MOSFET à accumulation de puissance avec limite en tensim

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- **PATENT ABSTRACTS OF JAPAN vol. 94, no. 010 & JP 06 302808 A (TOYOTA AUTOM LOOM WORKS LTD), 28 October 1994,**
- **PATENT ABSTRACTS OF JAPAN vol. 013, no. 525 (E-850), 22 November 1989 & JP 01 215067 A (HITACHI LTD), 29 August 1989,**
- **TSENGYOU SYAU ET AL: "COMPARISON OF ULTRALOW SPECIFIC ON-RESISTANCE UMOSFET STRUCTURES: THE ACCUFET, EXTFET, INVFET, AND CONVENTIONAL UMOSFET'S" 1 May 1994 , IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 41, NR. 5, PAGE(S) 800 - 808 XP000483878 * abstract; figure 7 ***

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Description

[0001] This invention relates to power accumulation-mode field-effect transistors and, in particular, to a power accumulation-mode field-effect transistor having a greater voltage blocking capability according to the preamble of claim 1.

[0002] Such a accumulation-mode field-effect transistor is known from T. Syau et al., "Comparison of Ultralow Specific On-Resistance UMOSFET Structures: The ACCUFET, EXTFET, INVFET, and Conventional UMOSFET's", IEEE Electron Device Letters, Vol. 41, No. 5, May 1994, pp. 800-808.

[0003] Accumulation mode field-effect transistors, sometimes referred to as "ACCUFETs", are trench-type MOSFETs which contain no body region and hence no PN junctions. The region between the trenched gates, sometimes called a "mesa", is made relatively narrow (e.g., 0.5 to 4.0 μm wide), and the gate material (typically polysilicon) is doped in such a way that it has a work function which depletes the entire mesa region, much like a junction field-effect-transistor (JFET). The current path extends between a "source" at the top of the mesa and a "drain" at the bottom of the substrate. The trenches are normally formed entirely in an epitaxial layer which is grown on top of the substrate.

[0004] A cross-sectional view of a typical ACCUFET 10 is illustrated in Fig. 1. Trenched gates 11 are etched in a silicon material 12, which includes an N-epitaxial layer 13 grown on an N+ substrate 14. Trenched gates 11 define two cells 10A and 10B. An N+ source 15 is formed at the top of the mesa between gates 11. A metal layer 16 is formed over the source regions, and a power source 17 and a load 18 are connected between the N+ source 15 and the N+ substrate 14, which acts as the drain.

[0005] ACCUFET 10 is turned off when the gate voltage is equal to the source voltage (i.e., $V_{gs} = 0$). If V_{gs} is increased, the depletion regions surrounding the gates (shown by the dashed lines) contract and open a current path between the source and the drain. With further increasing V_{gs} the depletion regions continue to contract until eventually accumulation regions are formed adjacent the trenches, enhancing channel conduction and further lowering the on-resistance of the device.

[0006] This sequence of events is illustrated in Figs. 2A, 2B and 2C, Fig. 2A showing ACCUFET 10 in the off condition, Fig. 2B showing ACCUFET 10 turned partially on, and Fig. 2C showing ACCUFET 10 turned fully, with the accumulation regions being designated by the numerals 19. In Figs. 2B and 2C the arrows represent the flow of electrons from the source to the drain.

[0007] At the beginning mentioned ACCUFET differs lightly from the structure depicted in Fig. 1. On one side of the trench there is additional a p-type diffusion under the N+ source regions beneath the contacts so to restrict the current flow between source and drain to the trench area.

[0008] Additional information concerning ACCUFETs is given in U.S. Patent No. 4,903,189 to Ngo et al.; B. J. Baliga et al., "The Accumulation-Mode Field-Effect Transistor: A New Ultralow On-Resistance MOSFET" and, IEEE Electron Device Letters, Vol. 13, No. 8, August 1992, pp. 427-429; each of which is incorporated herein by reference in its entirety.

[0009] ACCUFETs can be fabricated with a very high cell density and a very low on-resistance. Despite these advantages, ACCUFETs have not so far achieved widespread use in the field of power semiconductor devices for several reasons. One of the principal reasons is their inability to withstand high voltages when they are in an off condition.

[0010] This problem is illustrated in Figs. 3A and 3B, which shown oxide layers 11A bordering gates 11. Fig. 3A shows ACCUFET 10 connected to an inductive load 30. The symbols t_0, t_1, t_2, t_3 and t_4 represent sequential times in the process of turning off ACCUFET 10. The dashed lines in Fig. 3A represent the edges of the spreading depletion region at times t_0, t_1, t_2, t_3 and t_4. Fig. 3B illustrates the strength of the electric field in the gate oxide layer 11A and epitaxial layer 13 at times t_0, t_1, t_2, t_3 and t_4. As shown, as V_{gs} begins to decrease at time t_0, the electric field resides in the gate oxide layer 11A and a portion of epitaxial layer 13. At times t_1 and t_2, the strength of the field in the gate oxide layer 11A has increased somewhat, but a portion of the increase is absorbed by the epitaxial layer 13. At time t_2, however, the electric field has reached the interface between epitaxial layer 13 and N+ substrate 14. Since N+ substrate 14 is heavily doped, it cannot support an electric field to any significant extent, and thus all further increases in the field must be taken up in the limited space of gate oxide layer 11A and epitaxial layer 13. This means that the electric field in the gate oxide layer 11A begins to increase at a faster rate with decreases in V_{gs}. Unless limited in some way, the increases may eventually rupture gate oxide layer 11A, and in Fig. 3B this is shown as occurring at time t_4. When the gate oxide layer has been ruptured, the device is generally destroyed beyond repair.

[0011] Since many loads (such as load 30) include an inductive component, voltage spikes inevitably occur in the power lines as the loads are switched on and off. The inability of ACCUFETs to withstand these voltage spikes has seriously limited their use in the power MOSFET field.

[0012] Push-pull halfbridge circuit 40, shown in Fig. 4A, illustrates the problem that occurs when using ACCUFETs with an inductive load. Halfbridge circuit 40 includes a high-side ACCUFET 41 and a low-side ACCUFET 42, which drive a coil 43 in a motor, for example. ACCUFETs 41 and 42 are connected in series between a battery voltage V_{batt} and ground. Fig. 4B shows the voltages (V_{GS}) across the gate oxides of the ACCUFETs 41 and 42 and the voltage V_o at the output of the halfbridge circuit. Assume that at a starting point, V_o is low, meaning that high-side ACCUFET 41 is off and low-side ACCUFET 42 is on. With ACCUFET 42 on, generally some current will be flowing through ACCUFET 42 and coil 43. In this situation the gate of ACCUFET 42 is tied to V_{batt} and the gate of ACCUFET 41 is tied to a voltage equal to V_o, so that the V_{GS} in ACCUFET 41 is zero.

[0013] In order to switch V_o from low to high, low-side ACCUFET 42 is turned off and then high-side ACCUFET 41 is turned on. Both ACCUFETs cannot be on at the same time, however, or a direct current path from V_{batt} to ground would be created, leading to a large current and most likely the destruction of both devices. Thus, at time T_1 in Fig. 4B, ACCUFET 42 is turned off by switching its gate voltage from V_{batt} to ground. However, current flowing through coil 43 resists an abrupt cutoff, and V_o therefore increases rapidly to a level greater than V_{batt}, as shown by the top curve in Fig. 4B. V_o will increase until ACCUFET 42 either breaks down or is destroyed. Meanwhile, the V_{GS} in ACCUFET 41 falls rapidly at an equal rate (its source being biased more positively than its gate). It is highly likely that in this situation the gate oxide of ACCUFET 41 will rupture before ACCUFET 42 begins to conduct and thereby attempt to clamp the output voltage V_o.

[0014] A scenario similar to that shown in Figs. 4A-4B will occur in virtually any situation in which an ACCUFET is used to switch currents through an inductive load.

[0015] To complete the picture it is mentioned a MOSFET disclosed in EP-A-0583022 where between two trenches is formed a highly doped region to define a curved PN junction in the middle thereof such that the point at which the MOSFET would avalanche in operation is moved away from the trench corners into the bulk of the semiconductor material and therefore to reduce the formation of hat carrier injection into the gate insulating layer.

[0016] Accordingly, the object of this invention is to provide a device which has the superior cell density and on-resistance characteristics of an ACCUFET yet is able to switch an inductive load or survive voltage spikes of limited energy in a reliable manner particularly without damaging the trench gate.

[0017] The object of the invention is achieved in accordance with the characterising part of claim 1.

[0018] The ACCUFET of this invention includes a plurality of cells bordered by trench gates and containing semiconductor material of a selected conductivity. Each of the trench gates includes a conductive gate material, typically polysilicon, and an insulating layer, typically silicon dioxide, which insulates the conductive gate material from the semiconductor material in each cell. In order to limit the electric field imposed on the gate oxide layer, a protective region of conductivity opposite of that of the semiconductor material in the cell is created, thereby creating a PN junction which acts as a protective diode connected in parallel with the current path through the ACCUFET cell. The doping levels and location of the PN junction are set so as to establish a breakdown voltage for the diode which prevents the voltage across the gate oxide layer from reaching a level which would cause the gate oxide layer to rupture or be damaged. The diode should also clamp and therefore minimize the maximum silicon electric field in the vicinity of the gate to minimize or prevent the formation of hot carriers.

[0019] In the preferred embodiment, the protective region of conductivity opposite to the conductivity of the ACCUFET cells is formed in an adjacent cell. The cells may be in the form of longitudinal stripes or they may have a hexagonal, square, polygonal or other shape. Preferably, the protective regions are formed in a repetitive pattern across the ACCUFET such there is one protective region for a selected number of ACCUFET cells.

[0020] Embodiments of the invention will now be described by way of examples with reference to the accompanying drawings, in which:

[0021] Fig. 1. illustrates a cross-sectional view of a conventional accumulation-mode MOSFET (ACCUFET).

[0022] Fig. 2A illustrates an ACCUFET in an off condition; Fig. 2B illustrates a partially-on ACCUFET; and Fig. 2C illustrates a fully-on ACCUFET.

[0023] Fig. 3A illustrates the changes in the depletion region as an ACCUFET changes from an on condition to an off condition.

[0024] Fig. 3B illustrates schematically the strength of the electric field in the gate oxide layer and epitaxial layer of the ACCUFET of Fig. 3A as it changes from an on condition to an off condition.

[0025] Fig. 4A illustrates a push-pull halfbridge circuit containing two ACCUFETs connected to an inductive load.

[0026] Fig. 4B illustrates graphs which show the voltages at the output of the bridge circuit and across the gate oxides of the ACCUFETs shown in Fig. 4A.

[0027] Fig. 5A illustrates a cross-sectional view of a voltage-clamped ACCUFET in accordance with the invention.

[0028] Fig. 5B illustrates a diagram of an equivalent circuit for the ACCUFET shown in Fig. 5A.

[0029] Figs. 6A and 6B show three-dimensional cross-sectional views of alternative ACCUFET structures in accordance with the invention, Fig. 6A showing a square cell structure and Fig. 6B showing a striped cell structure.

[0030] Fig. 7 illustrates a top view of the ACCUFET shown in Fig. 6B.

[0031] Fig. 8 shows an alternative embodiment in accordance with the invention wherein the gate trenches extend into the heavily-doped substrate.

[0032] Figs. 9A-9E illustrate the steps of a process for fabricating the ACCUFET shown in Fig. 5A.

[0033] An ACCUFET in accordance with the invention is shown in Fig. 5A. ACCUFET 50 includes trench gates 51A and 51B formed in an N-epitaxial layer 52 which is grown on the surface of an N+ substrate 53. Gates 51A and 51B are insulated from an epitaxial layer 52 by gate oxide layers 54A and 54B, respectively. A shallow N+ region 55 at the surface of epitaxial layer 52 makes contact with a metal layer 56. N-epitaxial layer 52 would typically be doped to a concentration of 1 x 10^{14} to 1 x 10^{15} cm^{-3}. Gates 51A and 51B are preferably polysilicon doped with boron to a concentration of 8 x 10^{18} to 5 x 10^{19} cm^{-3}. Gate oxide layers 54A and 54B are typically 90-1000Å thick, and the distance between gates 51A and 51B is typically about 1.0 μm but may range from 0.5 to 4.0 μm.

[0034] N+ substrate 53 serves as the drain of ACCUFET 50 and may be contacted from the bottom. Alternatively, a submerged N+ layer instead of the N+ substrate could be used as the drain, and the drain could be contacted from the top side of the structure by means of, for example, an N+ sinker region and a top side contact. To provide protection for gate oxide layers 54A and 54B, a deep P+ region 57 is formed in epitaxial layer 52, creating a PN junction which functions as a diode (symbolized as diode D1).

[0035] Fig. 5B shows an equivalent circuit for the ACCUFET shown in Fig. 5A. As indicated, diode D1 is in parallel with the main current path through ACCUFET 50. It should be noted that integrating diode D1 inside of ACCUFET 50 achieves a different result from simply placing an external diode in parallel with an ACCUFET. An integrating the diode, series inductance in the diode (which occurs in a discrete, multichip or PCB version) is eliminated, allowing the diode to clamp the internal voltages within the ACCUFET nearly instantaneously (no overshoot). Moreover, the diodes can be distributed throughout the device to provide a uniform degree of clamping.

[0036] As noted above, the voltages at the gates 51A and 51B and the source (N+ region 55) are essentially the same when MOSFET 50 is turned off. Since N+ region 55 is tied to deep P+ region 57 via metal layer 56, when MOSFET 50 is turned off the voltage across gate oxides 54A and 54B cannot exceed the voltage across diode D1. If diode D1 is reverse-biased, the voltage across diode D1 is limited to its breakdown voltage; if diode D1 is forward-biased, then the voltage across diode D1 is limited to a normal diode drop (typically about 0.7 V).

[0037] The breakdown voltage of diode D1 is established by controlling the respective doping concentrations of deep P+ region 57, N-epitaxial layer 52 and N+ substrate 53, as well as the separation between PN junction 58 and the interface between N-epitaxial layer 52 and N+ substrate 53. For a normal ACCUFET, the doping concentration of N-epitaxial layer 52 would be in the range of 10^{14} to 10^{15} cm^{-3} to permit the ACCUFET to be turned off. N+ substrate 53 has a resistivity of 3mΩ-cm, and deep P+ region 57 has a sheet resistance of 40 to 150 Ω/□. N-epitaxial layer 52 is 2.5 to 5.0μm thick, but the net thickness from the bottom of deep P+ region 57 to N+ substrate 53 is 0.3 to 1.5 μm.

[0038] Figs. 6A and 6B show three-dimensional cross-sectional views of alternative ACCUFET structures in accordance with this invention. ACCUFET 60 shown in Fig. 6A is formed with a pattern of square or rectangular cells, with a deep P+ region 61 being formed in one of the cells. In ACCUFET 62 shown in Fig. 6B the cells are formed in stripes, with a deep P+ region 63 occupying one of the cells.

[0039] Fig. 7 illustrates a top view of MOSFET 62 shown in Fig. 6B, with the cross-section of Fig. 6B being shown as VIB-VIB. As indicated, a number of contacts connect a metal contact layer (not shown) to N+ source regions 64 and 65 and P+ region 63. An N+ region 67, formed at the perimeter of the structure, is used to make contact with the N+ substrate. Alternatively, the N+ substrate could be contacted from the back side.

[0040] Fig. 8 illustrates an alternative embodiment including a MOSFET 80 in which the trench gates 81 extend into the N+ substrate 82. Since N+ substrate 82 is unable to support a significant voltage difference, the gate oxide layers 85 are exposed to the entire voltage difference across the ACCUFET when it is turned off. In other words, there is no lightly-doped N-epitaxial layer to absorb a portion of the voltage drop across the device. As a result, the doping concentrations of P+ region 83 and N+ substrate 82 must be carefully established such that diode D2 breaks down before gate oxide layer 85 ruptures. According to the industry standard, the gate oxide layer should not be exposed to a voltage difference of more than 4 MV/cm times the thickness of the oxide layer expressed in cm. For example, a gate oxide layer 400Å thick will rupture at about 32V, and the breakdown voltage of diode D2 should therefore be about 16V. With a gate oxide layer 175Å thick, a clamping voltage of about 8V is needed.

[0041] Although there are numerous processes for fabricating an ACCUFET in accordance with this invention, Figs. 9A-9E illustrate an exemplary process for fabricating ACCUFET 50 shown in Fig. 5A.

[0042] Referring to Fig. 9A, the starting point is a conventional N+ substrate 53 on which an N-epitaxial layer 52 is grown using known processes.

[0043] A thick oxide layer 90 is grown, masked and etched, and a thin oxide layer 91 is grown on the top surface of the structure where deep P+ region 57 is to be formed. Deep P+ region 57 is then implanted through thin oxide layer 91 at a dose of 1 x 10^{14} to 7 x 10^{15} cm^{-2} and an energy of 60-100 keV. The resulting structure is illustrated in Fig. 9B. Oxide layers 90 and 91 are then removed.

[0044] In one version of the process, a thick oxide layer 92 is grown and removed by photomasking except over deep P+ region 57, and a thin oxide layer 93 is grown. Thin oxide layer 93 is masked and removed from the portions of the structure where the trenches are to be formed, as shown in Fig. 19C. The trenches are then masked and etched using known techniques of reactive ion or plasma dry etching. Then the trench is oxidized to form gate oxide layers 54A and 54B, and polysilicon is deposited into the trench until it overflows the top of the trench. The polysilicon is then doped with phosphorus by $POCl_3$ predeposition or ion implantation at a dose of 5×10^{13} to 5×10^{15} cm^{-2} and an energy of 60 keV, giving it a sheet resistance of 20-70 Ω/□. For a P-channel device, the polysilicon is doped with boron using ion implantation to a sheet resistance of roughly 40-120 Ω/□. The polysilicon is then etched back until it is planar with the surface of the trench except where a mask protects it, so that it can subsequently be contacted with metal.

[0045] The N+ source region 55 is then introduced using a mask and an arsenic ion implantation (or a boron ion implantation for a P-channel device) at a dose of 5×10^{14} to 1×10^{16} cm^{-2} at 20 to 100 keV. The resulting structure is shown in Fig. 9D.

[0046] A thin oxide layer is thermally grown. Borophosphosilicate glass (BPSG) is then deposited on the surface of the structure. The BPSG is momentarily heated to around 850° to 950°C to flow smoothly and flatten the surface topology of the die. Contact holes are etched in the oxide and BPSG layers, and metal layer 56 is deposited, forming contacts through the contact holes to the N+ source region 55 and the deep P+ region 57. This yields ACCUFET 50 shown in Fig. 9E. The die is then passivated with SiN or low-temperature BPSG, and pad mask windows are etched to facilitate bonding.

[0047] While specific embodiments of this invention have been described, it should be understood that such embodiments are illustrative only and not limiting.

Claims

1. An accumulation-mode field-effect transistor (50, 60, 62, 80) comprising

a) a semiconductor material of a first conductivity type;

b) a trench formed in said semiconductor material, said trench defining at least one transistor cell and at least one diode cell;

c) a gate (51A, 51B, 81) positioned in said trench at a first surface of said semiconductor material, said gate being separated from said semiconductor material by a gate insulating layer (54A, 54B, 85),

d) a drain region (53, 82) of said first conductivity type adjacent a second surface of said semiconductor material, opposite to said first surface;

wherein said at least one transistor cell comprises:

a heavily-doped source region (55, 64, 65, 86) of said first conductivity type located at said first surface;

a lightly-doped channel region (52, 84) of said first conductivity type adjacent said source region and adjacent said trench; said channel region being suitable for conducting a current between said source region (55, 64, 65, 86) and said drain region (53, 82);

and wherein said diode cell comprises:

a second conductivity type protective region (57, 61, 63, 83) forming a PN junction with said first conductivity type semiconductor material, thereby forming a diode (D1, D2) being connected in parallel with said channel region,

characterised in that

said diode has a breakdown voltage which is less than the voltage required to damage said gate insulating layer when said transistor is in an off condition; and said source region does not extend into said diode cell.

2. The transistor of Claim 1, **characterised in that** said trench defines in said surface a two-dimensional array of cells, each of said cells being in the shape of a closed figure and being surrounded on all sides by said trench, each cell in a first group of said cells comprising said transistor cell and each cell in a second group of said cells comprising a said diode cell.

3. The transistor of claim 2, **characterised in that** said diode cells are distributed at repetitive intervals in said two dimensional array, there being a predetermined number of transistor cells for every diode cell in said array.

4. The transistor of one of the preceding Claims, **characterised in that** said semiconductor material includes an epitaxial layer 52 formed on a substrate (53).

5. The transistor of one of the preceding Claims, **characterised in that** said trench extends only into said epitaxial layer (52).

6. The transistor of one of the preceding claims, **characterised in that** said PN junction being formed at a boundry of said protective region (57, 61, 63).

7. The transistor of Claim 4, **characterised in that** said trench extends through said epitaxial layer (84) and into said substrate (82).

8. The transistor of Claim 7, **characterised in that** said PN junction is formed at a junction between said protective region (83) and substrate (82).

9. The transistor of Claim 7 or 8 **characterised in that** said diode has a breakdown voltage which is less than 4 x 10^6 volts/centimeter multiplied by the thickness of said insulating layer expressed in centimeters.

Patentansprüche

1. Ein Anreicherungs-Feld-Effekt-Transistor (50, 60, 62, 80), der umfaßt

   a) ein Halbleitermaterial eines ersten Leitfähigkeitstyps;

   b) ein aus dem erwähnten Halbleitermaterial gebildeter Graben, wobei dieser Graben mindestens eine Transistorzelle und mindestens eine Diodenzelle begrenzt;

   c) ein in dem erwähnten Graben auf einer ersten Oberfläche des erwähnten Halbleitermaterials befindliches Gate (51A, 51B, 81), wobei dieses Gate vom erwähnten Halbleitermaterial durch eine Gate-Isolierschicht (54A, 54B, 85) getrennt ist;

   d) ein Drain-Bereich (53, 82) dieses ersten Leitfähigkeitstyps, im Anschluß an eine zweite Oberfläche des erwähnten Halbleitermaterials, gegenüber der erwähnten ersten Oberfläche;

   dadurch gekennzeichnet, daß die mindestens eine erwähnte Transistorzelle umfaßt:

   einen stark dotierten Source-Bereich (55, 64, 65, 86) des erwähnten ersten Leitfähigkeitstyps, der sich in der erwähnten ersten Oberfläche befindet;
   ein schwach dotierter Kanal-Bereich (52, 84) des erwähnten ersten Leitfähigkeitstyps im Anschluß an den erwähnten Source-Bereich und den erwähnten Graben; der erwähnte Kanal-Bereich eignet sich zum Leiten eines elektrischen Stroms zwischen dem erwähnten Source-Bereich (55, 64, 65, 86) und dem erwähnten Drain-Bereich (53, 82);

   und **dadurch gekennzeichnet, daß** die erwähnte Diodenzelle umfaßt:
   eine Schutzzone eines zweiten Leitfähigkeitstyps (57, 61, 63, 83), die mit dem erwähnten Halbleitermaterial eines ersten Leitfähigkeitstyps einen PN-Übergang, und dabei eine Diode (D1, D2) bildet, die parallel zu dem erwähnten Kanal-Bereich geschaltet ist,
   dadurch gekennzeichnet,

   daß die erwähnte Diode eine Durchbruchspannung aufweist, die kleiner ist, als die Spannung, die die erwähnte Isolationsschicht beschädigen würde, wenn der erwähnte Transistor ausgeschaltet wird;
   und **daß** sich der erwähnte Source-Bereich nicht in die erwähnte Diodenzelle erstreckt.

2. Transistor gemäß Anspruch 1, **dadurch gekennzeichnet, daß** der erwähnte Graben in der erwähnten Oberfläche eine zweidimensionale Anordnung von Zellen definiert, wobei jede der erwähnten Zellen die Form einer geschlossenen Figur hat und ringsum vom erwähnten Graben umgeben ist, und wobei jede Zelle einer ersten Gruppe erwähnter Zellen zur erwähnten Transistorzelle und jede Zelle einer zweiten Gruppe erwähnter Zellen zur erwähnten Diodenzelle gehört.

3. Transistor gemäß Anspruch 2, **dadurch gekennzeichnet, daß** die erwähnten Diodenzellen mit wiederkehrenden Lücken in der erwähnten zweidimensionalen Anordnung verteilt sind, wobei für jede Diodenzelle in der erwähnten Anordnung eine vorher festgelegte Anzahl von Transistorzellen vorhanden ist.

4. Transistor gemäß einem der vorstehenden Ansprüche, **dadurch gekennzeichnet, daß** das erwähnte Halbleitermaterial eine auf einem Substrat (53) gebildete epitaktische Schicht 52 aufweist.

5. Transistor gemäß einem der vorstehenden Ansprüche, **dadurch gekennzeichnet, daß** sich der erwähnte Graben nur in die erwähnte epitaktische Schicht (52) erstreckt.

6. Transistor gemäß einem der vorstehenden Ansprüche, **dadurch gekennzeichnet, daß** der erwähnte PN-Übergang an einer Grenze der erwähnten Schutzzone (57, 61, 63) gebildet wird.

7. Transistor gemäß Anspruch 4, **dadurch gekennzeichnet, daß** sich der erwähnte Graben durch die erwähnte epitaktische Schicht (84) und in das erwähnte Substrat (82) hinein erstreckt.

8. Transistor gemäß Anspruch 7, **dadurch gekennzeichnet, daß** der erwähnte PN-Übergang an einem Übergang von der erwähnten Schutzzone (83) zum Substrat (82) gebildet wird.

9. Transistor gemäß Anspruch 7 oder 8, **dadurch gekennzeichnet, daß** die erwähnte Diode eine Durchbruchspannung aufweist, die kleiner ist als 4 x 10^6 V/cm, multipliziert mit der Dicke der erwähnten Isolationsschicht, in cm ausgedrückt.

Revendications

1. Transistor à effet de champ de mode accumulation (50, 60, 62, 80) comprenant :

a) un matériau semiconducteur d'un premier type de conductivité ;
b) une tranchée qui est formée dans ledit matériau semiconducteur, ladite tranchée définissant au moins une cellule de transistor et au moins une cellule de diode ;
c) une grille (51A, 51B, 81) qui est positionnée dans ladite tranchée au niveau d'une première surface dudit matériau semiconducteur, ladite grille étant séparée dudit matériau semiconducteur par une couche d'isolation de grille (54A, 54B, 85) ;
d) une région de drain (53, 82) dudit premier type de conductivité adjacente à une seconde surface dudit matériau semiconducteur, opposée à ladite première surface,

dans lequel ladite au moins une cellule de transistor comprend :

une région de source lourdement dopée (54, 64, 65, 86) dudit premier type de conductivité située au niveau de ladite première surface ;
une région de canal légèrement dopée (52, 84) dudit premier type de conductivité adjacente à ladite région de source et adjacente à ladite tranchée, ladite région de canal convenant pour conduire un courant entre ladite région de source (55, 64, 65, 86) et ladite région de drain (53, 82), et

dans lequel ladite cellule de diode comprend :
une région de protection de second type de conductivité (57, 61, 63, 83) qui forme une jonction PN avec ledit matériau semiconducteur de premier type de conductivité, d'où ainsi la formation d'une diode (D1, D2) qui est connectée en parallèle à ladite région de canal,
caractérisé en ce que :

ladite diode présente une tension de claquage qui est inférieure à la tension requise pour endommager ladite couche d'isolation de grille lorsque ledit transistor est dans une condition bloquée ; et
ladite région de source ne s'étend pas dans ladite cellule de diode.

2. Transistor selon la revendication 1, **caractérisé en ce que** ladite tranchée définit, dans ladite surface, un réseau bidimensionnel de cellules, chacune desdites cellules étant selon la forme d'une figure fermée et étant entourée sur tous les côtés par ladite tranchée, chaque cellule dans un premier groupe desdites cellules comprenant ladite cellule de transistor et chaque cellule dans un second groupe desdites cellules comprenant une dite cellule de diode.

3. Transistor selon la revendication 2, **caractérisé en ce que** lesdites cellules de diode sont distribuées selon des intervalles répétitifs dans ledit réseau bidimensionnel, un nombre prédéterminé de cellules de transistor existant ainsi pour chaque cellule de diode dans ledit réseau.

4. Transistor selon l'une quelconque des revendications précédentes, **caractérisé en ce que** ledit matériau semiconducteur inclut une couche épidaxiale (52) formée sur un substrat (53).

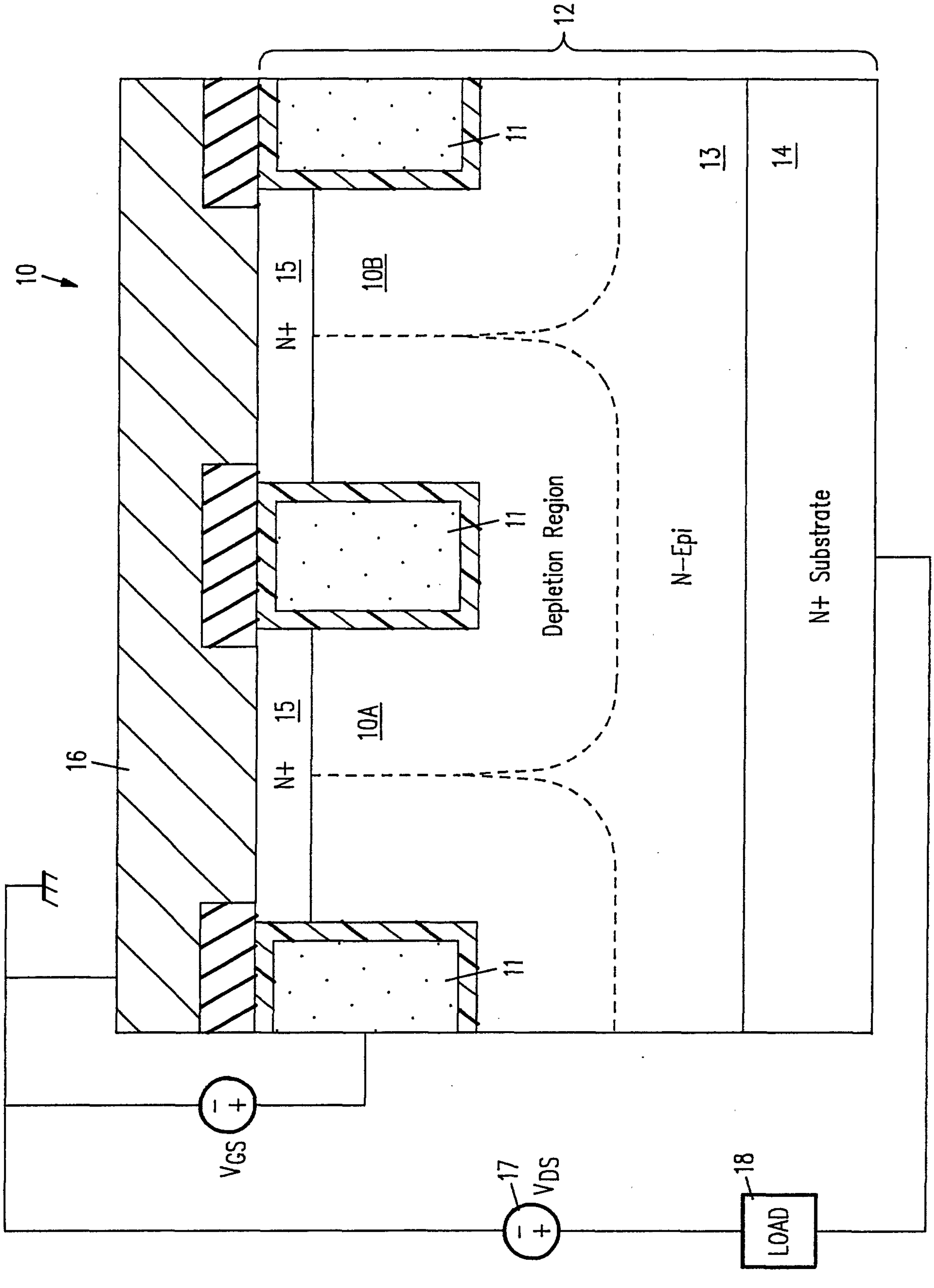
5. Transistor selon l'une quelconque des revendications précédentes, **caractérisé en ce que** ladite tranchée s'étend seulement dans ladite couche épidaxiale (52).

6. Transistor selon l'une quelconque des revendications précédentes, **caractérisé en ce que** ladite jonction PN est formée au niveau d'une frontière de ladite région de protection (57, 61, 63).

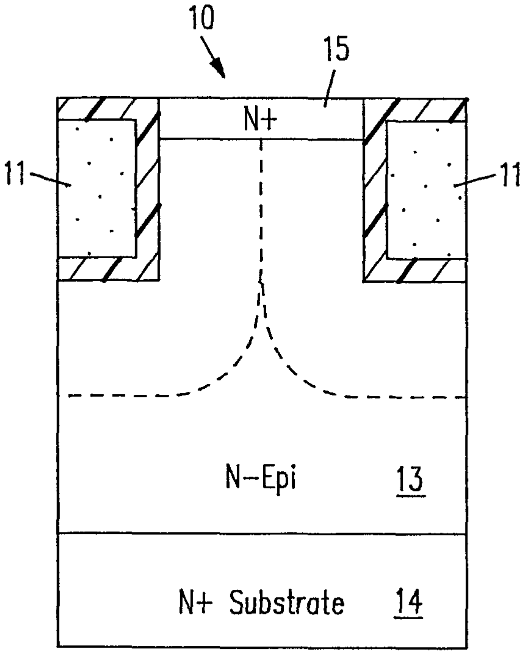
7. Transistor selon la revendication 4, **caractérisé en ce que** ladite tranchée s'étend au-travers de ladite couche épidaxiale (84) et à l'intérieur dudit substrat (82).

8. Transistor selon la revendication 7, **caractérisé en ce que** ladite jonction PN est formée au niveau d'une jonction entre ladite région de protection (83) et ledit substrat (82).

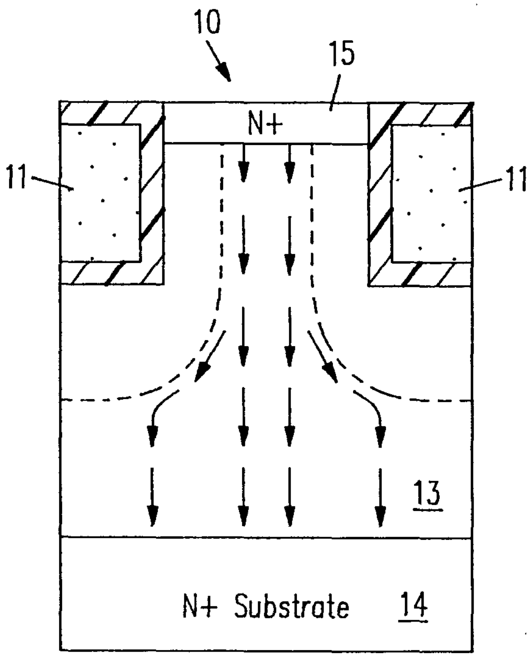
9. Transistor selon la revendication 7 ou 8, **caractérisé en ce que** ladite diode présente une tension de claquage qui est inférieure à 4 x 10^6 volts./cm x épaisseur de ladite couche isolante exprimée en centimètres.



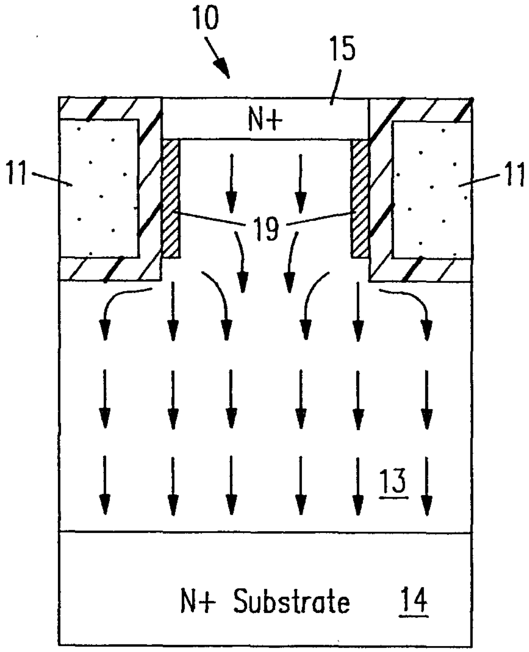
PRIOR ART
FIG. 1



PRIOR ART
FIG. 2A



PRIOR ART
FIG. 2B



PRIOR ART
FIG. 2C

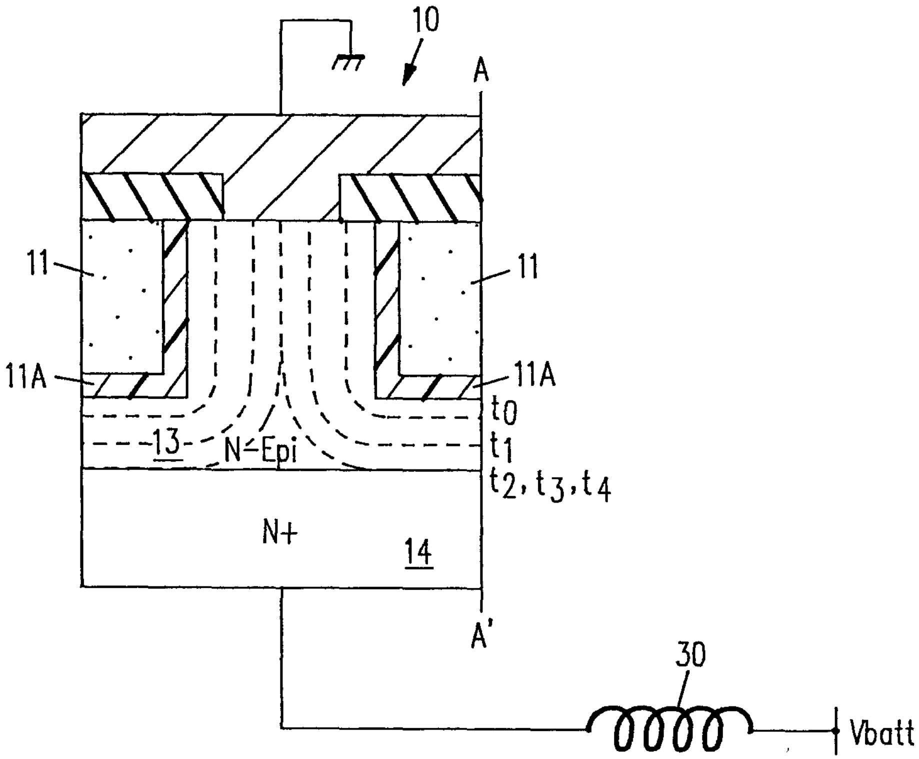

10
A
11
11
11A
11A
t0
t1
t2, t3, t4
13
N-Epi
N+
14
A'
30
Vbatt

FIG. 3A

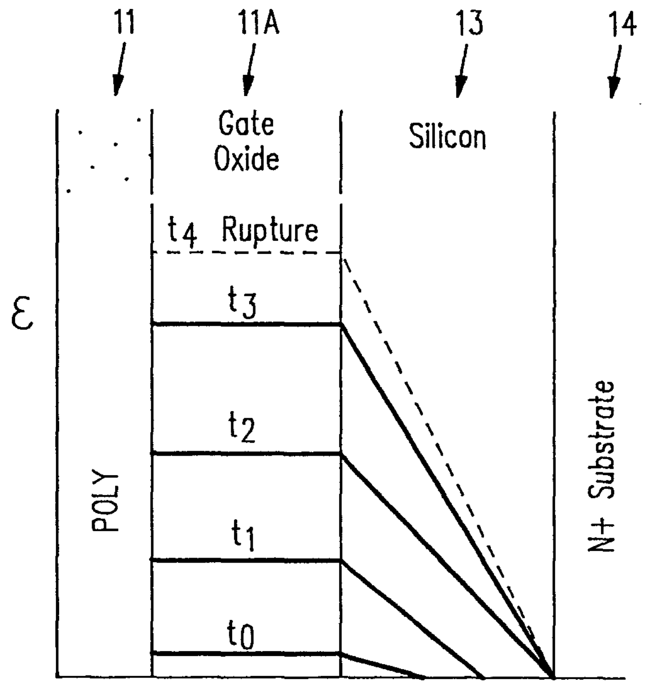

11
11A
13
14
Gate
Oxide
Silicon
t4 Rupture
t3
t2
t1
t0
ε
POLY
N+ Substrate

FIG. 3B

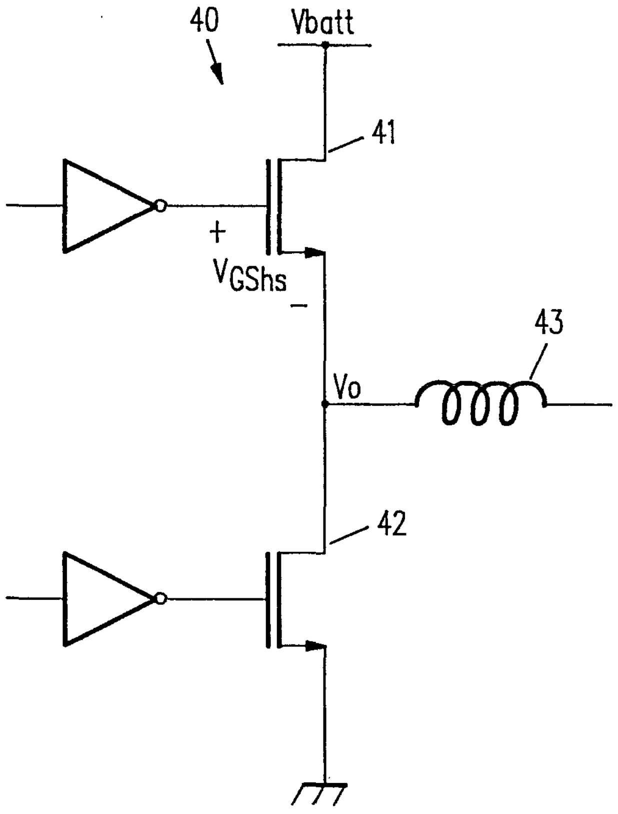

40
Vbatt
41
+
V_{GShs}
–
Vo
43
42

FIG. 4A

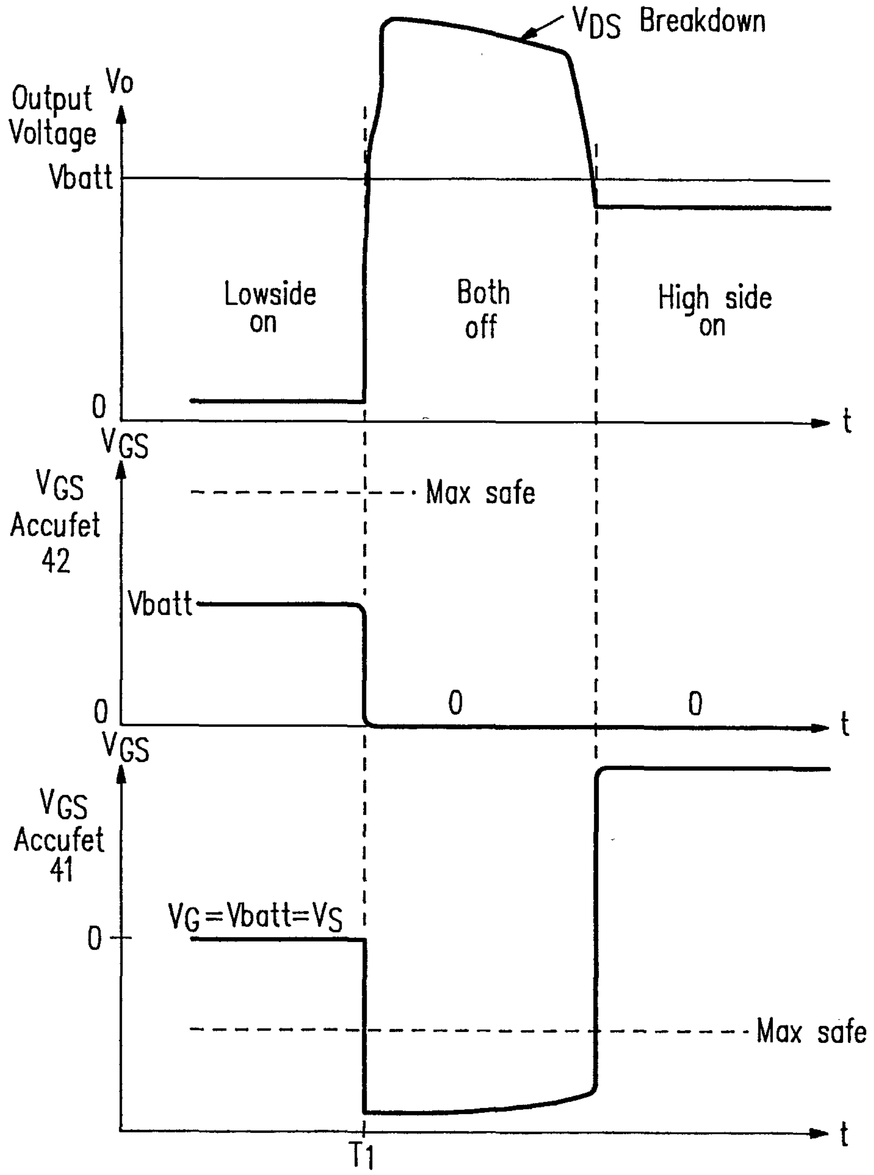

V_{DS} Breakdown
Output Voltage
Vo
Vbatt
0
Lowside on
Both off
High side on
t
V_{GS}
V_{GS} Accufet 42
Max safe
Vbatt
0
0
0
t
V_{GS}
V_{GS} Accufet 41
V_G=Vbatt=V_S
0
Max safe
t
T1

FIG. 4B

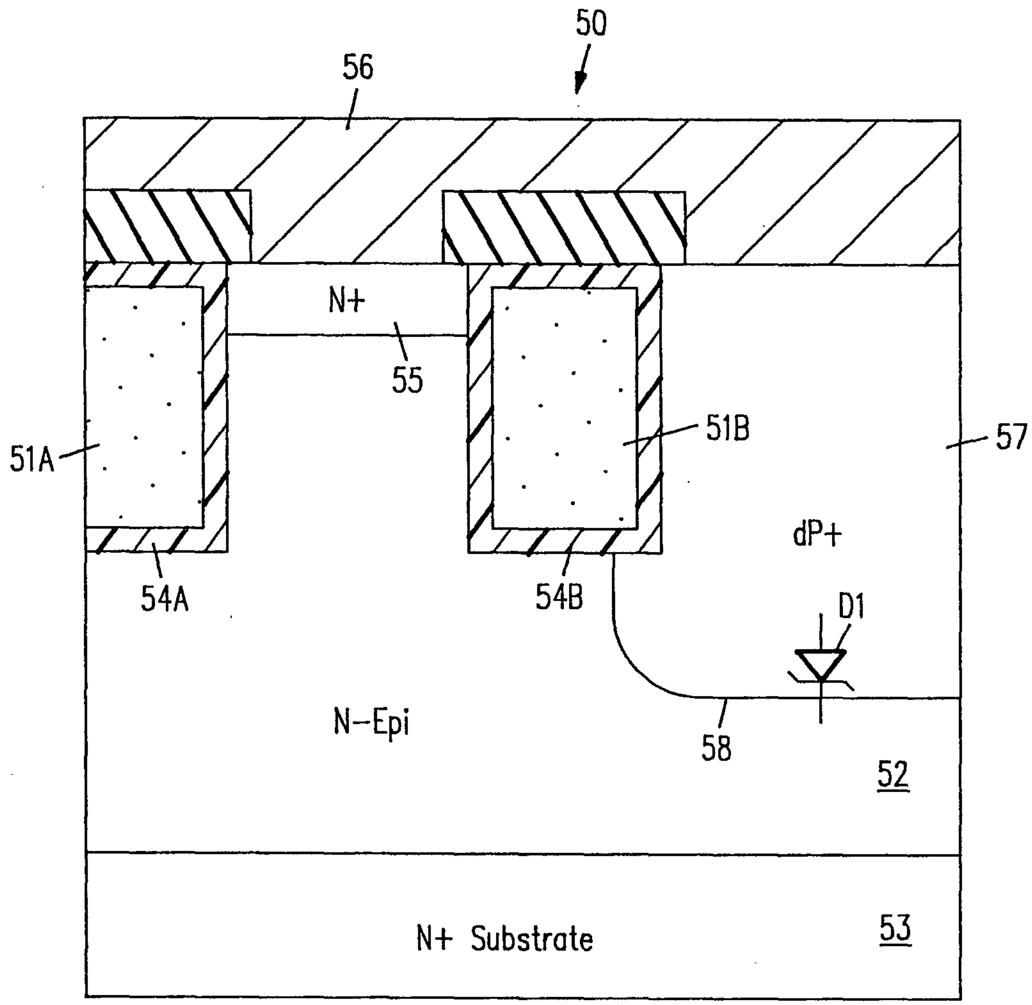


FIG. 5A

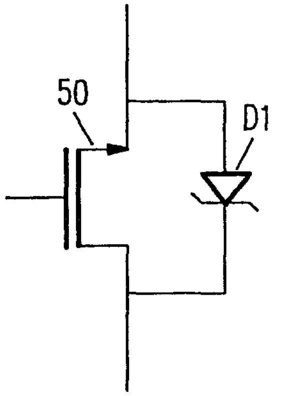


FIG. 5B

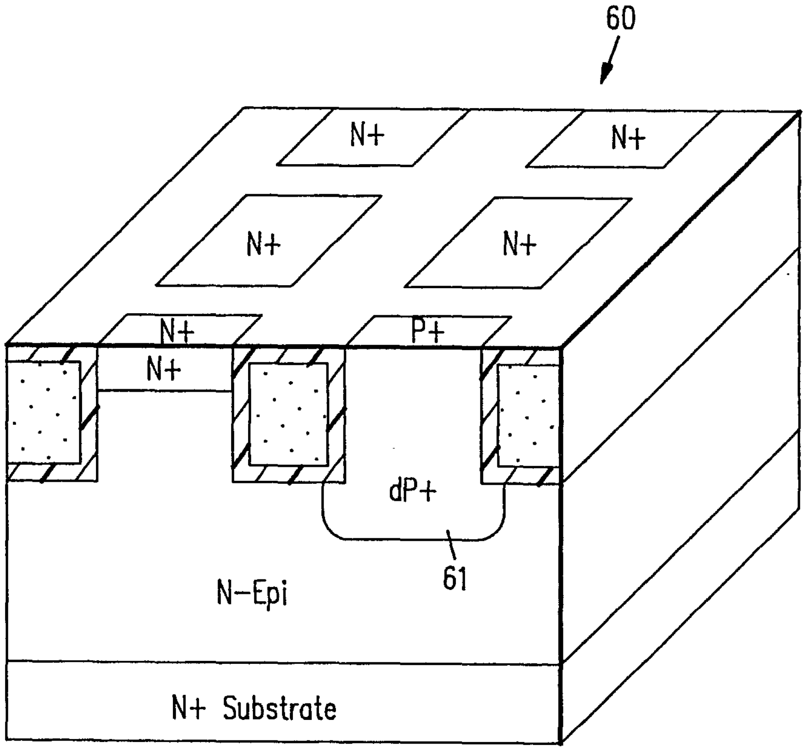

60
N+
N+
N+
N+
N+
P+
N+
dP+
61
N-Epi
N+ Substrate

FIG. 6A

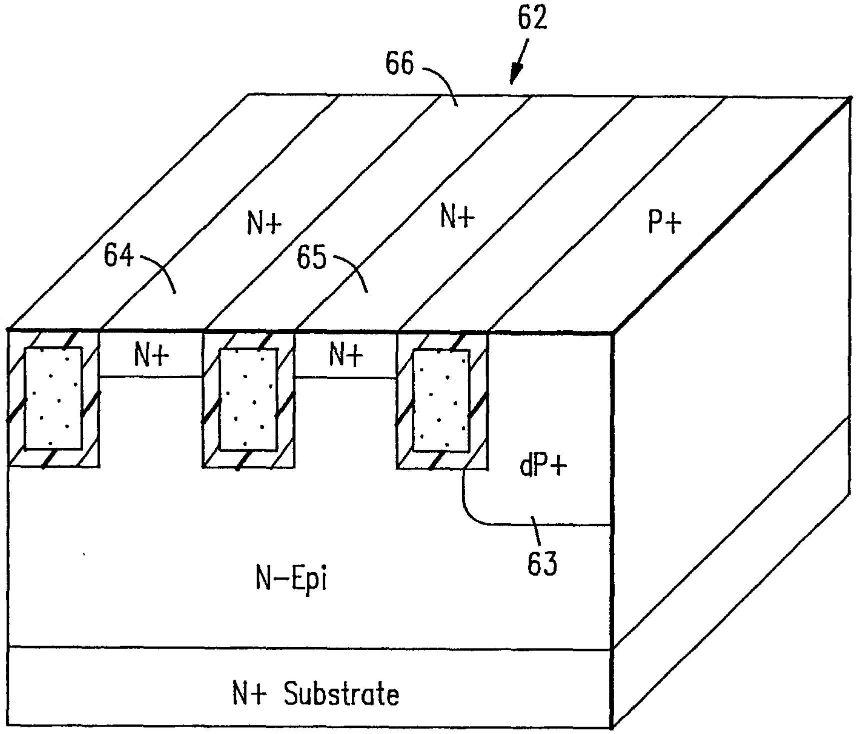

62
66
N+
N+
P+
64
65
N+
N+
dP+
63
N-Epi
N+ Substrate

FIG. 6B

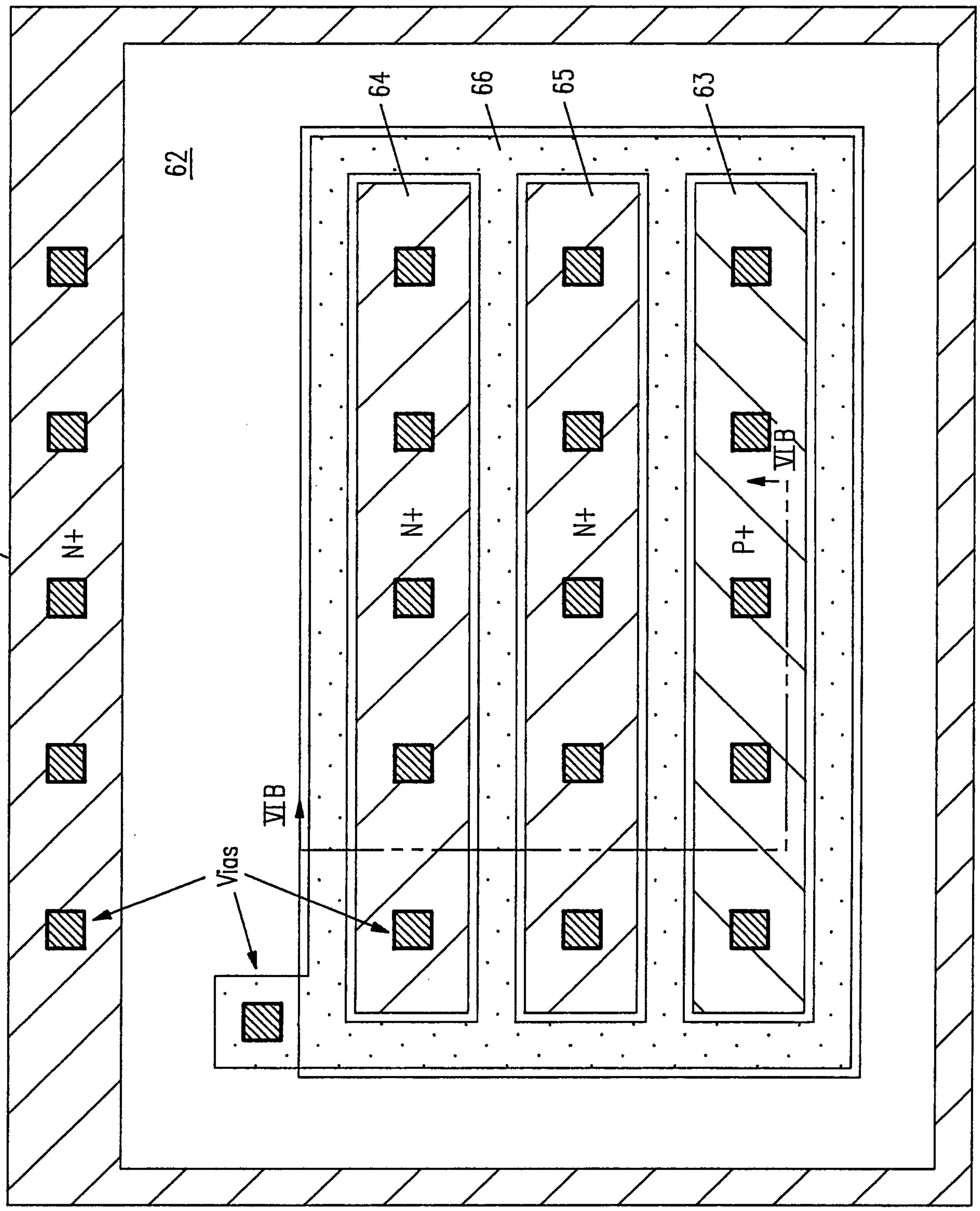


FIG. 7

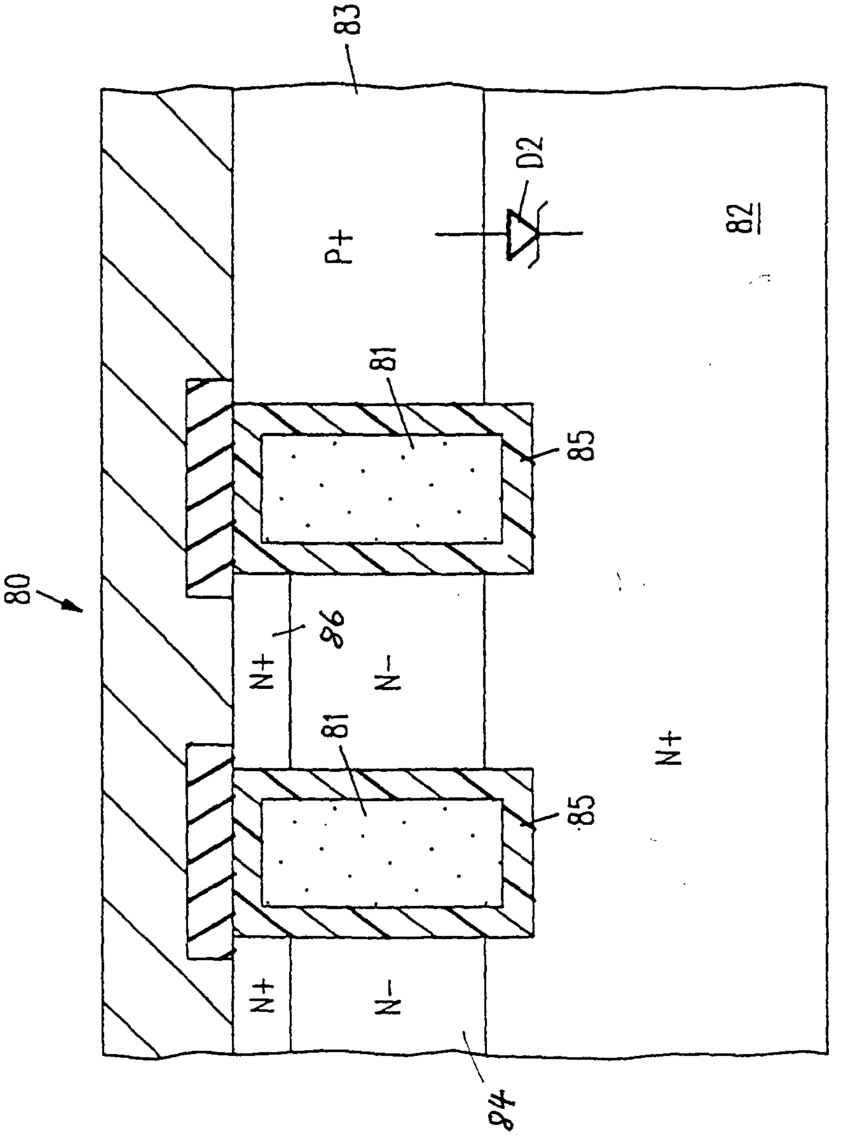


FIG. 8

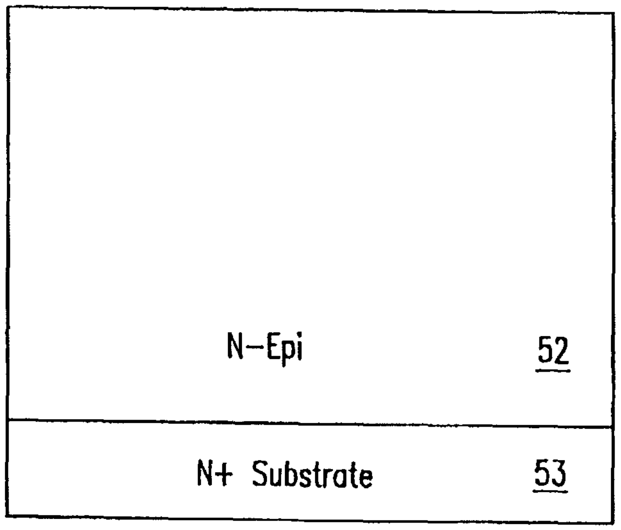


FIG. 9A

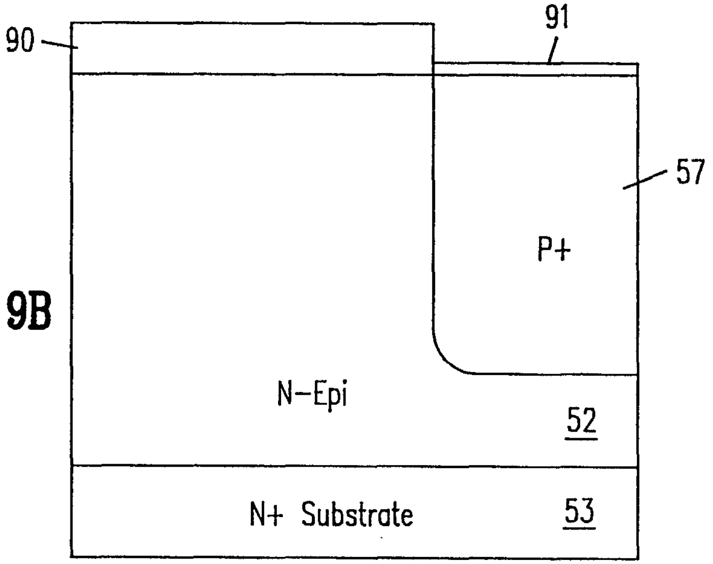


FIG. 9B

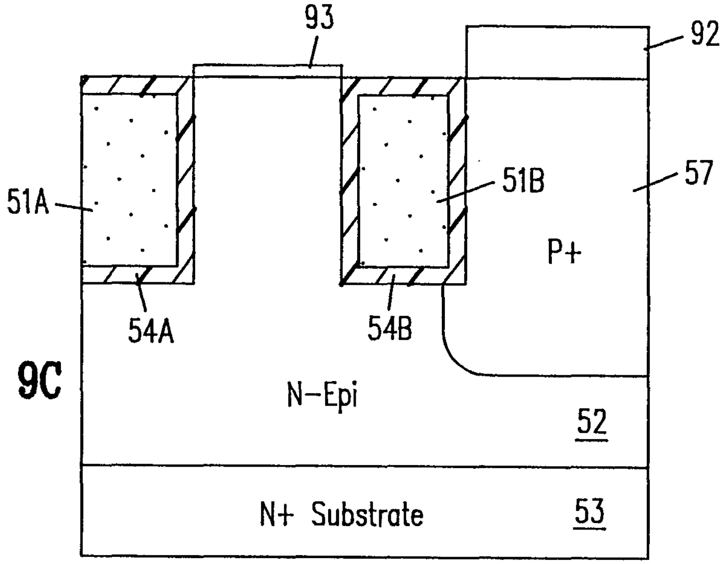


FIG. 9C

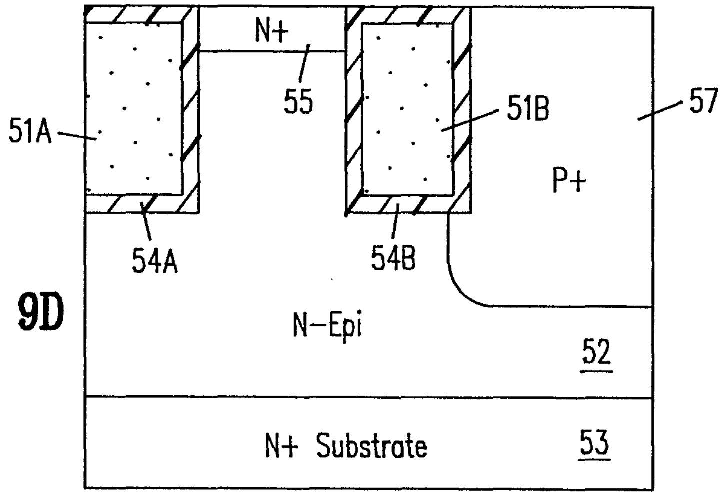


FIG. 9D

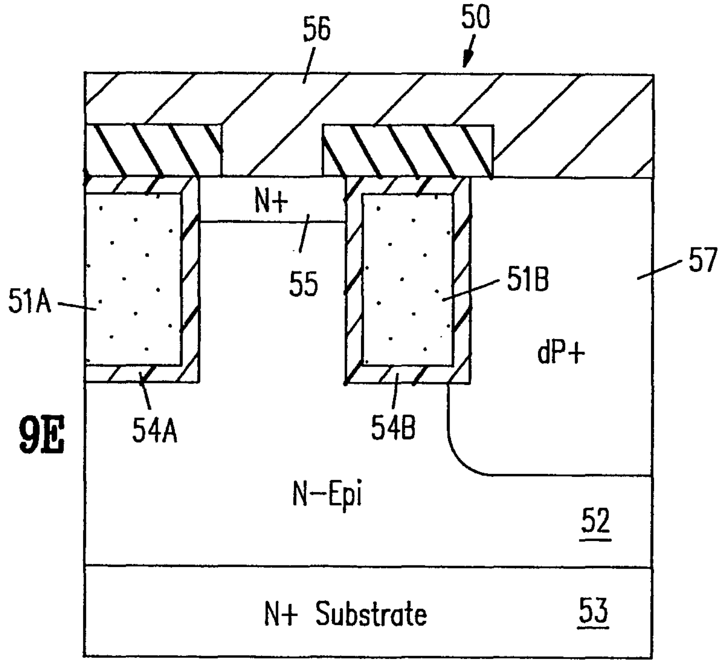


FIG. 9E