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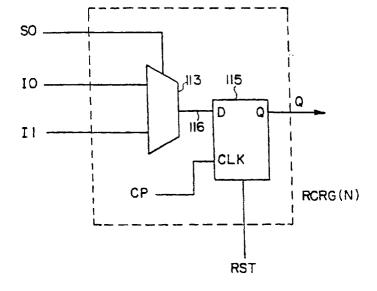
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(54) High-speed synchronous counter circuitry

(57) Digital counter register stages RCRG(N) are constructed as two-to-one mux registers, each employing a multiplexer stage (113) having first, second, and third inputs (S0, I0, I1) and an output (116) connected to the switching signal input (D) of a D-type flip-flop (15), whose Q output comprises a first input (I1) to the multi-

plexer stage (113). An inverter buffer (19) is associated with each register stage (RCRG(N)) and has an input connected to the output (Q) of said D-type flip-flop (115) and an output connected to the second input (I0) of the multiplexer stage (RCRG(N)) and fed forward to a NOR gate (21) associated with each subsequent register stage (RCRG(N)).

FIG. 2



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EUROPEAN SEARCH REPORT

Application Number EP 96 30 3243

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ategory	Citation of document with in of relevant passa	dication, where appropriate, ges	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.CI.6)	
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	The present search report has	been drawn up for all claims			
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MUNICH		6 November 1997	Bro	Brown, J	
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A technological background O : non-written disclosure		E : earlier patent do after the filing da her D : document cited L : document cited	T: theory or principle underlying the invention E: earlier patent document, but published on, or after the filling date D: document ofted in the application L: document cited for other reasons 8: member of the same patent family, corresponding		