

(19)



Europäisches Patentamt
European Patent Office
Office européen des brevets



(11)

EP 0 751 682 B1

(12)

EUROPEAN PATENT SPECIFICATION

(45) Date of publication and mention
of the grant of the patent:
13.08.2003 Bulletin 2003/33

(51) Int Cl.7: **H04N 5/44**, H04N 9/64

(21) Application number: **96304736.0**

(22) Date of filing: **27.06.1996**

(54) **Flicker reduction apparatus**

Vorrichtung zur Flimmerreduzierung

Dispositif de réduction de scintillement

(84) Designated Contracting States:
DE FR GB

(30) Priority: **30.06.1995 JP 16609395**
08.01.1996 JP 78596

(43) Date of publication of application:
02.01.1997 Bulletin 1997/01

(60) Divisional application:
03002299.0 / 1 307 056

(73) Proprietor: **MITSUBISHI DENKI KABUSHIKI**
KAISHA
Tokyo 100 (JP)

(72) Inventors:
• **Inoue, Sadayuki, c/o Mitsubishi Denki K.K.**
Tokyo 100 (JP)
• **Maeda, Naotoshi, c/o Mitsubishi Denki K.K.**
Tokyo 100 (JP)

• **Sukeno, Junji, c/o Mitsubishi Denki K.K.**
Tokyo 100 (JP)
• **Onishi, Hiroshi, c/o Mitsubishi Denki K.K.**
Tokyo 100 (JP)

(74) Representative: **Burke, Steven David et al**
R.G.C. Jenkins & Co.
26 Caxton Street
London SW1H 0RJ (GB)

(56) References cited:
EP-A- 0 651 568 WO-A-94/11854
GB-A- 2 181 323 US-A- 4 602 273
US-A- 4 639 763 US-A- 4 924 315
US-A- 5 012 326 US-A- 5 182 643

• **PATENT ABSTRACTS OF JAPAN vol. 095, no.**
004, 31 May 1995 & JP 07 030867 A (HITACHI
LTD), 31 January 1995

Note: Within nine months from the publication of the mention of the grant of the European patent, any person may give notice to the European Patent Office of opposition to the European patent granted. Notice of opposition shall be filed in a written reasoned statement. It shall not be deemed to have been filed until the opposition fee has been paid. (Art. 99(1) European Patent Convention).

EP 0 751 682 B1

Description

BACKGROUND OF THE INVENTION

[0001] The present invention relates to a scan conversion apparatus for converting a progressively scanned video signal to an interlaced video signal and to a flicker reduction apparatus for removing a flicker component contained in an input video signal.

[0002] Progressive scanning is employed in computer monitors, while interlaced scanning is employed in television sets, so the above type of scan conversion is needed when an image output from a computer is displayed on a television screen. This is expected to become a common situation, for the following reason.

[0003] The market for personal computers is expanding rapidly worldwide, but most personal computers have been purchased, either by firms or by individuals, as business tools. Recently, many manufacturers have been making personal computers easier to use by combining the computer and its keyboard, pointing device, monitor display, disk drives, and other components into a single unit, so that the user does not have to interconnect these components himself, and by adding pre-installed software. These personal computers are not intended for family use, however, but for use by a single individual, who sits facing a comparatively small display screen and manipulates the keyboard and pointing device by himself. The need for inexpensive, easy-to-operate computers for family use remains unanswered.

[0004] When computers are developed for family use, they will require a large display that can be watched by the whole family at once, with audio that can be heard by the whole family at once. That is, the display will have to be similar to a television display. The computer will also have to be operable like a television set or other home audio-visual appliance, by means of a wireless remote-control device, for example.

[0005] Providing an inexpensive display for such a computer presents a problem, because for a given size, a computer monitor is about four times as costly as a television display. The most readily available solution to this problem is to connect the computer to a television set through a device that converts the computer's progressive scanning to the interlaced scanning used by the television set. Thus as the personal computer evolves into a computer for family use, it can be anticipated that computer output will frequently be displayed on television screens, necessarily with scan conversion.

[0006] There is no single computer-display standard, but the video graphics array (VGA) standard is widely used and can be taken as a typical example. The VGA standard specifies progressive scanning with six hundred forty effective picture elements or pixels per horizontal scanning line, and four hundred eighty effective horizontal scanning lines per frame. The scanning rate is not standardized but is usually about sixty frames per second or sixty hertz (60 Hz).

[0007] There is also no single television standard, but recommendation BT.601 (system 525) of the Radiocommunication Sector of the International Telecommunications Union (ITU-R) can be taken as typical. This standard specifies seven hundred twenty effective pixels per horizontal scanning line at a sampling rate of 13.5 megahertz (13.5 MHz), with four hundred eighty-six effective scanning lines per frame. In television broadcasts each frame is divided into two interlaced fields, containing the even-numbered and odd-numbered scanning lines, respectively, and the scanning rate is about sixty fields per second. In the standard set by the National Television System Committee (NTSC), the scanning rate is 59.94 fields per second (59.94 Hz).

[0008] One reason for a frame rate in progressive scanning and a field rate in interlaced scanning of about sixty hertz is that this is the rate at which flicker ceases to be annoying in the range of brightness levels normally displayed on a computer monitor or television screen.

[0009] Since the computer's progressively-scanned frame rate is substantially equal to the interlaced field rate of the television set, scan conversion can be carried out basically by decimation: by deleting even-numbered scanning lines from one frame, odd-numbered scanning lines from the next frame, and so on in alternation. This leads to a severe flicker problem, however, because computer-generated images tend to contain many sharp edges and other fine detail. After scan conversion, detail with a vertical extent of only one scanning line will appear only in every other field, flickering at a rate of about thirty hertz. If the detail is bright, this flicker will be highly visible and irritating. Any sharp vertical brightness transition produces similar flicker.

[0010] A known method of reducing the flicker caused by the scan conversion of a computer-generated image is to use a low-pass spatial filter to reject the highest vertical spatial frequencies. For example, a filter that replaces each horizontal scanning line with the weighted average of that scanning line itself (given a weight of 1/2) and the adjacent scanning lines above and below (each given a weight of 1/4) can effectively eliminate flicker.

[0011] A problem is that while eliminating flicker, this filter also reduces the vertical resolution of the image, so that vertical details become blurred. In particular, computer-generated text often becomes difficult to read. There are known methods of improving vertical resolution by reducing the degree of filtering in areas where little vertical high-frequency energy is present, or where image motion is present, but these methods fail to improve the readability of text, which has considerable vertical high frequency energy and is motionless.

[0012] Attempts have been made to compensate for the loss of vertical resolution by expanding images in which text or other important detail occurs. One known method of expanding an image copies part of the input signal to, for example, the odd field of the output signal, and constructs the even field by mean-value interpola-

tion between adjacent odd-numbered scanning lines. After scan conversion by this method, however, odd-numbered fields appear sharper than even-numbered fields, because the odd fields are obtained directly from the original image while the even fields are obtained by averaging. Thus the entire screen appears to flicker.

[0013] Another known expansion method copies the original image to both the even and odd fields of the output image, so that the even and odd fields are identical. Both fields then appear equally sharp, but severe flicker occurs at horizontal edges in the output image.

[0014] US Patent 5,012,326 is concerned with motion-adaptive scan conversion processes which convert a progressively scanned signal to an interlaced signal for transmission over standard transmission equipment and which, after reception, reconvert to progressively scanned signals for display. In particular, US 5,012,326 is concerned with motion-adaptive scan conversion processes which use intrafield interpolation to convert moving pictures and interfield interpolation to convert still pictures. One described problem with this motion-adaptive approach is that clocking errors between a transmitter (at which conversion to interlaced scanning occurs) and a receiver (at which reversion to progressive scanning occurs) may result in rapid switching between interfield and intrafield interpolation resulting in "flutter". Another described problem is that suddenly moving images result in sudden blurring of the picture. US 5,012,326 describes separating a horizontal high frequency component of the signal at the transmitter end and forcing the motion-adaptive process to use interfield interpolation for scan conversion of this component. Thus, the problems of fluttering and blurring are ameliorated.

SUMMARY OF THE INVENTION

[0015] It would accordingly be desirable to reduce flicker without unnecessary loss of vertical resolution, when a video signal is converted from progressive scanning to interlaced scanning.

[0016] It would also be desirable to improve the legibility of text in a video signal that has been converted from progressive scanning to interlaced scanning.

[0017] It would be further desirable to avoid flicker when an image is expanded in the process of conversion from progressive scanning to interlaced scanning.

[0018] Aspects of the present invention are set out in the accompanying claims.

[0019] The invention may be embodied as a scan conversion apparatus which has a deflickering circuit that attenuates spatial frequency components having high vertical spatial frequency and simultaneously having low horizontal spatial frequency, thereby producing a filtered video signal. Selected horizontal scanning lines of the filtered video signal are stored in a frame memory, which has separate areas for storing even and odd horizontal scanning lines, thereby converting the filtered

video signal from progressive scanning to interlaced scanning.

[0020] The deflickering circuit may also be adapted to expand part of the input video signal by vertical interpolation, followed by vertical low-pass filtering. In this case a separate horizontal interpolating circuit expands the selected parts horizontally by performing horizontal interpolation.

[0021] In the case of a color video signal, the deflickering circuit preferably operates only on the luminance component.

[0022] There now follows a detailed description of embodiments of the present invention referred to as the second, fifth, sixth and eighth embodiments. To assist in understanding the embodiments of the present invention, further description is provided below and referred to as first, third, fourth and seventh embodiments. However, these are not embodiments of the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0023] In the accompanying drawings:-

FIG. 1 illustrates vertical and temporal frequency characteristics of a progressively scanned video signal;

FIG. 2 illustrates vertical and temporal frequency characteristics of an interlaced video signal;

FIG. 3 illustrates vertical and horizontal frequency characteristics of a video signal;

FIG. 4 is a block diagram illustrating the first seven embodiments of the invention;

FIG. 5 is a block diagram of the deflickering circuit in the first embodiment of the invention;

FIG. 6 is a block diagram of the vertical low-pass filter in FIG. 5;

FIG. 7 is a block diagram of the horizontal high-pass filter in FIG. 5;

FIG. 8 is a spatial frequency diagram illustrating the operation of the first embodiment;

FIG. 9 is a block diagram of the deflickering circuit in the second embodiment;

FIG. 10 illustrates the limiting characteristic of the amplitude limiter in FIG. 9;

FIG. 11 illustrates a variation of the limiting characteristic of the amplitude limiter in FIG. 9;

FIG. 12 is a block diagram of the deflickering circuit in the third embodiment;

FIG. 13 is a block diagram of the second vertical low-pass filter in FIG. 12;

FIG. 14 illustrates the frequency characteristic of the first vertical low-pass filter in FIG. 12;

FIG. 15 illustrates the frequency characteristic of the second vertical low-pass filter in FIG. 12;

FIG. 16 is a spatial frequency diagram illustrating the operation of the third embodiment;

FIG. 17 is a block diagram of the deflickering circuit

in the fourth embodiment;

FIG. 18 is a block diagram of the direct-current detector in FIG. 17;

FIG. 19 illustrates the limiting characteristics of the amplitude limiter in FIG. 17;

FIG. 20 is a block diagram of the deflickering circuit in the fifth embodiment;

FIG. 21 illustrates the operating characteristic of the amplitude converter in FIG. 20;

FIG. 22 is a block diagram of the deflickering circuit in the sixth embodiment;

FIG. 23 is a block diagram of the horizontal low-pass filter in FIG. 22;

FIG. 24 illustrates a first limiting characteristic of the amplitude limiter in FIG. 22;

FIG. 25 illustrates a second limiting characteristic of the amplitude limiter in FIG. 22;

FIG. 26 illustrates the operation of the sixth embodiment in an image that is substantially constant in the horizontal direction but has a step transition in the vertical direction;

FIG. 27 illustrates the operation of the sixth embodiment in an image that is not substantially constant in the horizontal direction, and has a step transition in the vertical direction;

FIG. 28 is a block diagram of the deflickering circuit in the seventh embodiment;

FIG. 29 is a block diagram of the eighth embodiment;

FIG. 30 is a block diagram of the deflickering circuit in the eighth embodiment;

FIG. 31 is a block diagram of the vertical low-pass filter in FIG. 30;

FIG. 32 is a block diagram of the horizontal interpolating circuits in the eighth embodiment;

FIG. 33 is a flowchart illustrating the expansion and flicker-suppression operation of the eighth embodiment;

FIG. 34 is a diagram further illustrating the expansion and flicker-suppression operation of the eighth embodiment;

FIG. 35 is a block diagram of a field-frame conversion circuit; and

FIG. 36 is a block diagram of another field-frame conversion circuit.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0024] Embodiments of the invention will be described with reference to the attached illustrative drawings. These embodiments will be described as converting a VGA video signal output by a computer to a video signal conforming to the standard set by the National Television System Committee (NTSC) for display by a television set, except that the luminance and chrominance components of the NTSC signal will be left separate.

[0025] Before the embodiments are described, it will be useful to give a more technical description of the way in which flicker arises.

[0026] The frequency characteristics of a video signal can be described by a three-dimensional Fourier transform performed in relation to two spatial axes and one temporal axis. FIG. 1 illustrates the vertical and temporal frequency characteristics of a progressively scanned video signal having a frame rate of 60 Hz and a resolution of 525 horizontal scanning lines per frame, including scanning lines in the vertical blanking interval, which are not displayed. The vertical axis indicates vertical spatial frequency (ν), which can be measured in cycles per height of the screen (cpH). The horizontal axis indicates temporal frequency, measured in hertz. The frequency components of a progressively scanned video signal appear repeatedly around multiples of 60 Hz in the temporal direction and multiples of 525 cpH in the vertical direction, in regions such as region 2.

[0027] The negative frequency values in FIG. 1 have essentially the same meaning as the positive frequency values. The frequency components corresponding to vertical fine detail are disposed at both the top and bottom of region 2 and the other regions.

[0028] FIG. 2 illustrates the frequency characteristics of the signal in FIG. 1 after conversion from progressive to interlaced scanning. The horizontal and vertical axes have the same meaning as in FIG. 1. In addition to the frequency components 2 that were present in FIG. 1, new frequency components 3 are present, located around odd multiples of 30 Hz and 525/2 cpH. The vertical spatial frequencies that give rise to flicker occur in the hatched regions, e.g. where the highest positive vertical spatial frequencies 4 in region 2 coincide with negative vertical spatial frequencies 5 in region 3, or where the highest negative spatial frequencies 6 in region 2 coincide with positive spatial frequencies 7 in region 8.

[0029] FIG. 3 shows region 2 in FIG. 2 viewed in the spatial frequency plane. The vertical axis indicates vertical spatial frequency (ν) as in FIG. 2. The horizontal axis now indicates horizontal spatial frequency (μ), which is conventionally measured in megahertz. Hatching is again used to indicate the frequency components that give rise to flicker. If the frequency components in areas 4 and 6 are eliminated, the flicker disappears, but vertical resolution suffers, as noted earlier.

[0030] The embodiments of the present invention will filter out, limit, or attenuate some but not all of the frequency components in regions 4 and 6, thereby reducing flicker to an unobtrusive level while maintaining adequate vertical spatial resolution. The degree of filtering, limiting, or attenuation will be responsive to horizontal spatial frequency characteristics of the video signal.

First embodiment

[0031] FIG. 4 shows the general structure of the first embodiment. The VGA signal comprises separate red,

green, and blue component signals (R, G, and B) which are received at input terminals 9, 10, and 12, and a synchronizing signal (VGA SYNC) that is received at an input terminal 14. The television set also provides a synchronizing signal (TV SYNC) to an input terminal 16.

[0032] The red, green, and blue component signals are supplied to a matrix circuit 18, which converts them to analog luminance and chrominance signals, more specifically to an analog luminance signal Y and two analog color difference signals R - Y and B - Y. The color difference signals are filtered by a pair of low-pass filters 20 and 22. The luminance signal Y and the filtered color difference signals R - Y and B - Y are then converted to digital signals by three analog-to-digital (A/D) converters 24, 26, and 28.

[0033] The digitized luminance signal (denoted Yin) is fed through a novel deflickering circuit 30, and the resulting filtered luminance signal (denoted Yout) is stored in a first frame memory 32. The digitized color difference signals R - Y and B - Y are stored in a pair of chrominance frame memories 34 and 36. At appropriate times, these signals are read out of the frame memories 32, 34, and 36 and converted to analog signals by three digital-to-analog (D/A) converters 38, 40, and 42. The resulting analog luminance signal Y is fed through a synchronizing signal adding circuit 44, which adds synchronizing pulses, to an output terminal 46. The analog color difference signals R - Y and B - Y are supplied to a chroma encoder 48, which combines them into a chrominance signal C that is delivered to an output terminal 50.

[0034] The VGA synchronizing signal is detected by a first synchronization detector 52, which furnishes horizontal and vertical synchronizing pulses to a first phase-locked loop (PLL) circuit 54 and a memory control circuit 56. The first PLL circuit 54 provides clock signals to the A/D converters 24, 26, and 28, the deflickering circuit 30, and the memory control circuit 56.

[0035] The TV synchronizing signal is detected by a second synchronization detector 58, which furnishes horizontal and vertical synchronizing pulses to the synchronizing signal adding circuit 44, the chroma encoder 48, a second PLL circuit 60, and the memory control circuit 56. The second PLL circuit 60 provides clock signals to the D/A converters 38, 40, and 42 and the memory control circuit 56.

[0036] FIG. 5 shows the structure of the novel deflickering circuit 30 in FIG. 4. This deflickering circuit 30 receives the digitized luminance signal Yin from A/D converter 24 at an input terminal 62, receives memory control signals from the memory control circuit 56 at an input terminal 64, and supplies a filtered luminance signal Yout to an output terminal 66, which is coupled to the first frame memory 32. The two input terminals 62 and 64 are coupled to a first vertical low-pass filter (VLPF) 68 and a line memory 70. The outputs of the first vertical low-pass filter 68 and line memory 70 are supplied to a subtractor 72, which furnishes their difference to a horizontal high-pass filter (HHPF) 74. The output of the first

vertical low-pass filter 68 is stored temporarily in a register 76. An adder 78 adds the register contents to the output of the horizontal high-pass filter 74 and supplies the sum to the output terminal 66.

[0037] The symbol V_L in FIG. 5 indicates the vertical low-frequency luminance signal V_L (containing luminance components with low vertical spatial frequencies) output by the first vertical low-pass filter 68. V_H indicates the vertical high-frequency luminance signal (containing luminance components with high vertical spatial frequencies) obtained by subtracting V_L from Yin. Y_{HH} indicates the horizontal-high-frequency-vertical-high-frequency signal obtained by horizontal high-pass filtering of V_H .

[0038] In the following description it will be assumed that all of these signals are eight-bit signals. The possible values of Yin and V_L are from zero and two hundred fifty-five (0 to 255). The possible values of V_H and Y_{HH} are from minus one hundred twenty-seven to plus one hundred twenty-eight (-127 to 128).

[0039] FIG. 6 shows the structure of the first vertical low-pass filter 68 in FIG. 5. This filter has three taps, with coefficients of 1/4, 1/2, and 1/4. More specifically, the luminance signal Yin received at input terminal 62 is stored in a first line memory 80, then passed from the first line memory 80 to a second line memory 82. These line memories 80 and 82 are controlled by the memory control signals received at input terminal 64. The input to line memory 80, the output from line memory 80, and the output from line memory 82 are furnished to respective multipliers 84, 86, and 88, and multiplied by respective weighting coefficients (tap coefficients) of 1/4, 1/2, and 1/4. The outputs of multipliers 84, 86, and 88 are added by an adder 90 and provided as the vertical low-frequency luminance signal V_L to an output terminal 92.

[0040] FIG. 7 shows the structure of the horizontal high-pass filter 74 in FIG. 5. The vertical high-frequency signal V_H is received at an input terminal 94, stored in a first register 96, then passed to a second register 98. The input to register 96, the output from register 96, and the output from register 98 are furnished to respective multipliers 100, 102, and 104, and multiplied by respective weighting coefficients of -1/4, 1/2, and -1/4. The outputs of multipliers 100, 102, and 104 are added by an adder 106 and provided as the horizontal-high-frequency-vertical-high-frequency signal Y_{HH} to an output terminal 108.

[0041] As FIGs. 5, 6, and 7 indicate, the hardware requirements of the deflickering circuit 30 are modest, consisting in all of three registers, three line memories, three adders, six multipliers, and a subtractor. The multipliers are particularly simple. Since the multipliers multiply by fixed coefficients of 1/2, 1/4, or -1/4, they need only perform a one- or two-bit right shift operation, or a two-bit right shift and a two's complement operation. The right shift operations can be carried out simply by means of appropriate signal line interconnections.

[0042] FIG. 8 shows the two-dimensional spatial fre-

quency plane again and illustrates the basic operating concept of the deflickering circuit 30. The horizontal and vertical axes have the same meaning as in FIG. 3.

[0043] Generally speaking, flicker occurring over a large area is much more noticeable than flicker occurring in a small area. When a large area flickers, not only is the flicker obvious, but the human eye extends the perception of flicker into adjacent areas, so that those areas appear to flicker too. Thus if the horizontal dividing lines or top and bottom boundary lines in a table or chart flicker, the flicker is extremely irritating; the entire table or chart appears to vibrate. If only the very short horizontal lines occurring in the letters of text in the table or chart flicker, however, the flicker will be barely perceptible and will not cause irritation.

[0044] The first embodiment accordingly separates vertical spatial frequency components that cause obvious flicker from components that cause less perceptible flicker, and removes only components that cause obvious flicker. More precisely, first all flicker-causing components are removed, then those components that cause less perceptible flicker are added back in. The vertical resolution in areas of small-scale detail, such as areas of text, is thereby restored sufficiently for the detail to be seen, e.g. for the text to be read.

[0045] In FIG. 8, first the high vertical spatial frequencies in regions 112, 114, 116, 118, 120, and 122 are removed from the luminance signal. Then the components in regions 112, 116, 118, and 122, representing high-vertical-high-horizontal spatial frequencies, are added back in. Thus only the components in regions 114 and 120, which combine high vertical spatial frequency with low horizontal spatial frequency, are removed.

[0046] Next the operation of the first embodiment will be described with reference to FIGs. 4 to 7. Details of the internal operation of the matrix circuit 18 and other well-known circuits will be omitted.

[0047] Referring to FIG. 4, after the red, green, and blue component signals received at input terminals 9, 10, and 12 have been converted by the matrix circuit 18 to a luminance signal Y and color difference signals R - Y and B - Y, the low-pass filters 20 and 22 limit the bandwidth of the color difference signals R - Y and B - Y to half the bandwidth output by the matrix circuit 18. This band limitation has little effect on final picture quality, because the human eye is less sensitive to chrominance detail than to luminance detail. Because of this band limitation, the sampling clock signal supplied from the first PLL circuit 54 to A/D converters 26 and 28 has half the rate of the sampling clock signal supplied to A/D converter 24. The data rate of each of the digitized color difference signals R - Y and B - Y is therefore half the data rate of the digitized luminance signal Yin.

[0048] The first PLL circuit 54 generates these sampling clock signals from the horizontal synchronizing pulses detected by the first synchronization detector 52. The sampling clock supplied to A/D converters 26 and 28 is obtained by dividing the frequency of the sampling

clock supplied to A/D converter 24. Both sampling clocks are supplied to the memory control circuit 56. The sampling clock supplied to A/D converter 24, referred to below as the VGA dot clock, is also supplied to the deflickering circuit 30. In addition, the first synchronization detector 52 supplies both horizontal and vertical synchronizing signals to the memory control circuit 56.

[0049] The memory control circuit 56 uses the VGA horizontal synchronizing signal supplied from the first synchronization detector 52 to generate read and write control signals for the line memories 70, 80, and 82 in the deflickering circuit 30 and its first vertical low-pass filter 68. These line memories are, for example, first-in-first-out (FIFO) memory circuits to which the memory control circuit 56 supplies line address reset signals for read access and write access, read and write enable signals, and read and write clock signals. The memory control circuit 56 also uses both the VGA horizontal and vertical synchronizing signals supplied from the first synchronization detector 52 to generate read and write control signals for the frame memories 32, 34, and 36, as will be described later.

[0050] Referring to FIG. 5, the digitized luminance signal Yin output from A/D converter 24 is received at input terminal 62 of the deflickering circuit 30, fed to the first vertical low-pass filter 68 and line memory 70, and processed as follows.

[0051] Referring to FIG. 6, the luminance signal Yin is supplied to the first line memory 80 and multiplier 84 in the first vertical low-pass filter 68. The first line memory 80 outputs the luminance signal Yin with a delay of one horizontal scanning line to the second line memory 82 and multiplier 86. The second line memory 82 outputs the luminance signal Yin with a delay of one more horizontal scanning line to multiplier 88. Line memories 80 and 82 receive the above-mentioned read and write control signals from the memory control circuit 56 at input terminal 64.

[0052] When a luminance pixel is output from the first line memory 80 and multiplied by 1/2 in multiplier 86, the luminance pixels directly above and below are simultaneously multiplied by 1/4 in multipliers 84 and 88. By taking the sum of these three products, adder 90 rejects the flicker-causing high vertical spatial frequencies, leaving the vertical low-frequency luminance signal V_L with only lower vertical spatial frequencies. V_L can be considered to be delayed by one horizontal scanning line with respect to Yin.

[0053] When a pixel value is output from the first line memory 80, multiplied by 1/2 in multiplier 86, and added by adder 90, the read and write control signals received from the memory control circuit 56 at input terminal 64 cause the line memory 70 in FIG. 5 to output the same pixel value. Subtractor 72 therefore subtracts the low-pass filtered value of each pixel from the unfiltered value of the same pixel. In this way all the low vertical spatial frequencies that were left by the first vertical low-pass filter 68 are removed by subtractor 72, leaving only high

vertical spatial frequencies in the output V_H of subtractor 72.

[0054] Referring to FIG. 7, this vertical high-frequency signal V_H is received by the horizontal high-pass filter 74 at input terminal 94 and supplied to the first register 96 and multiplier 100 in the horizontal high-pass filter 74. The first register 96 outputs V_H with a delay of one pixel to the second register 98 and multiplier 102. The second register 98 outputs V_H with a delay of one more pixel to multiplier 104. Registers 96 and 98 are controlled by the VGA dot clock output by the first PLL circuit 54, although this is not explicitly indicated in the drawing.

[0055] When a V_H pixel value is output from the first register 96 and multiplied by $1/2$ in multiplier 102, the values of the adjacent pixels to the right and left are simultaneously multiplied by $-1/4$ in multipliers 100 and 104. By taking the sum of these three products, adder 106 rejects low horizontal spatial frequencies. Since the input V_H to the horizontal high-pass filter 74 contained only high vertical spatial frequencies, the output Y_{HH} of the horizontal high-pass filter 74 contains only components which are high in both horizontal and vertical spatial frequency simultaneously (regions 112, 116, 118, and 122 in FIG. 8). Y_{HH} can be considered to be delayed by one pixel with respect to V_H and V_L .

[0056] Referring again to FIG. 5, register 76 delays V_L by one pixel, so that adder 78 adds each pixel in V_L to the corresponding Y_{HH} pixel. The filtered luminance signal Y_{out} output by adder 78 is delayed by one scanning line plus one pixel, and contains both the low vertical spatial frequencies present in V_L and the high vertical, high horizontal spatial frequencies present in Y_{HH} . In FIG. 8, this signal Y_{out} contains all components except those in the hatched regions 114 and 120.

[0057] Referring again to FIG. 4, the filtered luminance signal Y_{out} output by the deflickering circuit 30 and the color difference signals $R - Y$ and $B - Y$ output by A/D converters 26 and 28 are stored in the frame memories 32, 34, and 36 in accordance with write control signals received from the memory control circuit 56, as follows.

[0058] The control signals furnished from the memory control circuit 56 to the frame memories 32, 34, and 36 are adapted to convert a progressively scanned digital video signal input at a frame rate of 60 Hz to an interlaced digital video signal output at a field rate of 60 Hz. The conversion from frame structure to field structure takes place when the signal is written into the frame memories.

[0059] The memory control circuit 56 generates control signals as follows. Upon receiving a VGA vertical synchronizing signal from the first synchronization detector 52, the memory control circuit 56 decides whether the video data that follow will become an even field or an odd field. This decision can be made by having each VGA vertical synchronizing signal toggle an even/odd flag. If the decision is an odd field, the memory control circuit 56 generates control signals to write the odd-

numbered scanning lines into the frame memories 32, 34, and 36. If the decision is an even field, the memory control circuit 56 generates control signals to write the even-numbered scanning lines into the frame memories 32, 34, and 36. The memory control circuit 56 differentiates between even- and odd-numbered lines by counting the VGA horizontal synchronizing signals received from the first synchronization detector 52.

[0060] The frame memories 32, 34, and 36 therefore receive and store the digital video data in an interlaced sequence: first odd-numbered scanning lines, then even-numbered scanning lines, then odd-numbered scanning lines, and so on. Each frame memory 32, 34, and 36 has separate areas for storing two fields of digital video data, an even field and an odd field. One of the control signals output from the memory control circuit 56, which can be generated from the above-mentioned even/odd flag, switches between these two fields. The memory control circuit 56 also provides address signals and write enable signals, which are generated from the horizontal and vertical synchronizing signals received from the first synchronization detector 52 and the clock signals received from the first PLL circuit 54. Only the values of pixels in the VGA picture area are stored in the frame memories; values in the horizontal and vertical blanking intervals are not stored.

[0061] From the television synchronizing signal received at input terminal 16, the second synchronization detector 58 detects horizontal and vertical synchronizing signals, decides whether the field following each vertical synchronizing signal is an even or odd field, and generates an even/odd field decision signal. From the horizontal synchronizing signals detected by the second synchronization detector 58, the second PLL circuit 60 generates luminance and chrominance clock signals, the chrominance clock having half the frequency of the luminance clock. The luminance clock is supplied to D/A converter 38. The chrominance clock is supplied to D/A converters 40 and 42. Both clocks are supplied to the memory control circuit 56, together with the horizontal and vertical synchronizing signals and even/odd field decision signal from the second synchronization detector 58. The second synchronization detector 58 also sends the horizontal and vertical synchronizing signals and even/odd field decision signal to the synchronizing signal adding circuit 44 and chroma encoder 48.

[0062] Using the horizontal and vertical synchronizing signals and even/odd field decision signal received from the second synchronization detector 58, and the clock signals received from the second PLL circuit 60, the memory control circuit 56 generates read control signals for the frame memories 32, 34, and 36. These read control signals include address signals, read enable signals, and signals that select the even or odd field of stored video data. In response to these signals, the frame memories 32, 34, and 36 output the stored digital video data in an interlaced scanning sequence.

[0063] The D/A converters 38, 40, and 42 convert the

interlaced digital video signals output from the frame memories 32, 34, and 36 to interlaced analog video signals. To the interlaced analog luminance signal Y output by D/A converter 38, the synchronizing signal adding circuit 44 adds horizontal and vertical synchronizing pulses generated from the horizontal and vertical synchronizing signals and even/odd field decision signal received from the second synchronization detector 58. The synchronizing signal adding circuit 44 also inserts additional signal segments as necessary in the horizontal and vertical blanking intervals.

[0064] The chroma encoder 48 uses the analog color difference signals R - Y and B - Y received from D/A converters 40 and 42 to modulate a color subcarrier signal, thereby creating the output chrominance signal C. The modulation is performed in synchronization with the horizontal and vertical synchronizing signals and even/odd field decision signal received from the second synchronization detector 58.

[0065] The analog luminance and chrominance signals Y and C can be supplied from output terminals 46 and 50 directly to a television set, or if necessary, they can be combined into a composite video signal and supplied to the television set.

[0066] There are two reasons why the first step in the scan conversion process is to convert the VGA red, green, and blue component signals to the luminance signal Y and color difference signals R - Y and B - Y, rather than to operate directly on the red, green, and blue component signals.

[0067] The first reason concerns the ability of the human eye to detect flicker. The human visual sense is extremely sensitive to luminance flicker, but is not very sensitive to flicker occurring in the color difference signals. The inventors have carried out a computer simulation to evaluate the effect of removing flicker from the color difference signals, using the method employed in the deflickering circuit 30. It was found that the removal of flicker from the color difference signals was less noticeable than the attendant loss of vertical resolution. Removing flicker only from the luminance signal Y and not from the color difference signals R - Y and B - Y therefore helps to minimize the loss of vertical resolution in the scan conversion process, and the flicker remaining in the color difference signals has little effect on perceived picture quality. Furthermore, only one deflickering circuit 30 is required to remove flicker from the luminance signal Y, whereas three such circuits would be required to remove flicker from the VGA red, green, and blue component signals.

[0068] The second reason concerns the sensitivity of the human eye to the color difference signals themselves. The human visual sense is extremely sensitive to changes in the luminance signal Y, but is not very sensitive to changes in the color difference signals. Thus the human eye is unable to detect that the bandwidth of the color difference signals R - Y and B - Y has been cut in half by the low-pass filters 20 and 22. This reduction

of bandwidth enables A/D converters 26 and 28 to operate at half the luminance sampling rate, so that only half as much color-difference data is generated, and frame memories 34 and 36 require only half as much capacity for storing the data. The total size and cost of the scan conversion circuit is thus significantly reduced. Power consumption is also reduced, because of the reduced chrominance clock rate.

[0069] The first embodiment reduces flicker by removing luminance signal components simultaneously having high vertical and low horizontal spatial frequencies, without removing other luminance components, and without removing any perceptible chrominance information. The result is to eliminate most perceived flicker while retaining sufficient vertical resolution for most sizes of text to be read, and much vertical detail to be seen. Computer simulation of the first embodiment shows that at a viewing distance equal to the height of the screen (1H), there is some perceptible flicker, at slanted edges of characters in text, for example, but the flicker is confined to small areas. At a viewing distance equal to three times the height of the screen (3H), the flicker becomes imperceptible.

[0070] The remaining flicker in the first embodiment comes from the horizontal-high-frequency-vertical-high-frequency signal Y_{HH} , so this remaining flicker can be reduced by attenuating the amplitude of the output of the horizontal high-pass filter 74. For example, the multipliers 100, 102, and 104 in FIG. 7 can be adapted to multiply by $-1/8$, $1/4$, and $-1/8$, thereby attenuating the output of the horizontal high-pass filter 74 by a factor of two. A separate amplitude converter can also be provided, as will be described in the fifth embodiment.

Second embodiment

[0071] The second embodiment differs from the first only in the internal structure and operation of the deflickering circuit 30.

[0072] FIG. 9 shows the deflickering circuit 30 in the second embodiment, using the same reference numerals as in FIG. 5 for identical elements. The new elements in the second embodiment are a register 124, a subtractor 126, an amplitude limiter 128, and an adder 130.

[0073] FIG. 10 shows the input-output characteristic of the amplitude limiter 128, the horizontal axis representing input and the vertical axis representing output. For input values up to $\pm L$, the output is identical to the input. For input values between $\pm L$ and $\pm M$, the output remains constant at $\pm L$. Beyond $\pm M$, the output value decreases to zero. The output of the amplitude limiter 128 is thus limited to a maximum amplitude of $\pm L$. Computer simulation indicates that if the value of the vertical high-frequency component V_H output by adder 72 ranges from minus one hundred twenty-seven to plus one hundred twenty-eight, best results are obtained when L is between about ten and twenty.

[0074] The basic principle of the second embodiment

is that the sensitivity of the human eye to flicker depends not only on the spatial extent of the flicker but also on the amplitude of the flicker. A video signal that flickers between black and white, for example, is much more irritating than one that flickers between two slightly different shades of gray. Thus even wide-area flicker can be tolerated up to a limited flicker amplitude.

[0075] Next the operation of the second embodiment will be described. The description will be confined to the operation of the deflickering circuit 30; other parts operate as in the first embodiment.

[0076] Referring again to FIG. 9, the vertical high-frequency signal V_H output by adder 72 is input simultaneously to the horizontal high-pass filter 74 and register 124. As explained earlier, there is a delay equivalent to one pixel between the input and output of the horizontal high-pass filter 74. Operating in synchronization with the clock signal supplied from the first PLL circuit 54, register 124 delays V_H by an equal one-pixel amount. Subtractor 126 subtracts the output of the horizontal high-pass filter 74 from the output of register 124, thereby subtracting from the vertical high-frequency signal V_H those components that are also high in horizontal spatial frequency, and leaving the components that combine high vertical spatial frequency with low horizontal spatial frequency. The output of subtractor 126, denoted V_{HL} , corresponds to hatched regions 114 and 120 in FIG. 8.

[0077] The amplitude limiter 128 limits the output of subtractor 126 as indicated in FIG. 10, thereby limiting the line-to-line amplitude of luminance fluctuations in the vertical direction in areas combining high vertical spatial frequency with low horizontal spatial frequency. Adder 130 adds the output of the amplitude limiter 128 to the output of the horizontal high-pass filter 74, and supplies the resulting sum to adder 78, to be added to the output of register 76. The final output Y_{out} of the deflickering circuit 30 accordingly contains all luminance features with low vertical spatial frequencies or high horizontal spatial frequencies, and also, though with limited amplitude, luminance features combining high vertical spatial frequency with low horizontal spatial frequency.

[0078] Compared with the first embodiment, the deflickering circuit 30 in the second embodiment allows more flicker to pass through, but as the additional flicker is confined to small amplitude levels, the flicker is not readily perceived. Moreover, vertical fine detail which would be lost in the first embodiment is preserved, although in a generally muted form, in the second embodiment.

[0079] Computer simulations indicate that the second embodiment gives results generally similar to the first embodiment, perceived flicker being confined to small areas such as the slanted parts of characters in text, and becoming imperceptible at a distance equal to three screen heights. There is a noticeable improvement, however, in the visibility of vertical detail and the legibility of text.

[0080] The amplitude limiter 128 in the second em-

bodiment is not restricted to the type of characteristic shown in FIG. 10. It may have, for example, the characteristic shown in FIG. 11, which simply limits the output to a maximum amplitude of $\pm L$. Specifically, the output value is identical to the input value up to $\pm L$, and remains constant at $\pm L$ when the input value exceeds $\pm L$. Computer simulation indicates that the characteristic in FIG. 11 leads to slightly better vertical resolution than the characteristic in FIG. 10.

[0081] The amplitude limiter 128 may also be adapted to operate with a plurality of limiting characteristics, which can be selected by a control signal. The control signal may be provided from a manual control device, so that the user can adjust the flicker according to the viewing distance. Alternatively, the control signal may be provided from the computer that provides the input VGA video signal, allowing the computer to recognize the size of characters in the display and adjust the vertical resolution accordingly. Yet another alternative will be described in the fifth embodiment.

Third embodiment

[0082] The third embodiment differs from the first embodiment only in the internal structure and operation of the deflickering circuit 30.

[0083] FIG. 12 shows the deflickering circuit 30 in the third embodiment, using the same reference numerals as in FIG. 5 for identical elements. The first vertical low-pass filter 68 and horizontal high-pass filter 74 are the same as in the first embodiment, but their positions have been interchanged, and the position of register 76 has been moved accordingly. In addition, the line memory 70 of the first embodiment has been replaced by a second vertical low-pass filter 132.

[0084] The horizontal high-pass filter 74 produces a horizontal high-frequency signal H_H containing signal components with high horizontal spatial frequency, irrespective of their vertical spatial frequencies. Subtractor 72 now subtracts H_H from Y_{in} to produce a horizontal low-frequency signal H_L containing signal components with low horizontal spatial frequencies.

[0085] FIG. 13 shows the internal structure of the second vertical low-pass filter 132. The second vertical low-pass filter 132 has an input terminal 134 for receiving the horizontal high-frequency signal H_H , an output terminal 136 coupled to adder 78 in FIG. 12, two line memories 138 and 140 that delay H_H by one line each, three multipliers 142, 144, and 146 that multiply the input and output of line memory 138 and the output of line memory 140 by factors of 0.2, 0.6, and 0.2, respectively, and an adder 147 that adds the outputs of multipliers 142, 144, and 146 and provides their sum to output terminal 136. The line memories 138 and 140 are controlled by signals received from the memory control circuit 56 at input terminal 64. As can be seen by comparing FIGs. 6 and 13, the structure of the second vertical low-pass filter 132 is the same as the structure of the first vertical low-pass

filter 68 except for the values of the multiplier coefficients.

[0086] FIG. 14 shows the frequency characteristic of the first vertical low-pass filter 68, and the mathematical formula for this characteristic. The horizontal axis indicates vertical spatial frequency; the vertical axis indicates amplitude. Cross-hatching indicates the region 148 of remaining flicker. The first vertical low-pass filter 68 completely eliminates the vertical spatial frequency corresponding to 525/2 cPH in the center of this region 148, and strongly attenuates other spatial frequencies in region 148.

[0087] FIG. 15 shows the frequency characteristic of the second vertical low-pass filter 132, and the mathematical formula for this characteristic. The horizontal axis indicates vertical spatial frequency, and the vertical axis indicates amplitude. Cross-hatching again indicates the region of remaining flicker 149. This characteristic has the same general shape as the one in FIG. 14, but the second vertical low-pass filter 132 attenuates all vertical frequencies by a lesser amount than does the first vertical low-pass filter 68, and therefore reduces flicker less than does the first vertical low-pass filter 68.

[0088] FIG. 16 shows the two-dimensional spatial frequency plane and illustrates the principle of operation of the third embodiment. The horizontal and vertical axes have the same meaning as in FIG. 3. The hatched area 150 represents features with low horizontal spatial frequencies. If these features flicker, the flicker occurs over a horizontally wide area, so the flicker is obvious and irritating. The non-hatched area 152 represents features with high horizontal spatial frequencies, in which flicker is less perceptible.

[0089] The third embodiment reduces flicker in both areas 150 and 152, but with different vertical low-pass filters, so that flicker is reduced more in area 150 than in area 152. The first vertical low-pass filter 68 is used to reduce the readily perceptible flicker in area 150. The second vertical low-pass filter 132 is used to reduce the less perceptible flicker in area 152. This arrangement enables perceptible flicker to be eliminated almost completely, while still retaining enough vertical resolution to show small vertical features.

[0090] Next the operation of the third embodiment will be described. The description will be confined to the operation of the deflickering circuit 30, since other elements operate as in the first embodiment.

[0091] Referring again to FIG. 12, the digital luminance signal Yin received at input terminal 62 is supplied to the horizontal high-pass filter 74 and register 76. The horizontal high-pass filter 74 rejects low horizontal spatial frequencies (area 150 in FIG. 16), and outputs the horizontal high-frequency signal H_H (which contains the horizontal spatial frequencies in area 152 in FIG. 16) with a one-pixel delay. Register 76 provides an equivalent delay. Subtractor 72 subtracts the output of the horizontal high-pass filter 74 from the output of register 76 to produce the horizontal low-frequency signal H_L ,

which contains the frequency components in the hatched area 150 in FIG. 16.

[0092] These signals H_L and H_H are input to the first vertical low-pass filter 68 and second vertical low-pass filter 132, respectively. Operating as indicated by the frequency characteristics in FIGs. 14 and 15, the first vertical low-pass filter 68 strongly attenuates the high vertical spatial frequencies in the hatched region 150 in FIG. 16, while the second vertical low-pass filter 132 attenuates high vertical spatial frequencies in region 152 less strongly. Adder 78 adds the outputs of vertical low-pass filters 68 and 132 to produce the filtered luminance signal Yout supplied to output terminal 66.

[0093] Although the third embodiment performs horizontal high-pass filtering and vertical low-pass filtering in the reverse of the order in the first embodiment, the resulting attenuation of signal components combining high vertical spatial frequency with low horizontal spatial frequency is the same as in the first embodiment. Since the third embodiment also attenuates signal components with high vertical and high horizontal spatial frequencies, flicker is reduced to a greater extent than in the first embodiment; the small-scale flicker which remained in the first embodiment is substantially imperceptible in the third embodiment. Since the attenuation of high-vertical-high-horizontal spatial frequencies is less than the attenuation of high-vertical-low-horizontal spatial frequencies, however, more vertical resolution remains than if all high vertical spatial frequencies were filtered by the first vertical low-pass filter 68.

[0094] The third embodiment is not restricted to the frequency characteristics shown in FIGs. 14 and 15. These characteristics can be modified by altering the multiplier coefficients, for example, or providing additional filter taps (additional line memories and multipliers). Non-linear filters with amplitude limiters similar to the amplitude limiter 128 in the second embodiment can also be used. In general, any type of low-pass filter can be used, as long as the first vertical low-pass filter 68 attenuates high vertical spatial frequencies more strongly than does the second vertical low-pass filter 132.

[0095] The third embodiment can also be modified by dividing the two-dimensional spatial frequency plane into more than two regions. A pair of horizontal spatial filters can be used to obtain three signals with high, medium, and low horizontal spatial frequencies, for example, and a different vertical low-pass filter can be provided for each. The low horizontal spatial frequencies should then receive the strongest flicker attenuation, and the highest horizontal spatial frequencies should receive the least flicker attenuation.

Fourth embodiment

[0096] The fourth embodiment also differs from the first embodiment only in the internal structure and operation of the deflickering circuit 30.

[0097] FIG. 17 shows the deflickering circuit 30 in the fourth embodiment, using the same reference numerals as in FIG. 5 for the input and output terminals 62, 64, and 66. The deflickering circuit 30 in the fourth embodiment has a single vertical high-low separation filter 154 comprising two line memories 156 and 158, three multipliers 160, 162, and 164, two adders 166 and 168, and a subtractor 170. Subtractor 170 outputs a vertical high-frequency signal V_H to an amplitude limiter 171, which is controlled by a direct-current detector 172. Adder 168 outputs a vertical low-frequency signal V_L to another adder 173, which adds V_L to the output of the amplitude limiter 171 and supplies the resulting filtered luminance signal Y_{out} to output terminal 66.

[0098] FIG. 18 shows the structure of the direct-current detector 172. The luminance signal Y_{in} is received at an input terminal 174 and supplied to an averaging circuit 175 and a delay circuit 176. The averaging circuit 175 takes the average of the luminance signal Y_{in} over a certain number of horizontally adjacent pixels. A subtractor 177 subtracts the average value obtained by the averaging circuit 175 from the output of the delay circuit 176 and outputs their difference Y_E to a comparator 178 that generates a control signal S at an output terminal 179.

[0099] The fourth embodiment operates on the principle, mentioned earlier, that the human visual sense perceives high-amplitude flicker more readily than low-amplitude flicker. Perceived flicker in the fourth embodiment is accordingly reduced by limiting the amplitude of high-frequency vertical luminance fluctuations. In areas with only very low horizontal spatial frequencies, where the luminance level is substantially constant in the horizontal direction and flicker would be most noticeable, high-frequency vertical luminance fluctuations are not only limited but reduced to zero.

[0100] Areas of horizontally constant luminance level are areas in which, in each horizontal scanning line, the luminance signal has a direct-current or DC character. The term "DC-like" will be used below to mean "substantially constant in luminance level in the horizontal direction."

[0101] Next the operation of the deflickering circuit 30 in the fourth embodiment will be described. Other elements of the fourth embodiment operate as in the first embodiment.

[0102] Referring again to FIG. 17, the line memories 156 and 158 and multipliers 160, 162, and 164 operate in the same way as the line memories 80 and 82 and multipliers 84, 86, and 88 in the first vertical low-pass filter 68 of the preceding embodiments, shown in FIG. 6. The two adders 166 and 168 take the sum of the outputs of all three multipliers 160, 162, and 164, so the vertical low-frequency signal V_L output by the vertical separation filter 154 in the fourth embodiment is identical to the vertical low-frequency signal V_L output by the first vertical low-pass filter 68 in the first embodiment.

[0103] Subtractor 170 subtracts the sum of the out-

puts of multipliers 160 and 164 from the output of multiplier 162. The line memories 156 and 158, multipliers 160, 162, and 164, adder 166, and subtractor 170 function as a vertical high-pass filter in the same way that the registers 96 and 98, multipliers 100, 102, and 104, and adder 106 functioned as a horizontal high-pass filter in FIG. 7. The signal V_H output by subtractor 170 is complementary to the signal V_L output by adder 168 in that if V_H and V_L are added together, the result is identical to the luminance signal Y_{in} received at input terminal 62 (with a one-line delay). The vertical high-frequency signal V_H output by the vertical separation filter 154 is therefore identical to the high-frequency signal V_H obtained by the subtractor 72 in FIG. 5 in the first embodiment.

[0104] Referring to FIG. 18, the averaging circuit 175 takes the average of, for example, five consecutive samples of the luminance signal Y_{in} . The delay circuit 176 delays Y_{in} by a corresponding amount, three samples for example, so that the subtractor 177 obtains the difference between the average value obtained by the averaging circuit 175 and, preferably, the middle (e.g. third) sample value among the sample values averaged by the averaging circuit 175. The comparator 178 compares the absolute value of this difference Y_E with a positive threshold value β , activates the control signal S at output terminal 179 when $-\beta \leq Y_E \leq \beta$, and de-activates S when $Y_E < -\beta$ or $\beta < Y_E$.

[0105] Control signal S will accordingly be active in those portions of a horizontal scanning line in which the luminance level is substantially constant, or is changing at a substantially constant rate.

[0106] The averaging circuit 175 is not limited to taking the average of five consecutive samples. Other numbers of samples can be used.

[0107] FIG. 19 shows the input-output characteristics of the amplitude limiter 171, input being indicated on the horizontal axis and output on the vertical axis. The amplitude limiter 171 is adapted to operate with two input-output characteristics, which are selected by the control signal S from the direct-current detector 172.

[0108] The first characteristic 180, which is selected when the control signal S is inactive, is similar to the characteristic of the amplitude limiter 128 in the second embodiment, the output value being limited to the range between $-L$ and $+L$ and equal to the input value within that range.

[0109] The second characteristic 181, which is selected when the control signal S is active, limits the output value to zero, regardless of the input value.

[0110] By adding V_L to the output of the amplitude limiter 171, adder 173 restores all frequency components of the luminance signal Y , except that the amplitude of luminance fluctuations having high vertical spatial frequency has been limited. Also, in areas with a flat luminance gradient in the horizontal direction, the vertical high-frequency signal V_H is completely removed, instead of just being limited.

[0111] Compared with the second embodiment, the fourth embodiment reduces flicker to a lower level in areas of high horizontal spatial frequency by limiting the amplitude of V_H in these areas (the second embodiment limited V_H only in areas of low horizontal spatial frequency). One result is that the flicker at slanted edges of characters noted in the second embodiment is greatly reduced.

[0112] In areas of low horizontal spatial frequency, the fourth embodiment identifies the lowest horizontal spatial frequencies, which have DC-like characteristics, and reduces V_H to zero in those areas. As a result, in other areas of low horizontal spatial frequency, the amplitude of V_H does not have to be limited as severely as in the second embodiment. The value of the parameter L in the fourth embodiment can be higher than in the second embodiment, although L is still preferably in the range from about ten to about twenty.

[0113] In displays of charts and tables, the fourth embodiment reduces flicker more than the second embodiment does, both in areas of text, where V_H is limited, and at horizontal dividing or boundary lines, by where V_H is held to zero. This makes such displays easier to look at, although the text may appear fainter than in the second embodiment.

[0114] An advantage of the fourth embodiment, as compared with the second embodiment, is that it requires less hardware. The vertical separation filter 154 in the fourth embodiment is functionally equivalent to the combination of the first vertical low-pass filter 68, line memory 70, and subtractor 72 in the first embodiment. If compared with this combination, the vertical separation filter 154 can be seen to require one more subtractor but one less line memory. A subtractor, which only has to operate on two luminance values, has far fewer circuit elements than a line memory, which must store an entire scanning line of luminance values.

[0115] This advantage can be transferred to the first and second embodiments, and to other embodiments that follow, by substituting the vertical separation filter 154 of the fourth embodiment for the combination of the first vertical low-pass filter 68, line memory 70, and subtractor 72 in those other embodiments.

[0116] The fourth embodiment is not restricted to the pair of amplitude limiting characteristics illustrated in FIG. 19. Another pair of limiting characteristics which can be employed effectively will be described in the sixth embodiment. The amplitude limiter 171 may also operate with more than two limiting characteristics, which the comparator 178 can select by comparing the difference output by subtractor 177 with two or more threshold values.

Fifth embodiment

[0117] The fifth embodiment also differs from the first embodiment only in the internal structure and operation of the deflickering circuit 30.

[0118] FIG. 20 shows the deflickering circuit 30 in the fifth embodiment, using the same reference numerals as in FIG. 9 for elements that are the same as in the second embodiment. The additional elements in the fifth embodiment are the amplitude limiter 171 of the fourth embodiment, an amplitude converter 182 inserted between the horizontal high-pass filter 74 and adder 130, and a direct-current detector 183 that controls the amplitude limiter 171. The signals V_L , V_H , Y_{HH} , and V_{HL} have the same values as in the second embodiment.

[0119] FIG. 21 shows the input-output characteristic of the amplitude converter 182, input being indicated on the horizontal axis and output on the vertical axis. The amplitude converter 182 multiplies all input values by a constant value of 0.5, thereby reducing the amplitude of luminance fluctuations with high vertical and high horizontal spatial frequencies by one-half.

[0120] Next the operation of the deflickering circuit 30 in the fifth embodiment will be described with reference to FIGs. 20 and 21, omitting a description of the elements in the deflickering circuit 30 that operate in the same way as in the second and fourth embodiments. These elements include the first vertical low-pass filter 68, line memory 70, horizontal high-pass filter 74, registers 76 and 124, subtractor 72, adders 78 and 130, and limiter 171.

[0121] The output Y_{HH} of the horizontal high-pass filter 74, representing luminance fluctuations with high horizontal and high vertical spatial frequency, is processed by the amplitude converter 182 so as to reduce the amplitude of these luminance fluctuations by a factor of 0.5, as indicated in FIG. 21. The effect is to make small-scale flicker less noticeable by reducing the amplitude of the flicker.

[0122] The output Y_{HH} of the horizontal high-pass filter 74 is also supplied to the direct-current detector 183. The direct-current detector 183 compares Y_{HH} with a fixed threshold value α . If $-\alpha \leq Y_{HH} \leq \alpha$, the luminance signal Y_{in} is considered to be of a DC nature in either the vertical or horizontal direction, and the control signal S is activated. If $Y_{HH} < -\alpha$, or if $\alpha < Y_{HH}$, the control signal S is made inactive. Computer simulations indicate that if Y_{HH} varies from minus one hundred twenty-seven to plus one hundred twenty-eight, good results are obtained when α is between one and three.

[0123] The amplitude limiter 171 operates as in the fourth embodiment, limiting V_H to a maximum amplitude of $\pm L$ when control signal S is inactive, and to zero when S is active. When the control signal S is active because Y_{in} is substantially constant or DC-like in the vertical direction, V_H is close to zero to begin with, so V_{HL} is close to zero, and reducing V_{HL} to zero has little noticeable effect. When the control signal S is active because Y_{in} is substantially constant in the horizontal direction, reducing V_{HL} to zero prevents the type of flicker that occurs at horizontal dividing lines in tables and charts, as in the fourth embodiment.

[0124] The filtered luminance signal Y_{out} output by

the deflickering circuit 30 in the fifth embodiment is similar to Yout in the fourth embodiment in that flicker reduction is applied to all high vertical spatial frequencies. The difference is that whereas the fourth embodiment used amplitude limiting in areas of high horizontal spatial frequency, the fifth embodiment employs amplitude attenuation by a constant factor of one-half. In text displays where there is a large difference between the luminance levels of the text and background, as when dark text is displayed on a light background or vice versa, the fifth embodiment reduces the luminance difference less than did the fourth embodiment, making the text more readable.

[0125] As a variation of the fifth embodiment, the amplitude converter 182 can employ a non-linear amplitude modification characteristic, instead of the linear characteristic shown in FIG. 21. As another variation, instead of reducing the Y_{HH} amplitude, the amplitude converter 182 can increase the Y_{HH} amplitude in order to enhance vertical resolution, although this will make small-scale flicker more noticeable. As yet another variation, the amplitude converter 182 can be provided with a plurality of amplitude modification characteristics, which can be selected by the user or by the computer according to picture content. For example, the amplitude converter 182 can be adapted to multiply the Y_{HH} values by two in order to enhance vertical resolution, by one-half in order to reduce flicker, or by unity when neither of these effects is required.

[0126] Variations in the amplitude limiter 171 and direct-current detector 183 are also possible. The amplitude limiter 171 can be provided with more than two limiting characteristics, which are selected by the direct-current detector 183 by comparing Y_{HH} with a plurality of threshold values. To speed up the comparison process, instead of comparing Y_{HH} with positive and negative threshold limits (e.g. with $-\alpha$ and α as described above), the direct-current detector 183 can take the absolute value of Y_{HH} ($|Y_{HH}|$) and compare $|Y_{HH}|$ only with positive threshold values (e.g. α).

[0127] The direct-current detector 183 may also detect horizontally DC-like signals by testing the luminance signal Y_{in} received at input terminal 62, as in the fourth embodiment, or by testing the vertical high-frequency signal V_H output from subtractor 72, instead of testing Y_{HH} . The condition by which DC-like signals are detected may be more complex than simple comparison with a threshold value. The direct-current detector 183 may be a microcontroller or other computing device programmed to test such more complex conditions.

Sixth embodiment

[0128] The sixth embodiment also differs from the first embodiment only in the internal structure and operation of the deflickering circuit 30.

[0129] FIG. 22 shows the deflickering circuit 30 in the sixth embodiment, using the same reference numerals

as in FIG. 20 to denote elements corresponding to elements in the fifth embodiment. The sixth embodiment differs from the fifth embodiment in that the deflickering circuit 30 has no amplitude converter 182, the horizontal high-pass filter 74 of the fifth embodiment is replaced by a horizontal low-pass filter 184, and the amplitude limiter 185 operates differently from the amplitude limiter 171 in the fifth embodiment.

[0130] Although the preceding embodiments reject frequency components in areas 114 and 120 in FIG. 8, the rejection is not complete. The first vertical low-pass filter 68 has the characteristic shown in FIG. 14, which permits flicker-causing vertical spatial frequencies to remain to the extent indicated by the hatched region 148. The amplitude limiter 185 is adapted to cancel out these remaining flicker components when a DC-like signal is detected.

[0131] The output V_{HL} of the horizontal low-pass filter 184 has the same value as V_{HL} in the fifth embodiment. A subtractor 186 subtracts V_{HL} from V_H , with a one-pixel delay of V_H in register 124 to synchronize the two signals. The resulting difference Y_{HH} has the same value as Y_{HH} in the fifth embodiment.

[0132] FIG. 23 shows the structure of the horizontal low-pass filter 184. The signal V_H is received at an input terminal 188, stored in a first register 190, then passed to a second register 192. The input to the first register 190, the output from the first register 190, and the output from the second register 192 are furnished to respective multipliers 194, 196, and 198, and multiplied by respective weighting coefficients of $1/4$, $1/2$, and $1/4$. The outputs of the multipliers 194, 196, and 198 are added by an adder 200 and provided to an output terminal 202. The signal output at terminal 202 is V_{HL} .

[0133] The direct-current detector 183 operates in the sixth embodiment as in the fifth embodiment, by comparing Y_{HH} with a threshold α , and detecting a DC-like signal and activating the control signal S when $-\alpha \leq Y_{HH} \leq \alpha$. Computer simulation indicates that if Y_{HH} varies between minus one hundred twenty-seven and plus one hundred twenty-eight, best results are obtained when the value of α is about three.

[0134] As in the fifth embodiment, the amplitude limiter 185 receives V_{HL} and operates with two limiting characteristics which are selected by the control signal S . These limiting characteristics differ from the limiting characteristics of the amplitude limiter 171 in the fifth embodiment.

[0135] FIG. 24 shows the characteristic selected when the control signal S is inactive. Input values are indicated on the horizontal axis, and output values on the vertical axis. Input values with absolute values of ten or less are output without alteration. Input values with absolute values from ten to thirty-two are limited to an output value of ten. Input values with absolute values higher than thirty-two are limited to zero.

[0136] FIG. 25 shows the characteristic selected when the control signal S is active, again with input on

the horizontal axis and output on the vertical axis. Input values with absolute values of ten or less are limited to zero. Input values from minus one-hundred twenty-eight to minus ten are output as values from 11.8 to zero, according to the following formula, thereby reversing the sign of the V_{HL} signal.

$$\text{Output} = -0.1 \times (\text{input} + 10)$$

Input values from ten to one-hundred twenty-eight are output as values from zero to -11.8 according to the following formula, again reversing the sign of the V_{HL} signal.

$$\text{Output} = -0.1 \times (\text{input} - 10)$$

[0137] Adders 130 and 78 add the output of the amplitude limiter 185 to the signals V_L and Y_{HH} output from register 76 and subtractor 186 to create the filtered luminance signal Y_{out} .

[0138] The operation of the sixth embodiment will next be described for two cases.

[0139] Referring to FIG. 26, the first case is that of a signal which is DC-like in the horizontal direction but has a luminance step transition in the vertical direction. The black dots at the top of FIG. 26 represent seven vertically adjacent pixels, the first three having a luminance value of zero and the second four having a luminance value of sixty-four. The first vertical low-pass filter 68 converts this step-like vertical Y_{in} waveform to the smoother V_L waveform. Subtractor 72 obtains the V_H waveform shown below. The signal is by assumption DC-like in the horizontal direction, so V_{HL} is identical to V_H and Y_{HH} (not shown) is zero. The direct-current detector 183 compares Y_{HH} with α and activates control signal S. Operating with the characteristic shown in FIG. 25, the amplitude limiter 171 reduces V_{HL} to the Y_{LIM} waveform shown at the bottom of FIG. 26.

[0140] The output waveform Y_{out} is the sum of V_L , Y_{LIM} , and Y_{HH} (which is zero). Due to the reversal of the sign of Y_{LIM} , Y_{out} rises from a luminance level of zero to a luminance level of sixty-four even more gradually than does V_L . Flicker is removed substantially completely. Referring again to FIG. 14, which shows the spatial frequency characteristic of the first vertical low-pass filter 68 that produces V_L , the reversal of the sign of V_{HL} has removed the residual flicker in region 148.

[0141] Referring to FIG. 27, the second case is that of a signal which has the same vertical luminance step transition, but is not DC-like in the horizontal direction. Y_{in} , V_L , and V_H are the same as in FIG. 26, but the amplitude limiter 171 now operates with the characteristic shown in FIG. 24, so Y_{LIM} resembles a truncated version of V_H . The exact shape of the Y_{LIM} waveform depends on the V_{HL} waveform (not shown), which is no longer identical to V_H because Y_{HH} (also not shown) is no longer

er zero, but in any case, the sum of V_L , Y_{LIM} , and Y_{HH} differs from the input waveform Y_{in} only to the extent that Y_{LIM} differs from V_{HL} , so a Y_{out} waveform like the one shown is obtained. The transition from zero to sixty-four in this Y_{out} waveform takes place with nearly the same abruptness as the transition in the input waveform Y_{in} . There is accordingly substantially no loss of vertical resolution.

[0142] Computer simulation shows that in scan conversion of computer-generated tables and chart, the sixth embodiment can almost completely remove the residual flicker associated with horizontal lines, while maintaining excellent legibility of small text.

15 Seventh embodiment

[0143] The seventh embodiment also differs from the first embodiment only in the internal structure and operation of the deflickering circuit 30.

20 **[0144]** FIG. 28 shows the deflickering circuit 30 in the seventh embodiment. The first vertical low-pass filter 68, line memory 70, subtractor 72, adder 78, and amplitude limiter 185 are the same as in the sixth embodiment, except that the amplitude limiter 185 operates directly on the vertical high-frequency signal V_H output by the subtractor 72. The limiting characteristics of the amplitude limiter 185 are the characteristics shown in FIGs. 24 and 25. The control signal S that selects these characteristics is generated by the direct-current detector 172 employed in the fourth embodiment, which receives the delayed luminance signal Y_{in} output from line memory 70.

30 **[0145]** A detailed description of the seventh embodiment will be omitted, as all elements of the seventh embodiment have been described in preceding embodiments.

35 **[0146]** The operation of the seventh embodiment is generally similar to the operation of the sixth embodiment, except that the amplitude limiter 185 operates on the entire vertical high-frequency component V_H , instead of just the horizontal low-frequency part. Flicker is therefore removed more completely than in the sixth embodiment. When the direct-current detector 172 detects a horizontally DC-like input signal Y_{in} , the limiting characteristic in FIG. 25 is selected, and residual flicker is canceled out by a reversal of the sign of V_H , as in the sixth embodiment. When the input signal Y_{in} is not horizontally DC-like, the characteristic in FIG. 24 is selected, limiting the amplitude of the vertical high-frequency flicker.

40 Eighth embodiment

45 **[0147]** The eighth embodiment differs from the preceding embodiments in having a selectable enlargement mode.

[0148] FIG. 29 shows the structure of the eighth embodiment, using the same reference numerals as in FIG.

4 for identical elements. Descriptions of these elements will be omitted. Like the preceding embodiments, the eighth embodiment converts a progressively scanned VGA signal to an interlaced NTSC signal. The differences between the eighth embodiment and the preceding embodiments concern the internal structure of the deflickering circuit 220 and memory control circuit 222, an input terminal 224 at which the memory control circuit 222 receives expansion information, and three horizontal interpolating circuits 226, 228, and 230 inserted between the frame memories 32, 34, and 36 and D/A converters 38, 40, and 42.

[0149] FIG. 30 shows the structure of the deflickering circuit 220 in the eighth embodiment, using the same reference numerals as in FIG. 22 for elements that are identical to elements in the sixth embodiment. In addition to input terminals 62 and 64, the deflickering circuit 220 has a third input terminal 232 for receiving a mode control signal from the memory control circuit 222 in FIG. 29, and two output terminals 234 and 236. The vertical low-pass filter 238 differs in internal structure from the first vertical low-pass filter 68 in the sixth embodiment, and provides outputs to a selector 240 as well as providing the vertical low-frequency signal V_L . The selector 240 also receives the sum output by adder 78, and provides output signals to the output terminals 234 and 236. Both output terminals 234 and 236 are coupled to frame memory 32. The other elements in FIG. 30 are identical to the corresponding elements in FIG. 22.

[0150] FIG. 31 shows the internal structure of the vertical low-pass filter 238. The luminance signal Y_{in} received at input terminal 62 is supplied to a cascaded pair of line memories 242 and 244. The input to line memory 242, the output from line memory 242, and the output from line memory 244 are supplied, respectively, to three multipliers 246, 248, and 250 and multiplied by $1/4$. The output of line memory 242 is also supplied to a fourth multiplier 252 and multiplied by $1/2$. A first adder 254 adds the outputs of multipliers 246 and 248. A second adder 256 adds the outputs of multipliers 248 and 250. A third adder 258 adds the outputs of adders 254 and 256. A fourth adder 260 adds the output of multiplier 252 to the output of the first adder 254. A fifth adder 262 adds the output of multiplier 252 to the output of the second adder 256. The sum obtained by adder 260 is provided to a first output terminal 266. The sum obtained by adder 262 is provided to a second output terminal 268.

[0151] FIG. 32 shows the structure of the first horizontal interpolating circuit 226. The luminance signal read from the first frame memory 32 in FIG. 29 is received at an input terminal 270, while control signals from the memory control circuit 222 are received at input terminals 272 and 274. The signal received at input terminal 272 alternately selects the input luminance signal and an interpolated signal, as described below. The signal received at input terminal 274 selects a normal mode or an expanded mode. The output terminal 276 of the first

horizontal interpolating circuit 226 is coupled to the first D/A converter 38 in FIG. 29.

[0152] Input terminal 270 feeds the luminance signal into a cascaded pair of registers 278 and 280, each of which provides a one-pixel delay. An adder 282 adds the input of register 278 and the output of register 280, and a multiplier 284 multiplies the resulting sum by $1/2$. A first selector 286 selects either the output of register 278 or the output of multiplier 284, responsive to the signal received at input terminal 272. A second selector 288 selects either the output of the first selector 286 or the signal input at terminal 270, responsive to the mode signal received at input terminal 274, and provides the selected signal to the output terminal 276.

[0153] The other horizontal interpolating circuits 228 and 230 are identical in structure to the first horizontal interpolating circuit 226, although they operate on the color difference signals read from the second and third frame memories 34 and 36, and provide output to the second and third D/A converters 40 and 42.

[0154] Next the concept behind the eighth embodiment will be briefly explained.

[0155] The preceding embodiments reduced flicker with comparatively little loss of vertical resolution, but some loss of vertical resolution inevitably occurs, so those embodiments are unable to preserve the legibility of the smallest sizes of computer-generated text. If such text is to be read after scan conversion, it must be expanded during the scan conversion process. The eighth embodiment expands an arbitrary rectangular area having half the width and half the height of the screen, so that this area fills the screen.

[0156] For reasons described earlier, expansion by direct interpolation from one field into another leads to flicker problems. The eighth embodiment accordingly operates as shown in FIG. 33. In step 290, the memory control circuit 222 determines, from the received expansion information, whether expansion is required in the current frame. If expansion is required, in step 292 the memory control circuit 222 determines, from the expansion information, the location of the part of the original image that is to be expanded.

[0157] The actual expansion process is carried out in steps 294, 296, and 298. In step 294 vertical interpolation is performed to expand the height of the image, by using the same pixel data for both even and odd fields. Next flicker is suppressed in step 296 by means of a vertical low-pass filter with three taps. In step 298, horizontal interpolation is performed to expand the width of the image, by interpolating average values.

[0158] Where expansion is not carried out, the interpolation processes are bypassed and only a flicker-suppression step 300 is carried out.

[0159] Steps 294 and 296 are further illustrated in FIG. 34. The symbols a_{n-1} , a_n , and a_{n+1} represent three vertically adjacent input pixels in the same frame. In the vertical interpolation step 294, each input pixel value is copied to two pixel positions, one in an odd scanning

line, and the other in the even scanning line just below. Input pixels a_{n-1} , a_n , and a_{n+1} thereby produce six vertically adjacent pixels. This step doubles the height of the expanded part of the image by doubling the number of scanning lines in that part.

[0160] In the flicker suppression step 296, the vertically expanded image is filtered by a vertical low-pass filter with tap values of $1/4$, $1/2$, and $1/4$. The value of the pixel in the n -th scanning line of the odd field then becomes $(3a_n + a_{n-1})/4$, while the value of the pixel in the n -th scanning line of the even field becomes $(a_{n+1} + 3a_n)/4$. This filtering reduces flicker.

[0161] In the horizontal interpolation step 298 in FIG. 33, the image resulting from the flicker suppression step 296 is expanded horizontally by introducing a new pixel between each pair of horizontally adjacent pixels, the value of the new pixel being the average of the two horizontally adjacent pixels.

[0162] The operation of the eighth embodiment will next be described with reference to FIGs. 29 to 32, omitting descriptions of operations that are the same as in the first embodiment.

[0163] From the VGA horizontal synchronizing signal received from the first synchronization detector 52 and the expansion information received from input terminal 224, the memory control circuit 222 generates read and write control signals for line memories 70, 242, and 244 in the deflickering circuit 220 and its vertical low-pass filter 238, and generates signals that control selector 240 in the deflickering circuit 220 and the second selectors 288 in the horizontal interpolating circuits 226, 228, and 230. The line memories 70, 242, and 244 are FIFO memories. The read and write control signals include line address reset signals, read and write enable signals, and read and write clock signals as in the first embodiment. From the VGA horizontal and vertical synchronizing signals received from the first synchronization detector 52 and the expansion information received from input terminal 224, the memory control circuit 222 also generates write control signals for the frame memories 32, 34, and 36.

[0164] The digital luminance signal Y_{in} received from A/D converter 24 at input terminal 62 in FIG. 30 is supplied to the vertical low-pass filter 238 and line memory 70. Referring to FIG. 31, in the vertical low-pass filter 238, this signal Y_{in} is received by line memory 242 and multiplier 246. After a one-line delay in line memory 242, the signal is passed to line memory 244 and multipliers 248 and 252. After a further one-line delay in line memory 244, the signal is passed to multiplier 250. Line memories 242 and 244 are controlled by read and write control signals received from the memory control circuit 222 at input terminal 64.

[0165] The symbols a_{n+1} , a_n , and a_{n-1} in FIG. 31 have the same meaning as in FIG. 34, representing three vertically adjacent pixels. From the multiplier coefficients and the interconnections of the multipliers and adders it can readily be seen that the vertical low-pass filter 238

produces the value $(a_{n-1} + 2a_n + a_{n+1})/4$ at output terminal 264, the value $(a_{n+1} + 3a_n)/4$ at output terminal 266, and the value $(3a_n + a_{n-1})/4$ at output terminal 268. The latter two values are provided from output terminals 266 and 268 directly to the selector 240 in FIG. 30.

[0166] The value $(a_{n-1} + 2a_n + a_{n+1})/4$ obtained at output terminal 264 is the same as the value output by the first vertical low-pass filter 68 (FIG. 6) in the sixth embodiment, denoted V_L . The line memory 70, subtractors 72 and 186, registers 76 and 124, adders 78 and 130, direct-current detector 183, horizontal low-pass filter 184, and amplitude limiter 185 are the same as in the sixth embodiment, so the output of adder 78 is the same as the filtered luminance signal Y_{out} in the sixth embodiment. The output of adder 78 is supplied to selector 240.

[0167] Further processing differs depending on whether expansion is or is not performed, so the two cases will be described separately.

[0168] When scan conversion is performed without expansion, the memory control circuit 222 sends selector 240 in FIG. 30 a normal mode signal causing selector 240 to select the output of adder 78. As in the preceding embodiments, each frame memory 32, 34, and 36 stores two fields of data separately, an odd field and an even field, and the memory control circuit 222 generates a control signal selecting either the odd field or the even field. When the odd field is selected, this control signal causes selector 240 to route odd scanning lines of data output by adder 78 to output terminal 234 in FIG. 30, and these scanning lines are written in the odd field in frame memory 32. When the even field is selected, this control signal causes selector 240 to route even scanning lines of data output by adder 78 to output terminal 236, and these scanning lines are written in the even field in frame memory 32.

[0169] Color difference signal data are written in field memories 34 and 36 as in the preceding embodiments. Data are also read from field memories 32, 34, and 36 as in the preceding embodiments. Referring to FIG. 32, the memory control circuit 222 sends selector 288 in the three horizontal interpolating circuits 226, 228, and 230 a normal-mode control signal causing selector 288 to select the data received at input terminal 270, so that these data pass through unaltered from input terminal 270 to output terminal 276, as if the horizontal interpolating circuits 226, 228, and 230 were not present.

[0170] From the above description it can be seen that when expansion is not performed, the eighth embodiment operates like the sixth embodiment. The data written in the frame memories 32, 34, and 36 in this case will be referred to as normal image data.

[0171] When expansion is performed, the memory control circuit 222 determines, from the expansion information received at input terminal 224, which part of the input image is to be expanded, and sends an expansion-mode signal to the deflickering circuit 220. Referring to FIGs. 30 and 31, this signal causes selector 240 to select the signals at output terminals 266 and 268 of the

vertical low-pass filter 238 and route these signals to output terminals 236 and 234, respectively. Each horizontal scanning line input to the vertical low-pass filter 238 thereby generates two output scanning lines: an odd scanning line at output terminal 234 and an even scanning line at output terminal 236.

[0172] Within the area to be expanded, for the luminance signal, the memory control circuit 222 supplies write control signals and address signals that cause the data generated at output terminal 234 to be written in the odd field of frame memory 32, and the data generated at output terminal 236 to be written simultaneously in the even field of frame memory 32. For the color difference signals, the memory control circuit 222 supplies write control signals that cause each horizontal scanning line to be written simultaneously into both the even and odd fields of frame memories 34 and 36. That is, the color difference signals are interpolated by controlling the frame memories 34 and 36 so that the same horizontal scanning line data are written in both the even and odd fields. Data for pixels not appearing in the area being expanded are not written in the field memories 32, 34, and 36. The memory control circuit 222 can generate the necessary write addresses by a counting process referenced to, for example, the top left corner of the expanded area.

[0173] Within the expanded area, the luminance data are both expanded and filtered to reduce flicker. The color difference data are expanded but not filtered. As in the preceding embodiments, not filtering the color difference data reduces the hardware requirements of the scan conversion circuit, and chrominance flicker is not readily perceived by the human eye.

[0174] The reading of expanded image data from the frame memories 32, 34, and 36 also differs from the reading of normal image data. Pixel data not located in the area to be expanded are not read. In the expanded area, the read control signals generated by the memory control circuit 222 for the frame memories 32, 34, and 36 have half the frequency of the normal read signals. Referring to FIG. 32, when a luminance pixel is read from frame memory 32 into the horizontal interpolating circuit 226, it is simultaneously stored in register 278 and sent to adder 282. The previous pixel (horizontally adjacent to the left) is simultaneously moved from register 278 to register 280. Adder 282 and multiplier 284 obtain the average of the pixel value input to register 278 and the pixel value held in register 280.

[0175] After the pixel has been read into register 278, the memory control circuit 222 first sends selectors 272 and 274 control signals causing the output of multiplier 284 to be selected. The average value of two adjacent pixels is thus sent from output terminal 276 to D/A converter 38.

[0176] Next, while registers 278 and 280 continue to hold the same pixel values, the memory control circuit 222 alters the control signal at input terminal 272 so that selector 286 selects the output of register 278, and the

pixel value held in register 278 is sent to output terminal 276 and D/A converter 38. Each pixel input to the horizontal interpolating circuit 226 thus generates two output pixels.

[0177] The above process is repeated for each pixel in the area that is being expanded, selector 286 selecting the outputs of multiplier 284 and register 278 alternately. In this way the image is expanded by a factor of two horizontally, by horizontal average-value interpolation between each pair of pixels in the original image. This does not produce flicker because the interpolated pixels are disposed in the same field as the original pixels.

[0178] The color-difference signals are processed in the same way by horizontal interpolating circuits 228 and 230, so that the chrominance signal is also expanded horizontally by interpolation of average values.

[0179] In expansion mode, the frame memories 32, 34, and 36 need store only half of the pixel data for each horizontal scanning line. Performing horizontal interpolation after scan conversion thus has the effect of reducing the power consumption of the scan conversion circuitry, by reducing the number of read and write accesses to the frame memories 32, 34, and 36.

[0180] The expansion information received at input terminal 224 can be generated by the computer in response to user commands. A typical use of the expansion function is to let the user zoom in on a desired part of a display. An expanded view of the entire display can be obtained by vertical and horizontal scrolling. By expanding the display, the eighth embodiment can greatly enhance the readability of text, while strongly suppressing flicker.

[0181] The eighth embodiment has been described as taking an arbitrary rectangular area with half the width and half the height of the original display, and expanding this area to fill the screen. It is also possible, however, to expand a smaller portion of the original display and replace only part of the original image with the expanded image. This can be accomplished by suitable modification of the read, write, and mode control signals output by the memory control circuit 222.

[0182] The eighth embodiment is not restricted to horizontal expansion by interpolation of average values. Generally similar results can be obtained by simply repeating each pixel value to generate two horizontally adjacent pixels.

[0183] As described above, the invention improves the legibility of computer-generated text in tables, charts, menus, and the like while reducing the flicker caused by the horizontal dividing lines or boundary lines of these items, but the effect of the invention extends further. Without causing obvious flicker, the invention enhances the visibility of many types of vertical fine detail, including detail in pictorial images containing no text.

[0184] The preceding eight embodiments have received a progressively scanned video signal input a

frame at a time, but the invention can be adapted to reduce flicker in other types of video signals. For example, the input signal may be an interlaced video signal that was originally progressively scanned, but has been converted from progressive to interlaced scanning without flicker reduction, then transmitted over a communication channel or stored on a recording medium. This type of interlaced video signal can be converted back to progressive scanning by a field-frame conversion circuit employing a memory device, then supplied to the deflickering circuit of one of the preceding embodiments to remove flicker.

[0185] FIGs. 35 and 36 show two examples of field-frame conversion circuits.

[0186] In FIG. 35, an interlaced video signal is received, a field at a time, at an input terminal 310 and stored in a frame memory 312, from which a progressively scanned video signal is output at an output terminal 314. A sync separation circuit (not visible) separates synchronizing signals from the input video signal, identifies even and odd fields, and controls the addresses at which successive scanning lines are stored in the frame memory 312 in such a way as to convert the video signal from an interlaced structure to a progressively scanned structure. The resulting progressively scanned video signal is supplied from output terminal 314 to one of the embodiments described above, for deflickering and re-conversion from progressive scanning to interlaced scanning.

[0187] In FIG. 36, the interlaced video signal is received at an input terminal 310, temporarily stored in a field memory 316, supplied without delay from input terminal 310 to a first output terminal 318, and supplied with a delay of one field from field memory 316 to a second output terminal 320. The signals obtained at output terminals 318 and 320 are combined into a progressively scanned signal by, for example, a vertical low-pass filtering process that takes a weighted average of the values of a pixel in the current field and the two vertically adjacent pixels in the preceding field. The resulting progressively scanned video signal is then supplied to one of the embodiments described above, for deflickering and re-conversion to interlaced scanning.

[0188] In this way the invention can be employed to reduce the flicker resulting from scan conversion, without unnecessary loss of vertical resolution, even after scan conversion has already taken place.

[0189] More generally, the invention can be used to reduce flicker present in an interlaced video signal, without unnecessary loss of vertical resolution, even if the flicker was not produced by scan conversion.

[0190] The invention is not limited to VGA-to-NTSC conversion. The invention can be used in converting any type of progressively scanned video signal to any type of interlaced video signal. Examples of other types of progressively scanned video signals include digital television broadcast signals conforming to the proposed European DVB standard, American ATV standard, or

Japanese ISDB standard, as well as computer-generated video signals of types other than VGA.

[0191] The deflickering circuits described in the preceding embodiments can be used to reduce flicker in red, green, and blue component signals, or in color difference signals, if circumstances make this desirable. If flicker is removed from the color difference signals, the operating characteristics or configurations of the deflickering circuits that process the two color difference signals may differ from the operating characteristics or configuration of the deflickering circuit 30 that processes the luminance signal, or from each other.

[0192] The matrix circuit may convert the input red, green, and blue signals to a luminance signal and two color signals (e.g. Y, U, and V), instead of to luminance and color difference signals (Y, R - Y, B - Y). Modulation of the color subcarrier may be performed before the conversion from progressive to interlaced scanning. The effect of reducing flicker in the luminance signal Y remains the same.

[0193] The filters used to separate horizontal and vertical high-frequency and low-frequency components need not have the configurations shown in FIGs. 6, 7, 13, and 17. Other types of high-pass and low-pass filters can be employed, including, for example, filters with more taps, filters with different filter configurations, finite-impulse-response (FIR) filters, infinite-impulse-response (IIR) filters, and the like. The vertical high-frequency and low-frequency signals V_H and V_L can be separated by using a high-pass filter to extract V_H and subtracting V_H from the input signal Y_{in} to obtain V_L , instead of subtracting V_L from Y to obtain V_H .

[0194] Those skilled in the art will recognize that further modifications are possible within the scope claimed below.

Claims

1. A flicker reduction apparatus for reducing flicker in an input video signal, the apparatus comprising:

vertical-high-frequency-horizontal-low-frequency component separating means for separating from the input signal components having both vertical high frequencies and horizontal low frequencies;
first amplitude limiting means for limiting the amplitude of the separated components; and
first adding means for adding the limited-amplitude components to the remaining components of the input signal.

2. A flicker reduction apparatus according to claim 1, comprising:

direct-current component detecting means for detecting a horizontal direct-current compo-

nent in the input video signal;

wherein the amplitude limit value of the first amplitude limiting means is switched according to the result of the detection of the direct-current component, output from the direct-current component detecting means.

3. A flicker reduction apparatus according to claim 1, comprising:

vertical high-frequency component separating means for separating a vertical high-frequency component from the input video signal; and direct-current component detecting means for detecting a horizontal direct-current component in the vertical high-frequency component output from the vertical high-frequency component separating means;

wherein the amplitude limit value of the first amplitude limiting means is switched according to the result of the detection of the direct-current component, output from the direct-current component detecting means.

4. A flicker reduction apparatus according to claim 2 or 3, comprising:

horizontal high-frequency component separating means for separating a horizontal high-frequency component from the input video signal;

wherein the amplitude of the horizontal high-frequency component output from the horizontal high-frequency component separating means is compared with a predetermined value, and said direct-current component detecting means is arranged such that the said direct-current component is detected when the absolute value of the amplitude of the horizontal high-frequency component is not larger than said predetermined value.

5. A flicker reduction apparatus according to claim 1, the apparatus comprising:

frequency separating means for separating vertical low-frequency and high-frequency components from the input video signal; direct-current component detecting means for detecting a horizontal low-frequency component from the input video signal; second amplitude limiting means for limiting the amplitude of the vertical high-frequency component output from the frequency separating means; and adding means for adding the vertical low-frequency component output from the frequency

separating means and the output of the amplitude limiting means;

wherein control is so exercised that the amplitude limit value of the second amplitude limiting means is switched according to the result of the detection of the direct-current component, output from the direct-current component detecting means.

6. A flicker reduction apparatus according to claim 5, wherein said direct-current component detecting means is arranged such that when the horizontal direct-current component in the input video signal is detected, the horizontal direct-current component in the vertical high-frequency component output from the frequency separating means is detected.
7. A flicker reduction apparatus according to claim 5, comprising:

horizontal high-frequency component separating means for separating a horizontal high-frequency component from the input video signal;

wherein the amplitude of the horizontal high-frequency component output from the horizontal high-frequency component separating means is compared with a predetermined value, and said direct-current component detecting means is arranged such that when the absolute value of the amplitude is not more than the predetermined value, said direct-current component is detected.

8. A flicker reduction apparatus according to claim 1, the apparatus comprising:

frequency separating means for separating vertical high-frequency and low-frequency components from the input video signal; horizontal low-frequency component suppressing means for suppressing a horizontal low-frequency component of the vertical high-frequency component output from the frequency separating means; amplitude converting means for converting the amplitude of the vertical-high-frequency-horizontal-high-frequency component output from the horizontal low-frequency component suppressing means; and second adding means for adding the vertical low-frequency component output from the frequency separating means and the output of the amplitude converting means.

9. A flicker reduction apparatus according to claim 1, the apparatus comprising:

first frequency separating means for separating

vertical high-frequency and low-frequency components from the input video signal;
second frequency separating means for separating vertical-high-frequency-horizontal-high-frequency and vertical-high-frequency-horiz-
ontal-low-frequency components from the
vertical high-frequency component of the input
video signal;

direct-current component detecting means for
detecting a horizontal direct-current compo-
nent from the input video signal;

amplitude converting means for converting the
amplitude of the vertical-high-frequency-horiz-
ontal-low-frequency based on the output of
the direct-current component detecting means;

and

second adding means for adding the vertical
low-frequency component separated by said
first frequency separating means, the vertical-
high-frequency-horizontal-high-frequency
component separated by said second frequen-
cy separating means, and the output of said
amplitude converting means,

wherein when the amplitude of the vertical-
high-frequency-horizontal-low-frequency compo-
nent is converted at the amplitude converting
means, if the direct-current component is detected
by said direct-current component detecting means,
a reverse characteristic of the vertical-high-fre-
quency-horizontal-low-frequency is given.

10. A flicker reduction apparatus according to claim 9,
wherein when the horizontal direct-current compo-
nent in the input video signal is detected, the ampli-
tude of the vertical-high-frequency-horizontal-high-
frequency component separated at the second fre-
quency separating means is compared with a pre-
determined value, and said direct-current compo-
nent detecting means is so arranged that when the
amplitude is less than the predetermined value,
said direct-current component is detected.

11. A flicker reduction apparatus according to claim 1,
the apparatus comprising:

frequency separating means for separating
vertical high-frequency and low-frequency
components from the input video signal;
direct-current component detecting means for
detecting a horizontal direct-current compo-
nent from the input video signal;
amplitude converting means for converting the
amplitude of the vertical high-frequency compo-
nent based on the output of the direct-current
component detecting means;
second adding means for adding the vertical
low-frequency component separated by said

frequency separating means, and the output of
said amplitude converting means,

wherein when the amplitude of the vertical
high-frequency component is converted at the am-
plitude converting means, if the direct-current com-
ponent is detected by said direct-current compo-
nent detecting means, a reverse characteristics of
the vertical high-frequency is given.

12. A flicker reduction apparatus according to claim 1,
wherein the input video signal is an interlaced video
signal received a field at a time, the apparatus com-
prising:

a field-frame conversion circuit for temporarily
storing said interlaced video signal, converting
said interlaced video signal to a progressively
scanned video signal, and outputting said pro-
gressively scanned video signal a frame at a
time.

13. A flicker reduction apparatus according to claim 1,
wherein a memory is used to generate a progres-
sively scanned video signal.

Patentansprüche

1. Flimmerreduktionsvorrichtung zum Reduzieren des
Flimmerns in einem Eingangsvideosignal, welche
Vorrichtung aufweist:

eine Vertikalhochfrequenz/Horizontalniedrig-
frequenz-Komponenten-Trennvorrichtung zum
Trennen von Komponenten mit sowohl vertikalen
Hochfrequenzen als auch horizontalen
Niedrigfrequenzen von dem Eingangssignal;
eine erste Amplitudenbegrenzungsvorrichtung
zum Begrenzen der Amplitude der getrennten
Komponenten; und
eine erste Additionsvorrichtung zum Hinzufü-
gen der in der Amplitude begrenzten Kompo-
nenten zu den verbleibenden Komponenten
des Eingangssignals.

2. Flimmerreduktionsvorrichtung nach Anspruch 1,
welche aufweist:

eine Gleichstromkomponenten-Erfassungs-
vorrichtung zum Erfassen einer horizontalen
Gleichstromkomponente in dem Eingangsvi-
deosignal;

worin der Amplitudengrenzwert der ersten Amplitu-
denbegrenzungsvorrichtung umgeschaltet wird
entsprechend dem Ergebnis der Erfassung der
Gleichstromkomponente, das von der Gleichstrom-

komponenten-Erfassungsvorrichtung ausgegeben wird.

3. Flimmerreduktionsvorrichtung nach Anspruch 1, welche aufweist:

5

eine Vertikalhochfrequenz-Komponententrennvorrichtung zum Trennen einer vertikalen Hochfrequenzkomponente von dem eingegebenen Videosignal; und

10

eine Gleichstromkomponenten-Erfassungsvorrichtung zum Erfassen einer horizontalen Gleichstromkomponente in der vertikalen Hochfrequenzkomponente, die von der Vertikalhochfrequenz-Komponententrennvorrichtung ausgegeben wurde;

15

worin der Amplitudengrenzwert der ersten Amplitudenbegrenzungsvorrichtung umgeschaltet wird entsprechend dem Ergebnis der Erfassung der Gleichstromkomponente, das von der Gleichstromkomponenten-Erfassungsvorrichtung ausgegeben wurde.

20

4. Flimmerreduktionsvorrichtung nach Anspruch 2 oder 3, welche aufweist:

25

eine Horizontalhochfrequenz-Komponententrennvorrichtung zum Trennen einer horizontalen Hochfrequenzkomponente von dem Eingangsvideosignal;

30

worin die Amplitude der horizontalen Hochfrequenzkomponente, die von der Horizontalhochfrequenz-Komponententrennvorrichtung ausgegeben wurde, mit einem vorbestimmten Wert verglichen wird, und die Gleichstromkomponenten-Erfassungsvorrichtung so ausgebildet ist, dass die Gleichstromkomponente erfasst wird, wenn der absolute Wert der Amplitude der horizontalen Hochfrequenzkomponente nicht größer als der vorbestimmte Wert ist.

35

40

5. Flimmerreduktionsvorrichtung nach Anspruch 1, welche Vorrichtung aufweist:

45

eine Frequenztrennvorrichtung zum Trennen von vertikalen Niederfrequenz- und Hochfrequenzkomponenten von dem Eingangsvideosignal;

50

eine Gleichstromkomponenten-Erfassungsvorrichtung zum Erfassen einer horizontalen Niederfrequenzkomponente in dem Eingangsvideosignal; eine zweite Amplitudenbegrenzungsvorrichtung zum Begrenzen der Amplitude der vertikalen Hochfrequenzkomponente, die von der Frequenztrennvorrichtung ausgegeben wurde; und

55

eine Additionsvorrichtung zum Hinzufügen der vertikalen Niederfrequenzkomponente, die von der Frequenztrennvorrichtung ausgegeben wurde, zu dem Ausgangssignal der Amplitudenbegrenzungsvorrichtung;

worin die Steuerung so durchgeführt wird, dass der Amplitudengrenzwert der zweiten Amplitudenbegrenzungsvorrichtung umgeschaltet wird entsprechend dem Ergebnis der Erfassung der Gleichstromkomponente, das von der Gleichstromkomponenten-Erfassungsvorrichtung ausgegeben wurde.

6. Flimmerreduktionsvorrichtung nach Anspruch 5, bei der die Gleichstromkomponenten-Erfassungsvorrichtung so ausgebildet ist, dass, wenn die horizontale Gleichstromkomponente in dem Eingangsvideosignal erfasst wird, die horizontale Gleichstromkomponente in der vertikalen Hochfrequenzkomponente, die von der Frequenztrennvorrichtung ausgegeben wurde, erfasst wird.

7. Flimmerreduktionsvorrichtung nach Anspruch 5, welche aufweist:

eine Horizontalhochfrequenz-Komponententrennvorrichtung zum Trennen einer horizontalen Hochfrequenzkomponente von dem Eingangsvideosignal;

worin die Amplitude der horizontalen Hochfrequenzkomponente, die von der Horizontalhochfrequenz-Komponententrennvorrichtung ausgegeben wurde, mit einem vorbestimmten Wert verglichen wird, und die Gleichstromkomponenten-Erfassungsvorrichtung so ausgebildet ist, dass, wenn der absolute Wert der Amplitude nicht mehr als der vorbestimmte Wert ist, die Gleichkomponente erfasst wird.

8. Flimmerreduktionsvorrichtung nach Anspruch 1, welche Vorrichtung aufweist:

eine Frequenztrennvorrichtung zum Trennen von vertikalen Hochfrequenz- und Niederfrequenzkomponenten von dem Eingangsvideosignal;

eine Horizontalniederfrequenz-Komponentenunterdrückungsvorrichtung zum Unterdrücken einer horizontalen Niederfrequenzkomponente der vertikalen Hochfrequenzkomponente, die von der Frequenztrennvorrichtung ausgegeben wurde;

eine Amplitudenumwandlungsvorrichtung zum Umwandeln der Amplitude der Vertikalhochfrequenz-/Horizontalhochfrequenz-Komponente, die von der Horizontalniederfrequenz-Komponentenunterdrückungsvorrichtung ausgegeben

ben wurde; und
eine zweite Additionsvorrichtung zum Hinzufügen der vertikalen Niedrigfrequenzkomponente, die von der Frequenztrennvorrichtung ausgegeben wurde, zu dem Ausgangssignal der Amplitudenumwandlungsvorrichtung.

9. Flimmerreduktionsvorrichtung nach Anspruch 1, welche Vorrichtung aufweist:

eine erste Frequenztrennvorrichtung zum Trennen von vertikalen Hochfrequenz- und Niedrigfrequenzkomponenten von dem Eingangsvideosignal; eine zweite Frequenztrennvorrichtung zum Trennen von Vertikalhochfrequenz/Horizontalhochfrequenz- und Vertikalhochfrequenz/Horizontalniedrigfrequenz-Komponenten von der vertikalen Hochfrequenzkomponente des Eingangsvideosignals; eine Gleichstromkomponenten-Erfassungsvorrichtung zum Erfassen einer horizontalen Gleichstromkomponente in dem Eingangsvideosignal;
eine Amplitudenumwandlungsvorrichtung zum Umwandeln der Amplitude der Vertikalhochfrequenz /Horizontalniedrigfrequenz auf der Grundlage des Ausgangssignals der Gleichstromkomponenten-Erfassungsvorrichtung; und
eine zweite Additionsvorrichtung zum Überlagern der vertikalen Niedrigfrequenzkomponente, die von der ersten Frequenztrennvorrichtung getrennt wurde, der Vertikalhochfrequenz/Horizontalhochfrequenz-Komponente, die von der zweiten Frequenztrennvorrichtung getrennt wurde, und des Ausgangssignals der Amplitudenumwandlungsvorrichtung;

worin, wenn die Amplitude der Vertikalhochfrequenz/Horizontalniedrigfrequenz-Komponente in der Amplitudenumwandlungsvorrichtung umgewandelt wird, wenn die Gleichstromkomponente von der Gleichstromkomponenten-Erfassungsvorrichtung erfasst wird, eine umgekehrte Charakteristik der Vertikalhochfrequenz/Horizontalniedrigfrequenz gegeben wird.

10. Flimmerreduktionsvorrichtung nach Anspruch 9, worin, wenn die horizontale Gleichstromkomponente in dem Eingangsvideosignal erfasst wird, die Amplitude der Vertikalhochfrequenz/Horizontalhochfrequenz-Komponente, die von der zweiten Frequenztrennvorrichtung getrennt wurde, mit einem vorbestimmten Wert verglichen wird, und die Gleichstromkomponenten-Erfassungsvorrichtung so ausgebildet ist, dass, wenn die Amplitude geringer als der vorbestimmte Wert ist, die Gleichstromkomponente erfasst wird.

11. Flimmerreduktionsvorrichtung nach Anspruch 1, welche Vorrichtung aufweist:

eine Frequenztrennvorrichtung zum Trennen von vertikalen Hochfrequenz- und Niedrigfrequenzkomponenten von dem Eingangsvideosignal;
eine Gleichstromkomponenten-Erfassungsvorrichtung zum Erfassen einer horizontalen Gleichstromkomponente in dem Eingangsvideosignal;
eine Amplitudenumwandlungsvorrichtung zum Umwandeln der Amplitude der vertikalen Hochfrequenzkomponente auf der Grundlage des Ausgangssignals der Gleichstromkomponenten-Erfassungsvorrichtung;
eine zweite Additionsvorrichtung zum Hinzufügen der vertikalen Niedrigfrequenzkomponente, die von der Frequenztrennvorrichtung getrennt wurde, zu dem Ausgangssignals der Amplitudenumwandlungsvorrichtung;

worin, wenn die Amplitude der vertikalen Hochfrequenzkomponente in der Amplitudenumwandlungsvorrichtung umgewandelt wird, wenn die Gleichstromkomponente von der Gleichstromkomponenten-Erfassungsvorrichtung erfasst wird, eine umgekehrte Charakteristik der Vertikalhochfrequenz gegeben wird.

12. Flimmerreduktionsvorrichtung nach Anspruch 1, worin das Eingangsvideosignal ein verschachteltes Videosignal ist, das gleichzeitig als Halbbild empfangen wird, welche Vorrichtung aufweist:

eine Halbbild/Vollbild-Umwandlungsschaltung zum vorübergehenden Speichern des verschachtelten Videosignals, Umwandeln des verschachtelten Videosignals in ein fortschreitend abgetastetes Videosignal, und Ausgeben des fortschreitend abgetasteten Videosignals gleichzeitig als ein Vollbild.

13. Flimmerreduktionsvorrichtung nach Anspruch 1, worin ein Speicher verwendet wird, um ein fortschreitend abgetastetes Videosignal zu erzeugen.

Revendications

1. Dispositif de réduction de papillotement pour réduire le papillotement dans un signal vidéo d'entrée, le dispositif comprenant:

des moyens de séparation de la composante verticale à haute fréquence et de la composante horizontale à basse fréquence pour réaliser une séparation à partir des composantes du si-

- gnal d'entrée possédant à la fois des fréquences verticales élevées et des basses fréquences horizontales;
des premiers moyens de limitation d'amplitude pour limiter l'amplitude des composantes séparées; et
des premiers moyens d'addition pour additionner les composantes limitées en amplitude aux autres composantes du signal d'entrée.
2. Dispositif de réduction de papillotement selon la revendication 1, comprenant:
- des moyens de détection de la composante de courant continu pour détecter une composante horizontale de courant continu dans le signal vidéo d'entrée; et
- dans lequel la valeur limite de l'amplitude des premiers moyens de limitation d'amplitude est commutée en fonction du résultat de la détection de la composante de courant continu, délivrée par les moyens de détection de la composante de courant continu.
3. Dispositif de réduction de papillotement selon la revendication 1, comprenant:
- des moyens de séparation de la composante verticale à haute fréquence pour séparer une composante verticale à haute fréquence, du signal vidéo d'entrée; et
des moyens de détection de la composante de courant continu pour détecter une composante horizontale de courant continu dans la composante verticale à haute fréquence délivrée par les moyens de séparation de la composante verticale à haute fréquence;
- dans lequel la valeur limite de l'amplitude du premier moyen de limitation d'amplitude est commutée en fonction du résultat de la détection de la composante de courant continu, délivré par les moyens de détection de la composante de courant continu.
4. Dispositif de réduction du papillotement selon la revendication 2 ou 3, comprenant:
- des moyens de séparation de la composante horizontale à haute fréquence pour séparer une composante horizontale à haute fréquence à partir du signal vidéo d'entrée;
- dans lequel l'amplitude de la composante horizontale à haute fréquence délivrée par les moyens de séparation de la composante horizontale à haute fréquence est comparée à une valeur prédéterminée, et lesdits moyens de détection de la composante de courant continu sont agencés de telle sorte que ladite composante à courant continu est détectée lorsque la valeur absolue de l'amplitude de la composante horizontale à haute fréquence n'est pas supérieure à ladite valeur prédéterminée.
5. Dispositif de réduction de papillotement selon la revendication 1, le dispositif comprenant:
- des moyens de séparation de fréquence, pour séparer les composantes verticales à basse fréquence et à haute fréquence, du signal vidéo d'entrée;
des moyens de détection de la composante de courant continu pour détecter une composante horizontale à basse fréquence, à partir du signal vidéo d'entrée;
des seconds moyens de limitation d'amplitude pour limiter l'amplitude de la composante verticale à haute fréquence délivrée par les moyens de séparation de fréquence; et
des moyens d'addition pour additionner la composante verticale à basse fréquence délivrée par les moyens de séparation de fréquence et le signal de sortie des moyens de limitation d'amplitude;
- dans lequel une commande est réalisée de telle sorte que la valeur limite de l'amplitude des seconds moyens de limitation d'amplitude est commutée conformément au résultat de la détection de la composante de courant continu, délivré par les moyens de détection de la composante de courant continu.
6. Dispositif de réduction de papillotement selon la revendication 5, dans lequel lesdits moyens de détection de la composante de courant continu sont agencés de telle sorte que, lorsque la composante horizontale de courant continu dans le signal vidéo d'entrée est détectée, la composante horizontale de courant continu dans la composante verticale à haute fréquence délivrée par les moyens de séparation de fréquence est détectée.
7. Dispositif de réduction de papillotement selon la revendication 5, comprenant:
- des moyens de séparation de la composante horizontale à haute fréquence pour séparer une composante horizontale à haute fréquence du signal vidéo d'entrée;
- dans lequel l'amplitude de la composante horizontale à haute fréquence délivrée par les moyens de séparation de la composante horizontale à haute fréquence est comparée à une valeur prédéterminée.

née, et lesdits moyens de détection de la composante de courant continu sont agencés de telle sorte que, lorsque la valeur absolue de l'amplitude n'est pas supérieure à la valeur prédéterminée, ladite composante de courant continu est détectée.

5

8. Dispositif de réduction de papillotement selon la revendication 1, le dispositif comprenant:

ces moyens de séparation de fréquence pour séparer les composantes verticales à haute fréquence et à basse fréquence à partir du signal vidéo d'entrée;

10

des moyens de suppression de la composante horizontale à basse fréquence pour supprimer une composante horizontale à basse fréquence de la composante verticale à haute fréquence délivrée par les moyens de séparation de fréquence;

15

des moyens de conversion d'amplitude pour convertir l'amplitude du signal de sortie de composante verticale à haute fréquence et de la composante horizontale à haute fréquence, délivré par les moyens de suppression de la composante horizontale à haute fréquence; et des seconds moyens d'addition pour additionner la composante verticale à basse fréquence délivrée par les moyens de séparation de fréquence et le signal de sortie des moyens de conversion d'amplitude.

20

25

30

9. Dispositif de réduction de papillotement selon la revendication 1, le dispositif comprenant:

des premiers moyens de séparation de fréquence pour séparer des composantes verticales à haute fréquence et à basse fréquence à partir du signal vidéo d'entrée;

35

des seconds moyens de séparation de fréquence pour séparer des composantes verticale à haute fréquence et horizontale à haute fréquence et verticale à haute fréquence et horizontale à basse fréquence à partir de la composante verticale à haute fréquence du signal vidéo d'entrée;

40

45

des moyens de détection de la composante de courant continu pour détecter une composante horizontale de courant continu à partir du signal vidéo d'entrée;

des moyens de conversion d'amplitude pour convertir l'amplitude des composantes verticale à haute fréquence et horizontale à basse fréquence sur la base du signal de sortie des moyens de détection de la composante de courant continu; et

50

des seconds moyens d'addition pour additionner la composante verticale à basse fréquence séparée par lesdits premiers moyens de sépa-

55

ration de fréquence, la composante verticale à haute fréquence et horizontale à haute fréquence séparées par lesdits seconds moyens de séparation de fréquence et le signal de sortie dudit moyen de conversion d'amplitude,

dans lequel, lorsque l'amplitude de la composante verticale à haute fréquence et horizontale à basse fréquence est convertie dans lesdits moyens de conversion d'amplitude, si la composante de courant continu est détectée par lesdits moyens de détection de la composante de courant continu, une caractéristique inverse de la composante verticale à haute fréquence et horizontale à basse fréquence est délivrée.

10. Dispositif de réduction de papillotement selon la revendication 9, dans lequel lorsque la composante horizontale de courant continu dans le signal vidéo d'entrée est détectée, l'amplitude de la composante verticale à haute fréquence et horizontale à haute fréquence, séparée dans les seconds moyens de séparation de fréquence, est comparée à une valeur prédéterminée et lesdits moyens de détection de composante de courant continu sont agencés de telle sorte que lorsque l'amplitude est inférieure à la valeur prédéterminée, ladite composante de courant continu est détectée.

11. Dispositif de réduction de papillotement selon la revendication 1, le dispositif comprenant:

des moyens de séparation de fréquence pour séparer une composante verticale à haute fréquence et une composante verticale à basse fréquence à partir du signal vidéo d'entrée;

des moyens de détection de la composante de courant continu pour détecter une composante horizontale de courant continu à partir du signal vidéo d'entrée;

des moyens de conversion d'amplitude pour convertir l'amplitude de la composante verticale à haute fréquence sur la base du signal de sortie des moyens de détection de la composante de courant continu;

des seconds moyens d'addition pour additionner la composante verticale à basse fréquence séparée par lesdits moyens de séparation de fréquence et le signal de sortie desdits moyens de conversion d'amplitude,

dans lequel, lorsque l'amplitude de la composante verticale à haute fréquence est convertie par les moyens de conversion d'amplitude, si la composante de courant continu est détectée par lesdits moyens de détection de la composante de courant continu, une caractéristique inverse de la haute fréquence verticale est obtenue.

- 12.** Dispositif de réduction de papillotement selon la revendication 1, dans lequel le signal vidéo d'entrée est un signal vidéo entrelacé reçu à raison d'une trame à la fois, le dispositif comprenant:

5

un circuit de conversion trame-image complète pour mémoriser temporairement ledit signal vidéo entrelacé, convertir ledit signal vidéo entrelacé en un signal vidéo balayé progressivement et délivrer ledit signal vidéo délivré balayé progressivement à raison d'une trame complète à la fois.

10

- 13.** Dispositif de réduction de papillotement selon la revendication 1, dans lequel une mémoire est utilisée pour générer un signal vidéo balayé progressivement.

15

20

25

30

35

40

45

50

55

FIG. 1

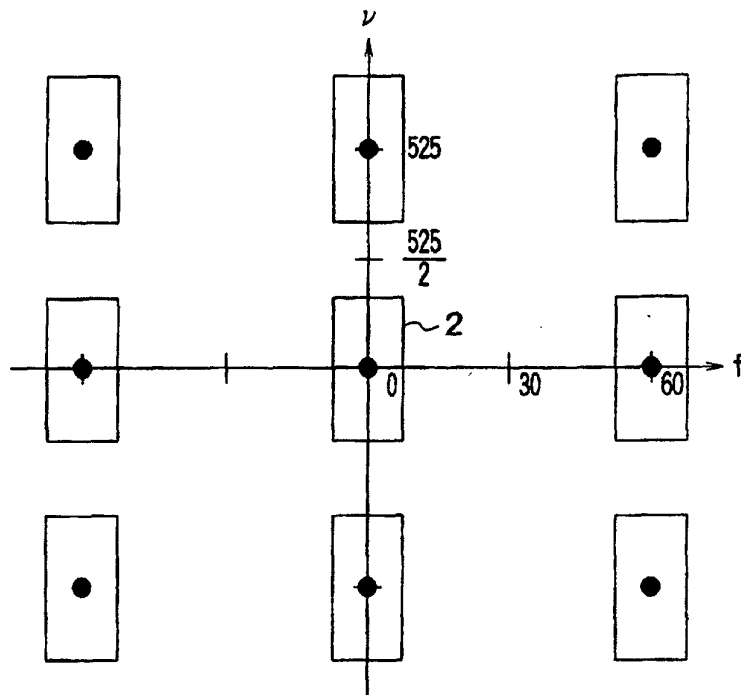


FIG. 2

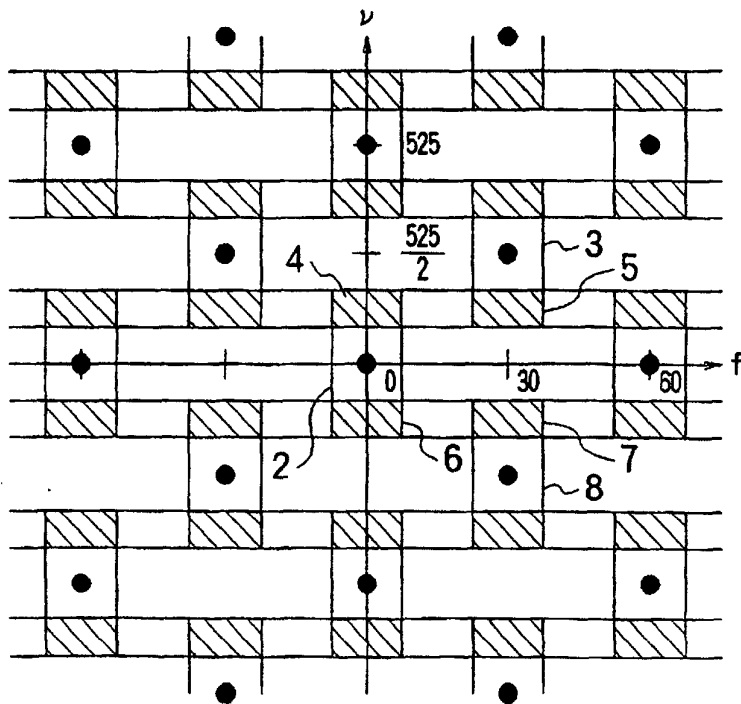


FIG. 3

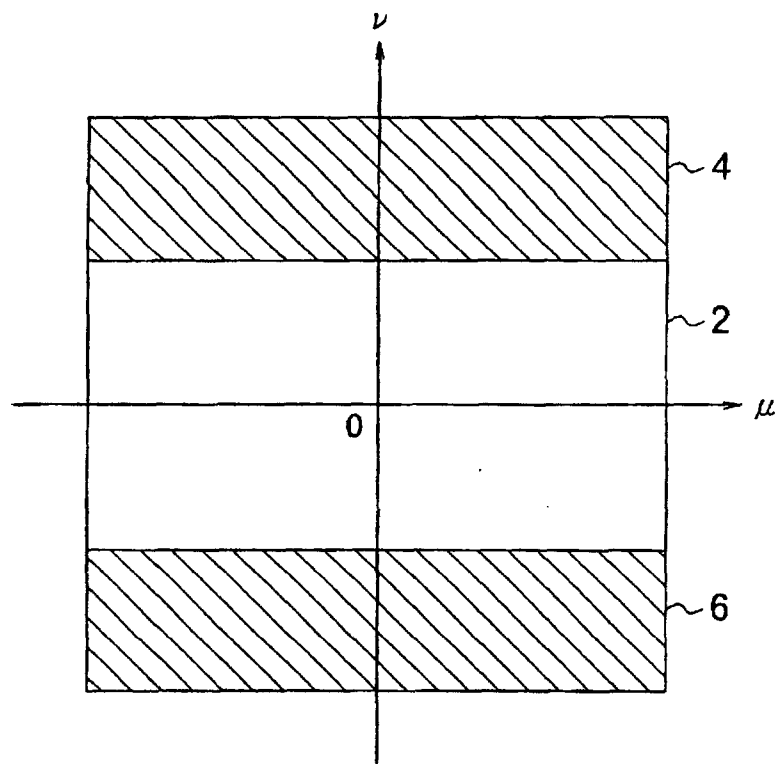


FIG. 4

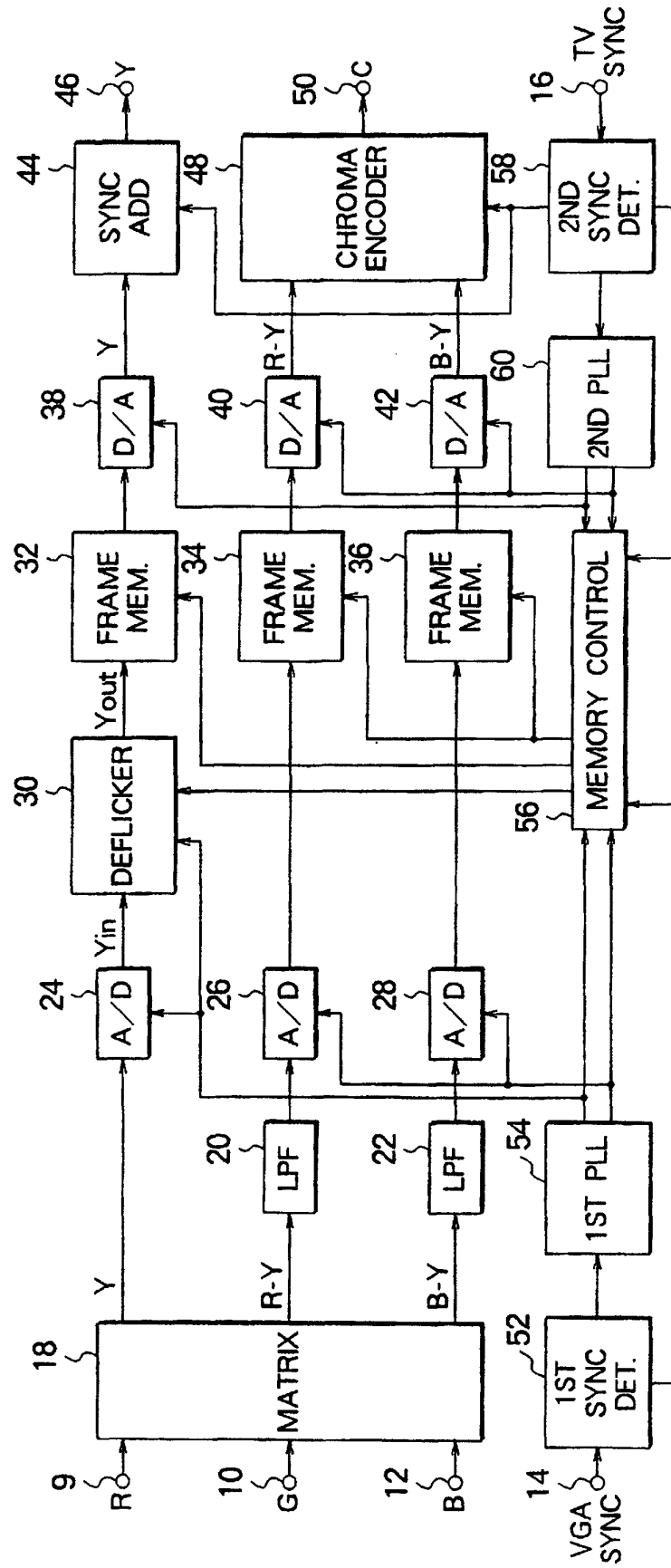


FIG. 5

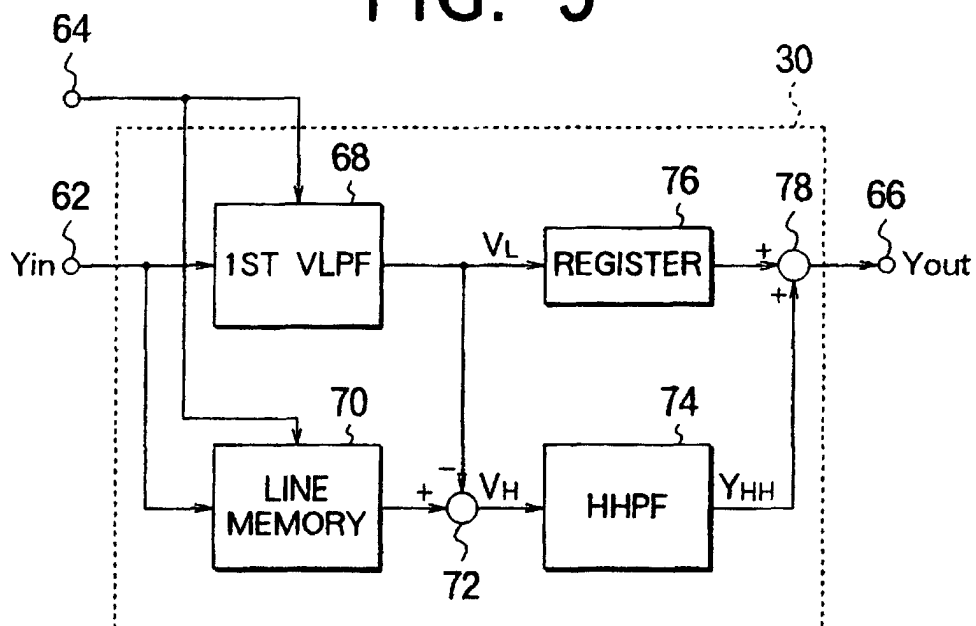


FIG. 6

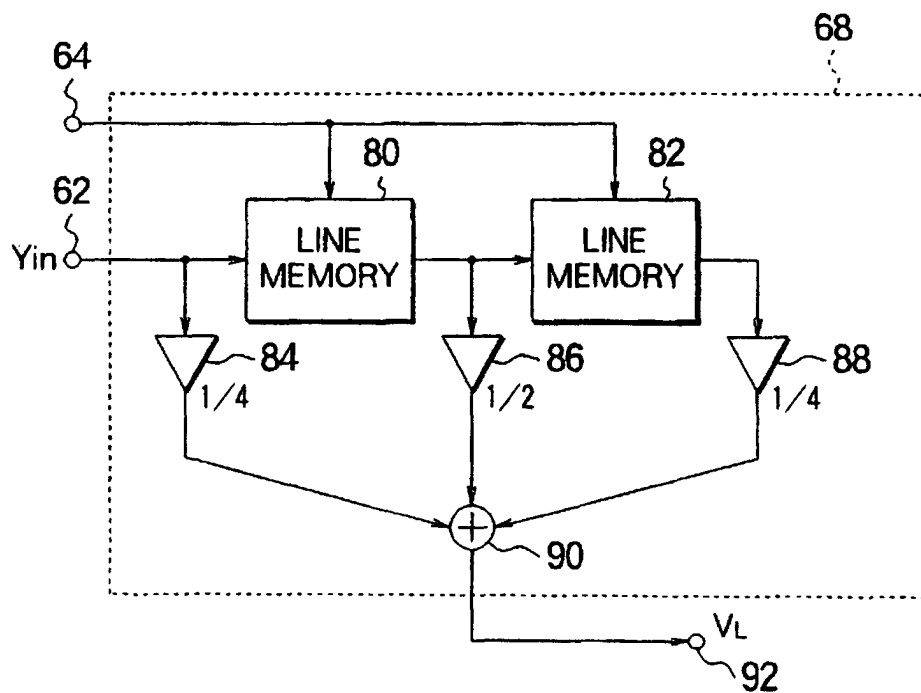


FIG. 7

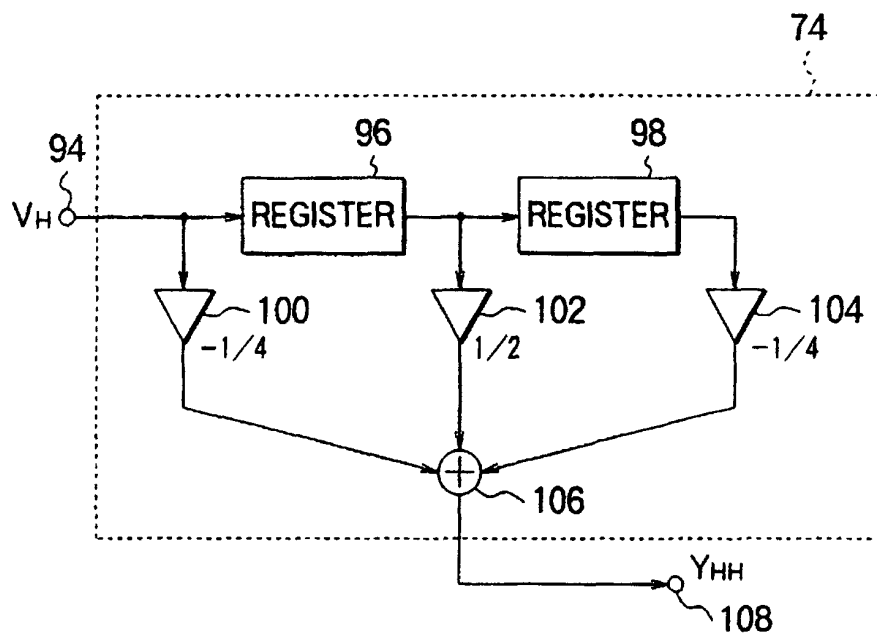


FIG. 8

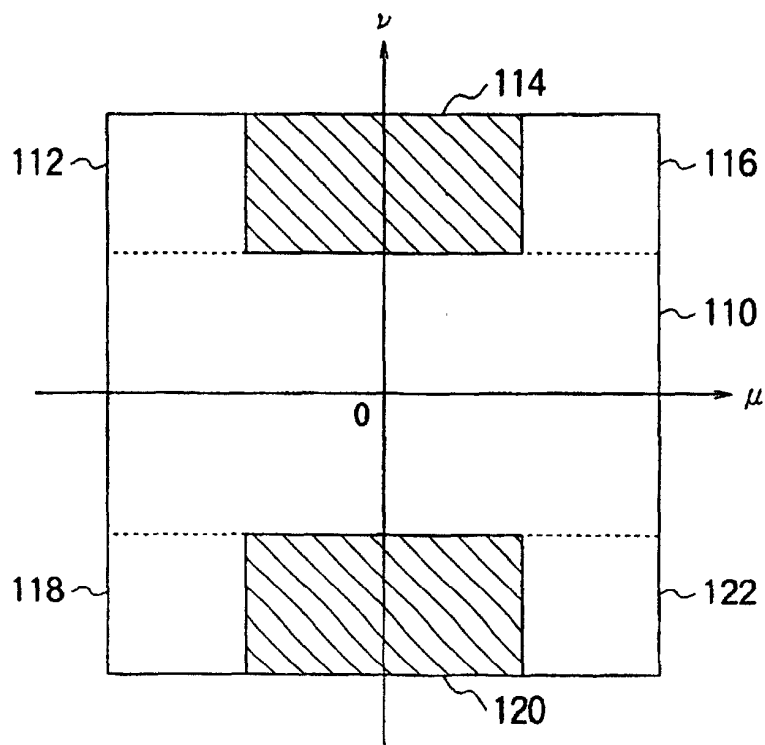


FIG. 9

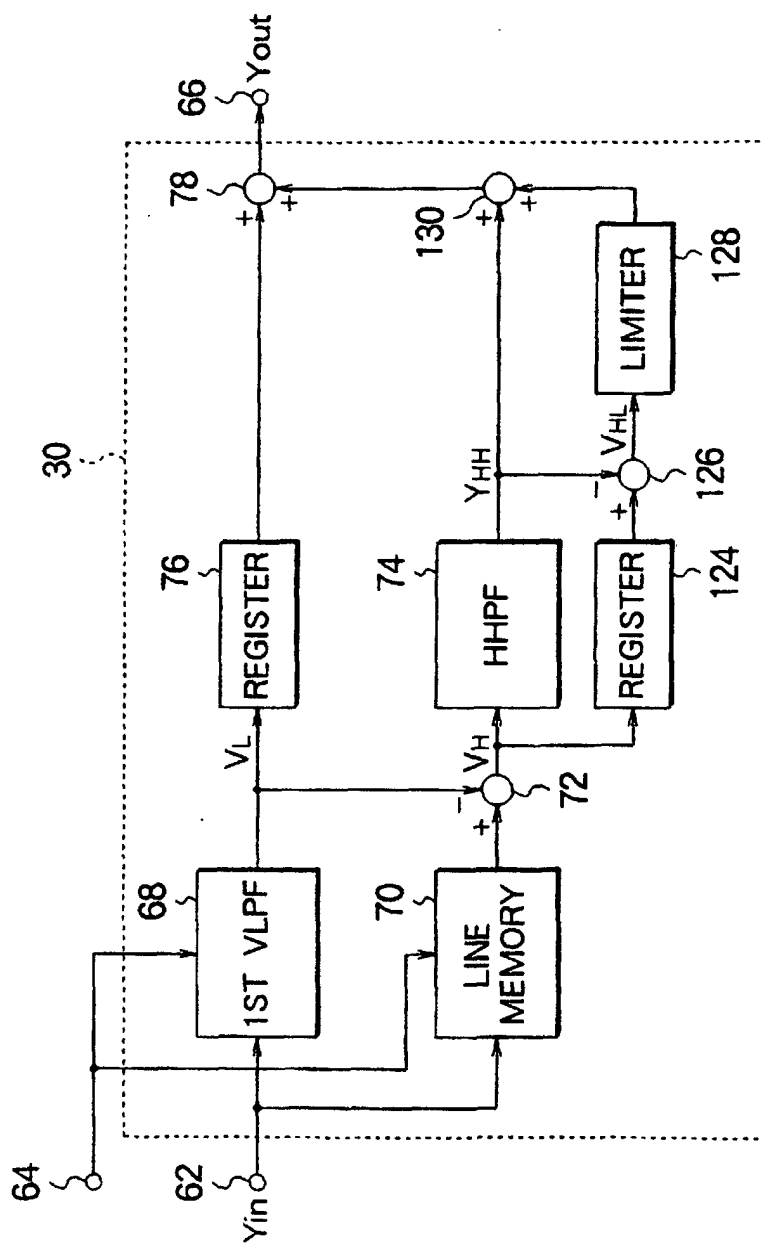


FIG. 10

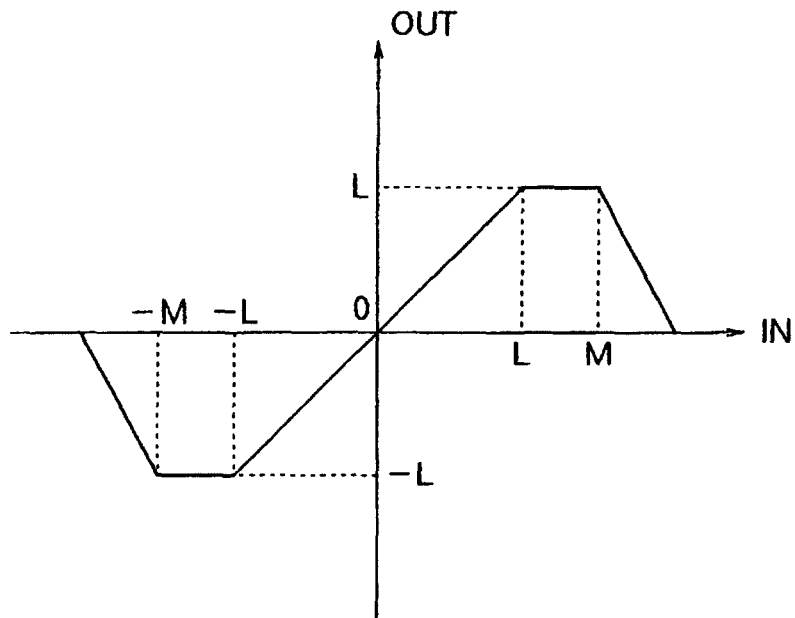


FIG. 11

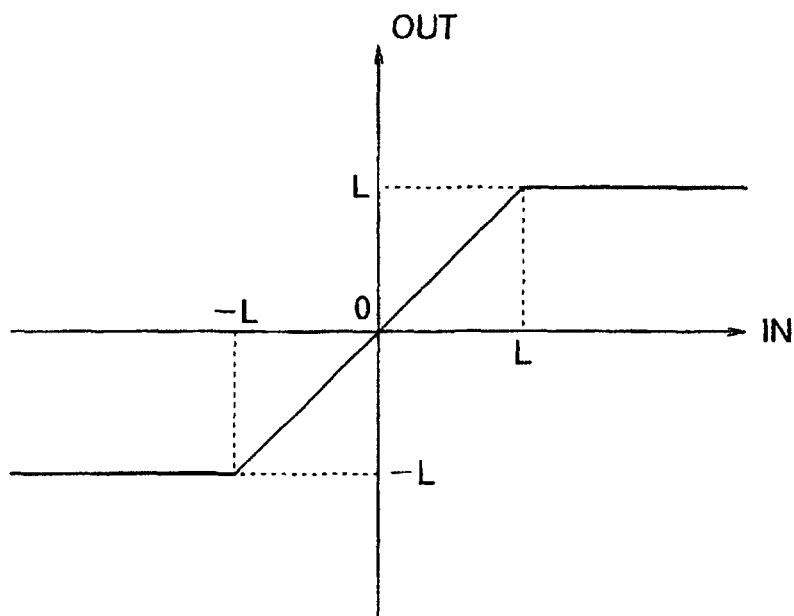


FIG. 12

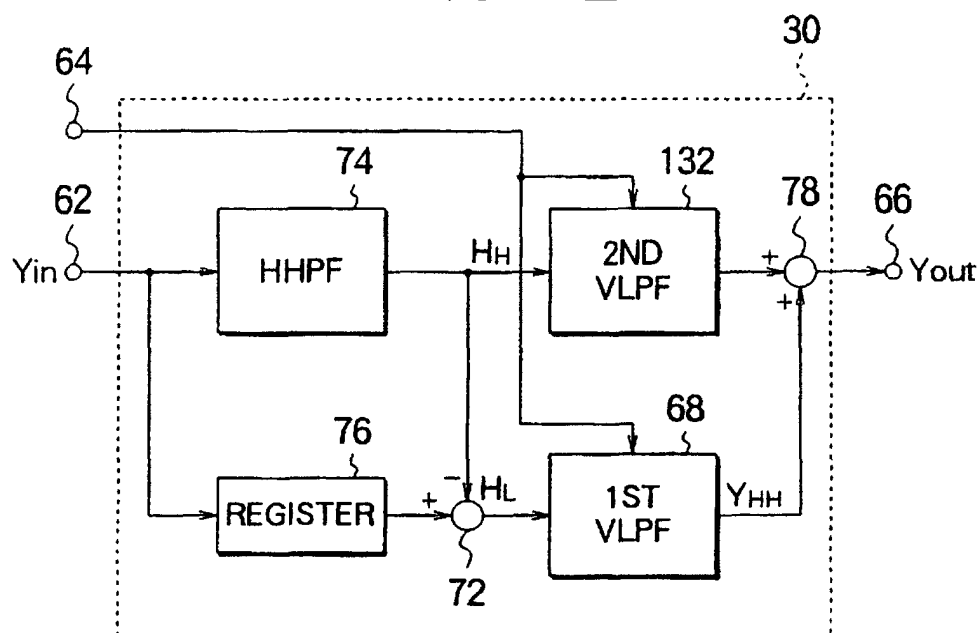


FIG. 13

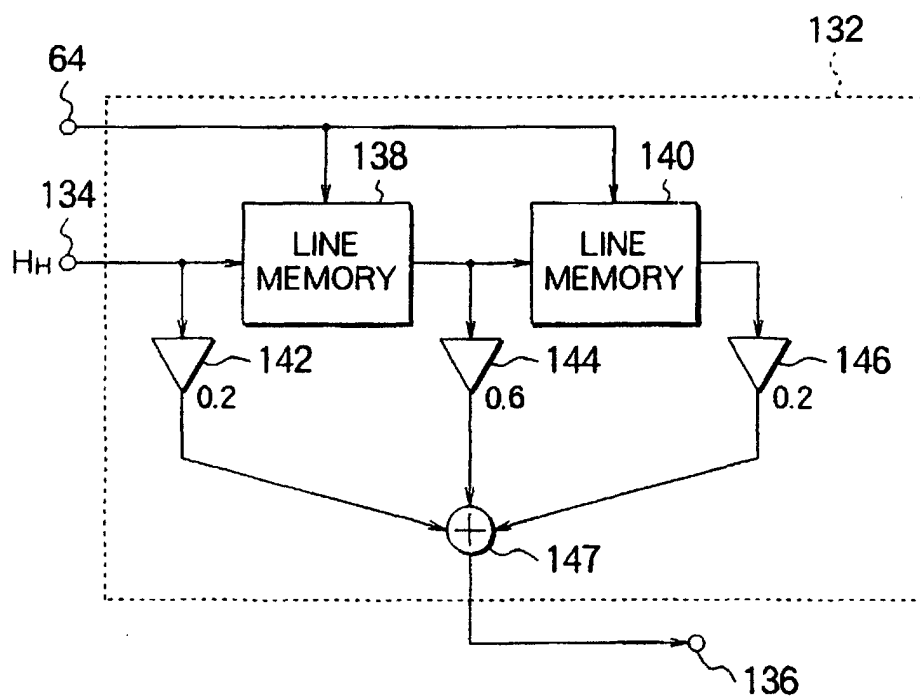


FIG. 14

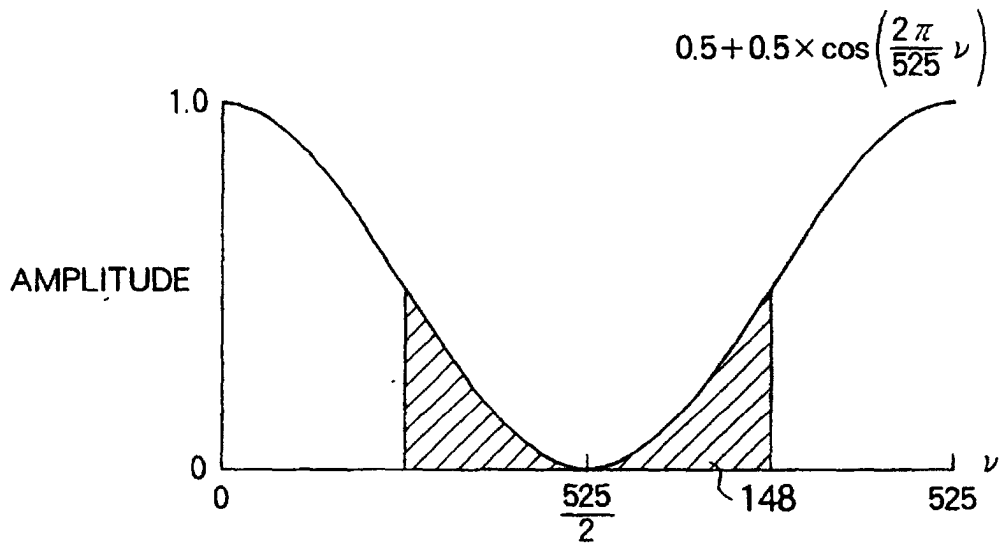


FIG. 15

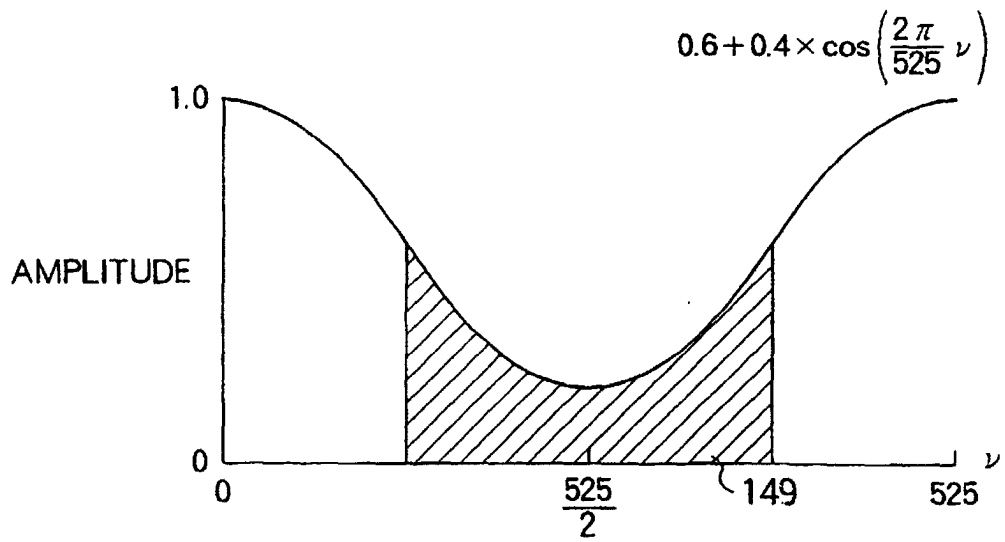


FIG. 16

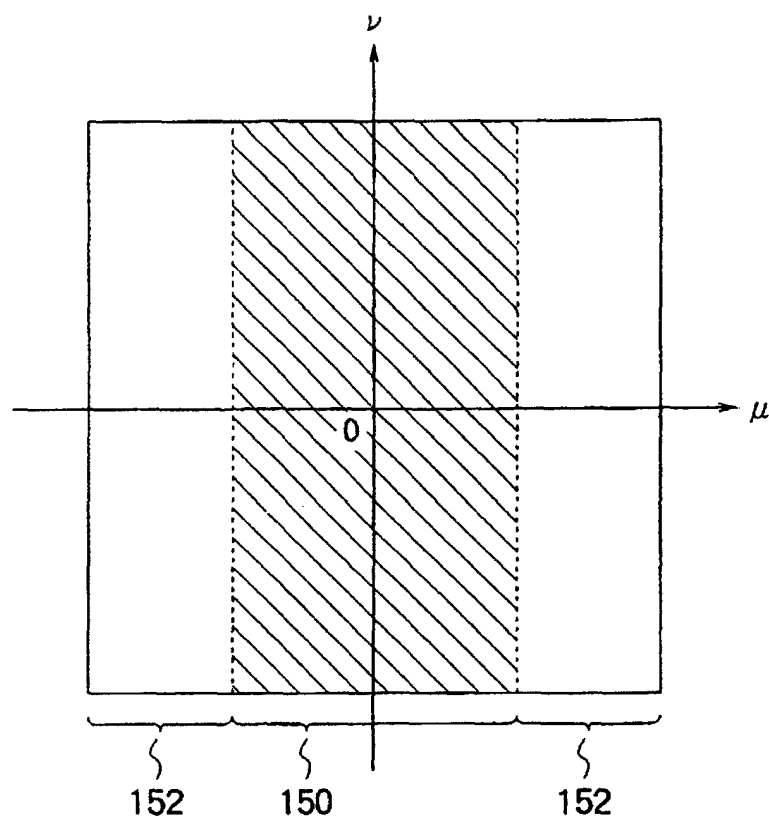


FIG. 17

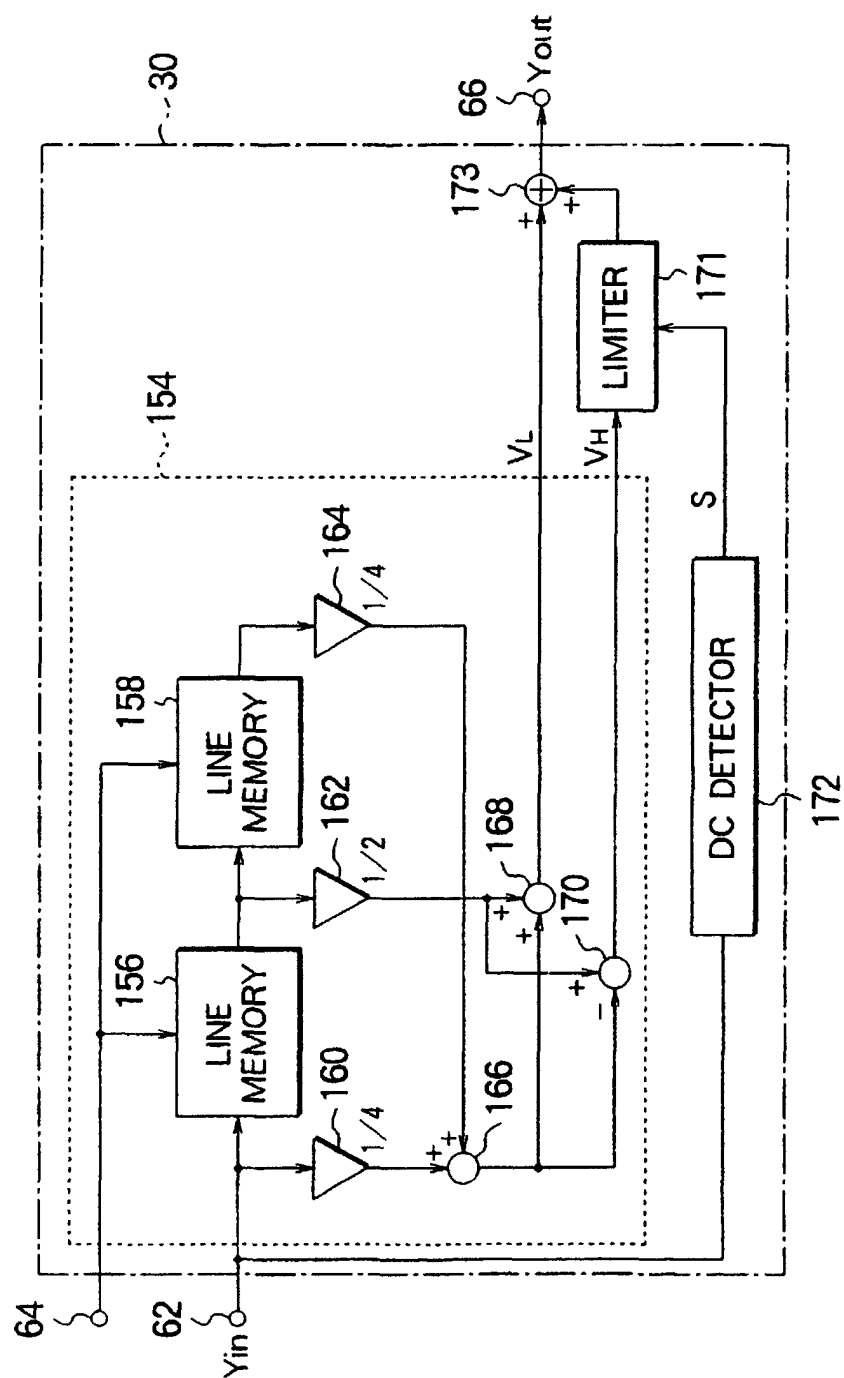


FIG. 18

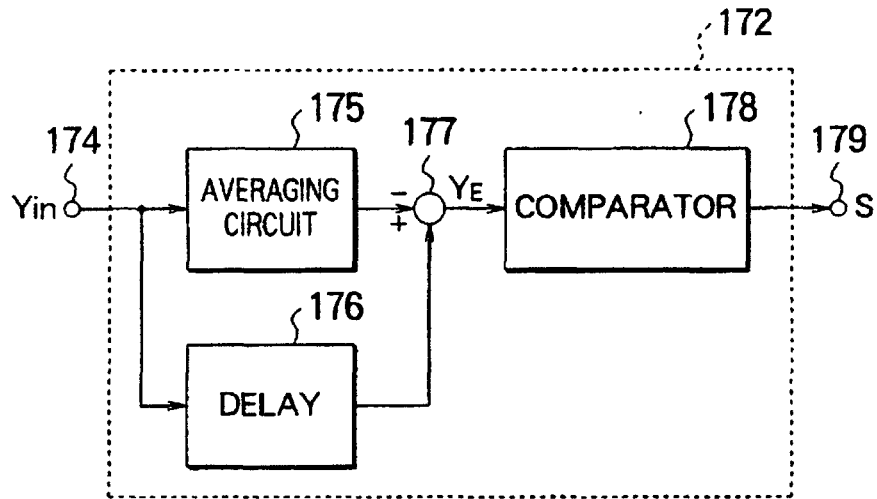


FIG. 19

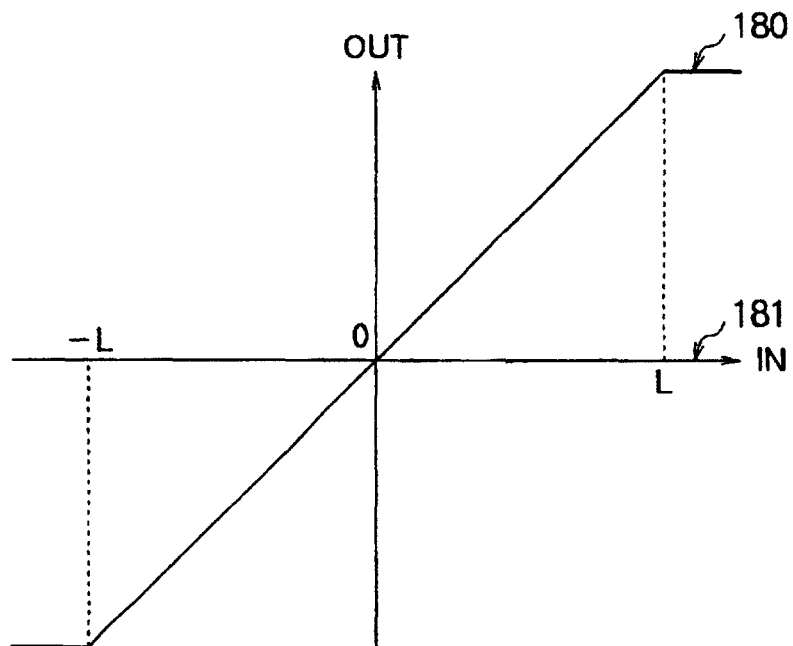


FIG. 20

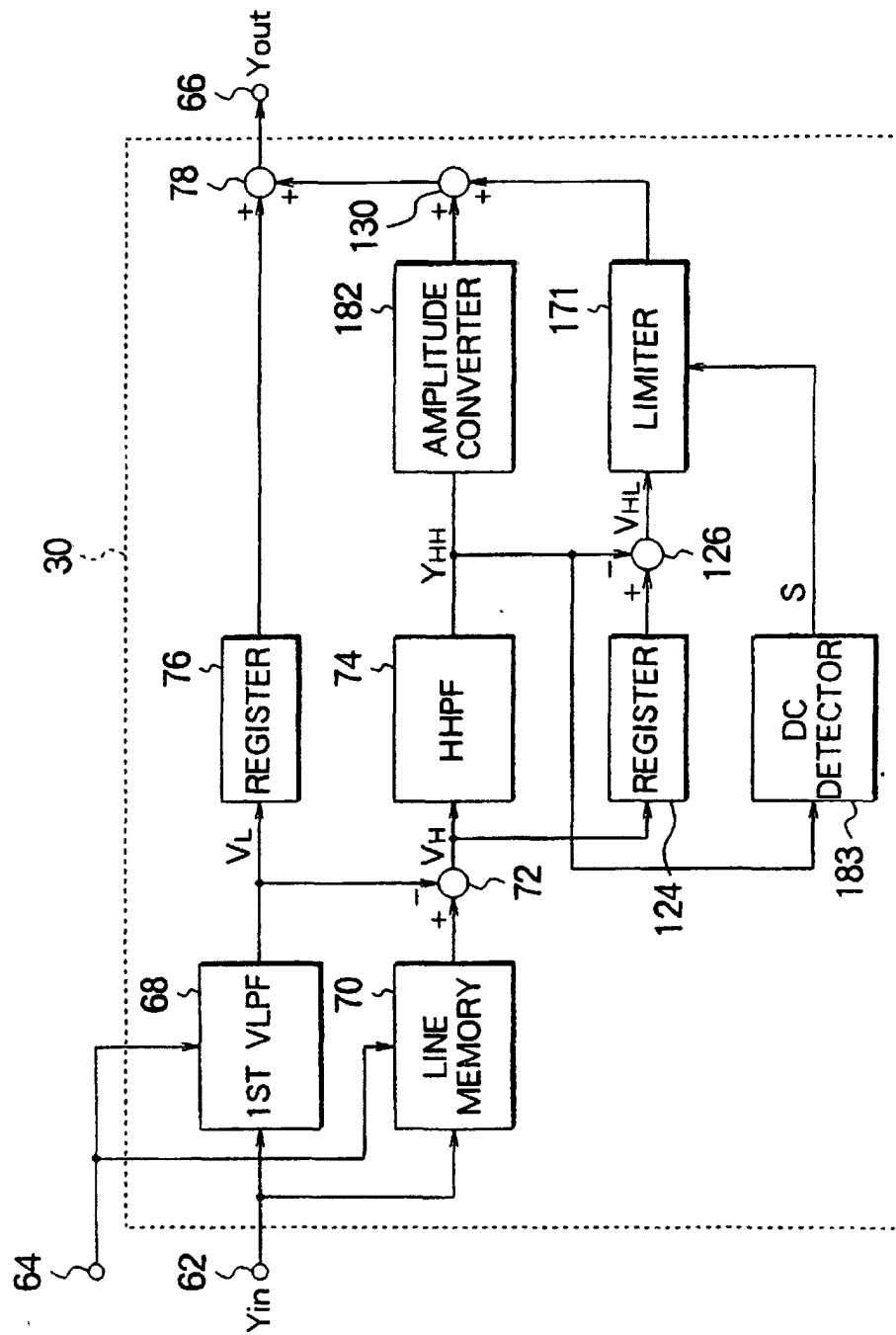


FIG. 21

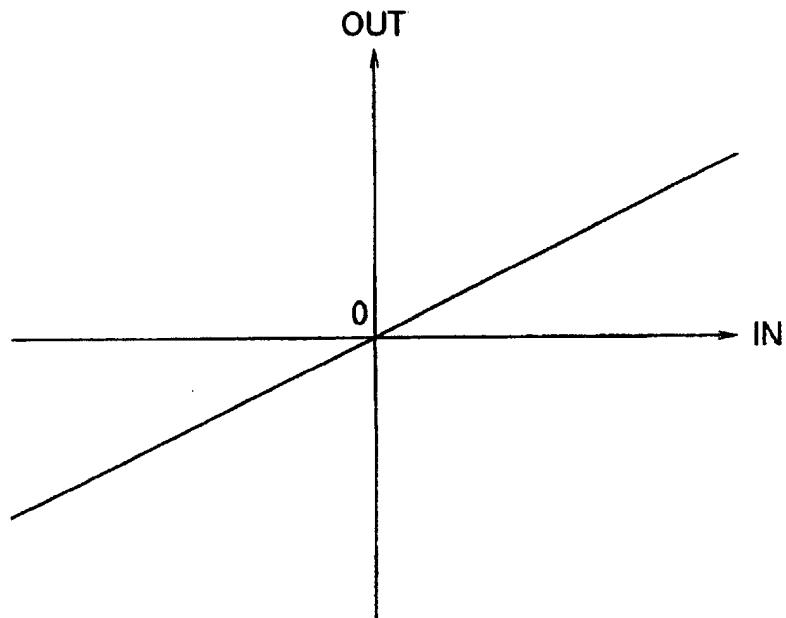


FIG. 22

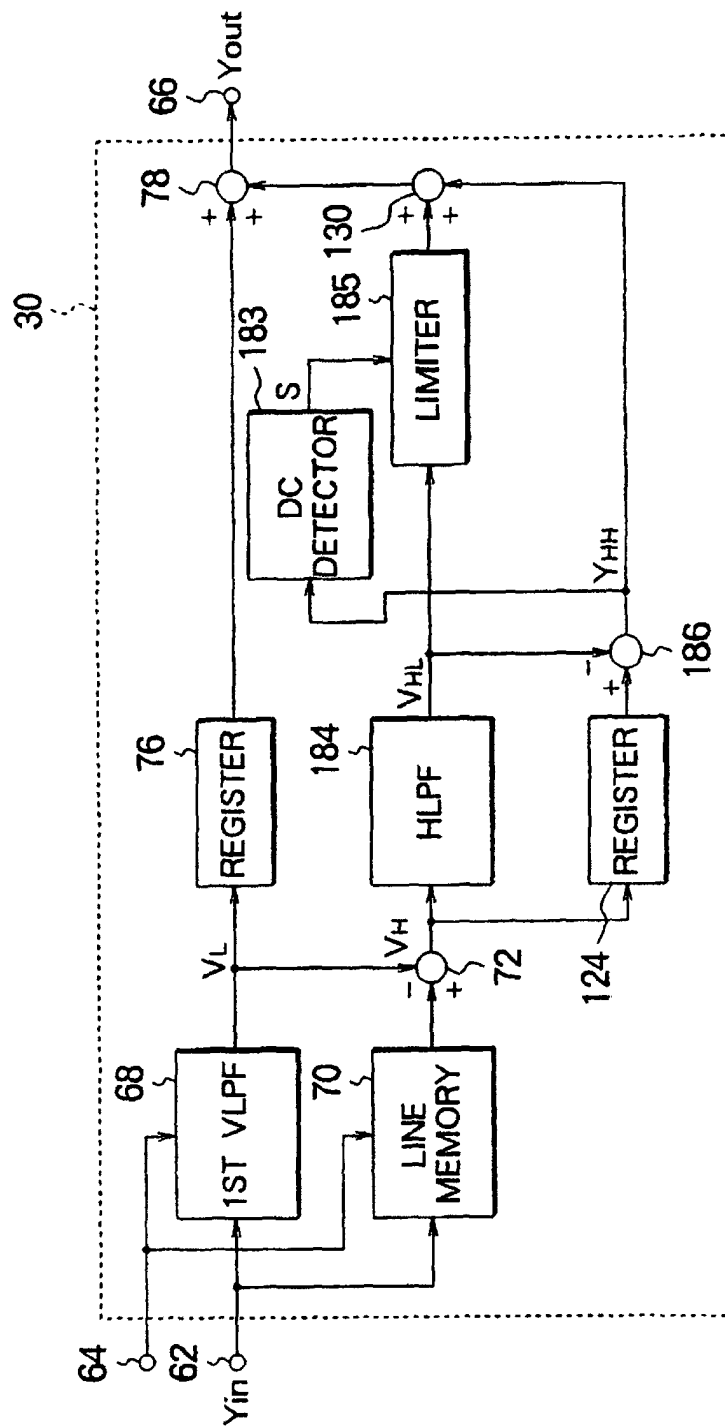


FIG. 23

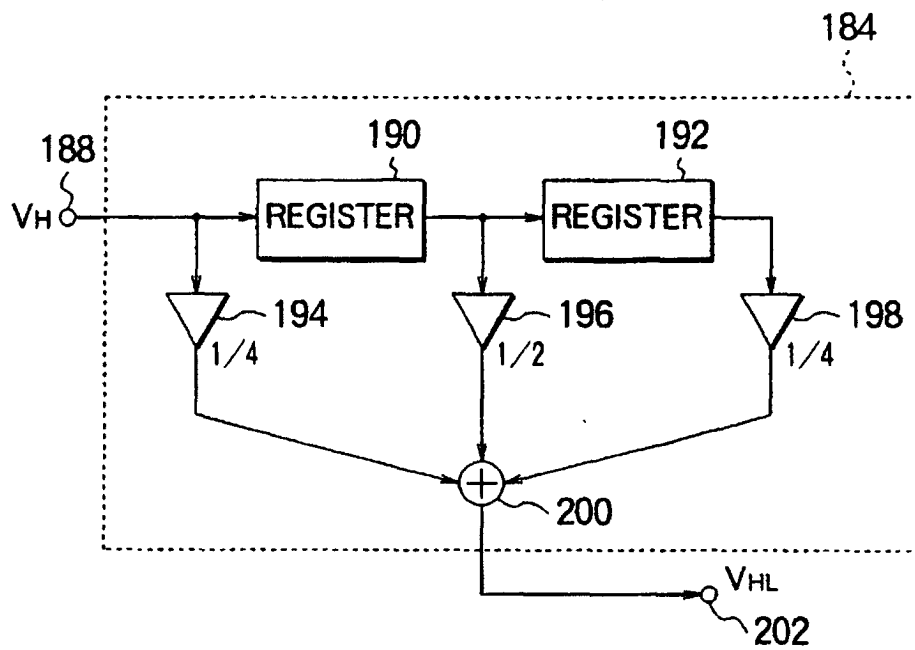


FIG. 24

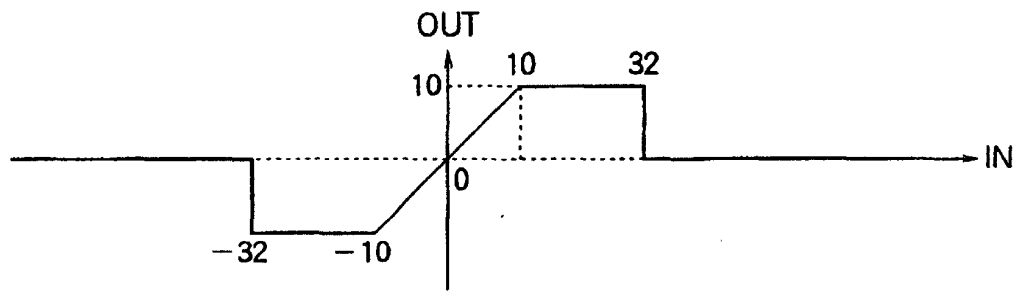


FIG. 25

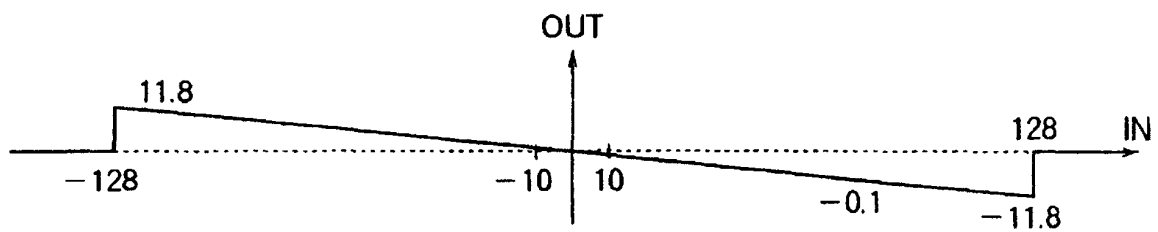


FIG. 26

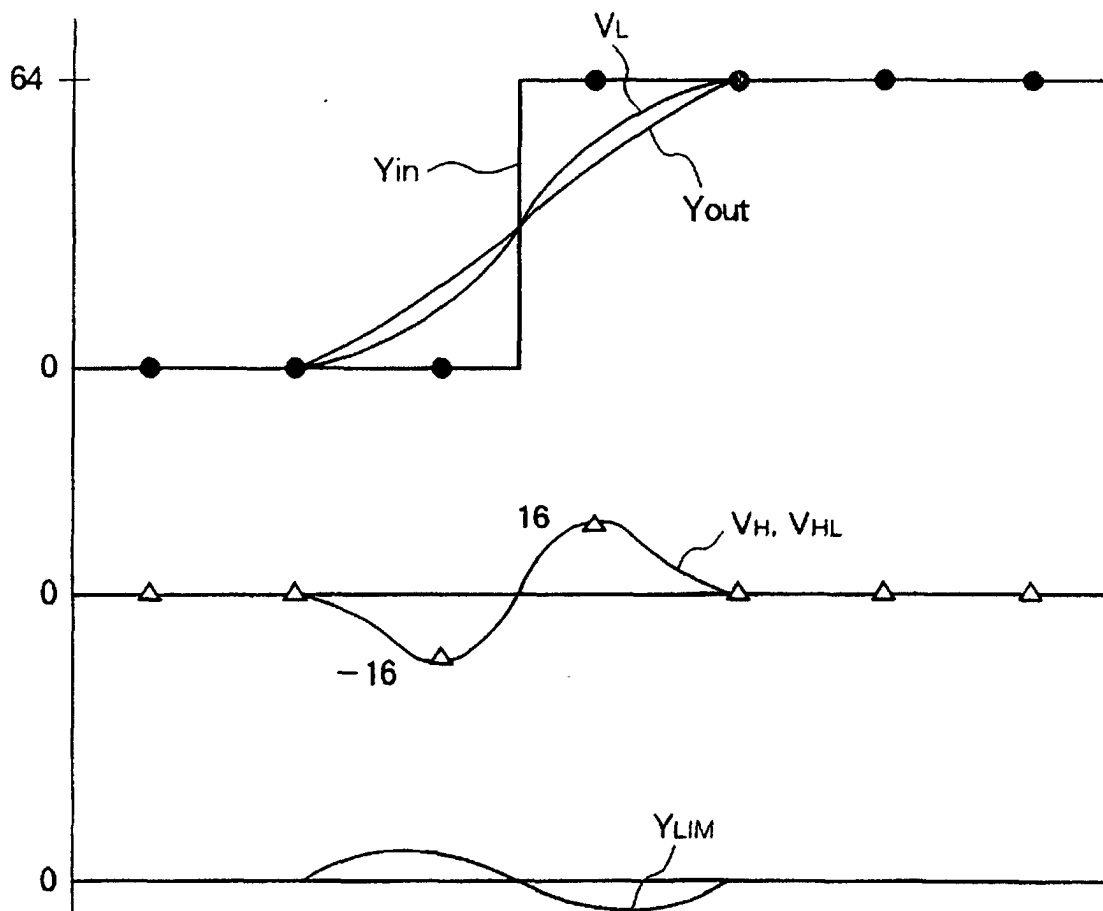


FIG. 27

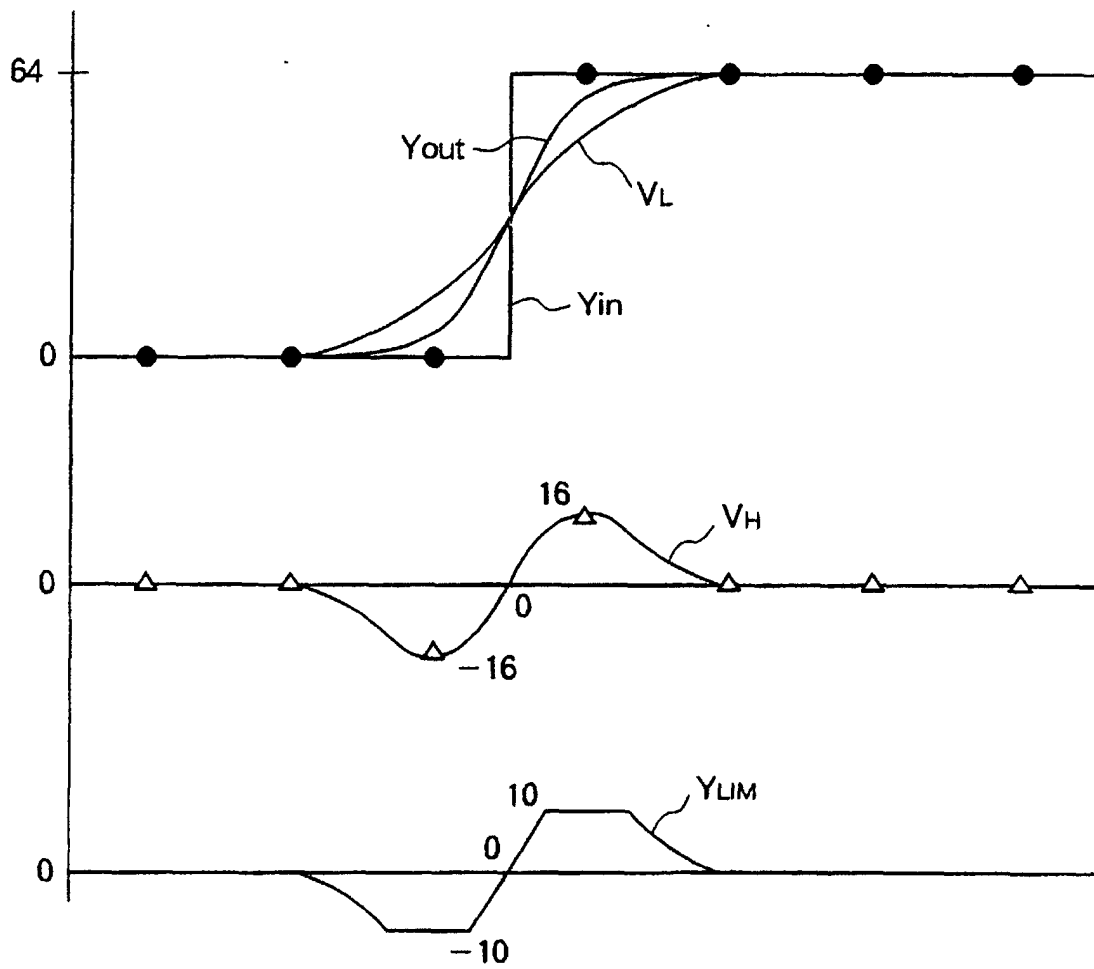


FIG. 28

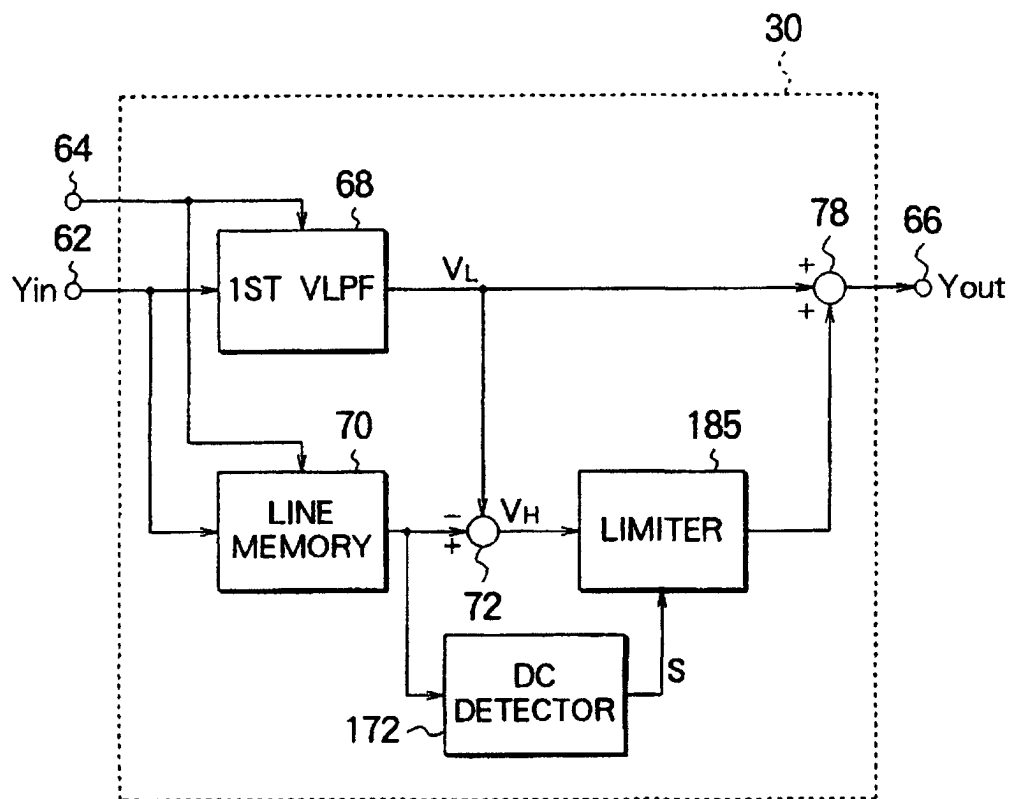


FIG. 29

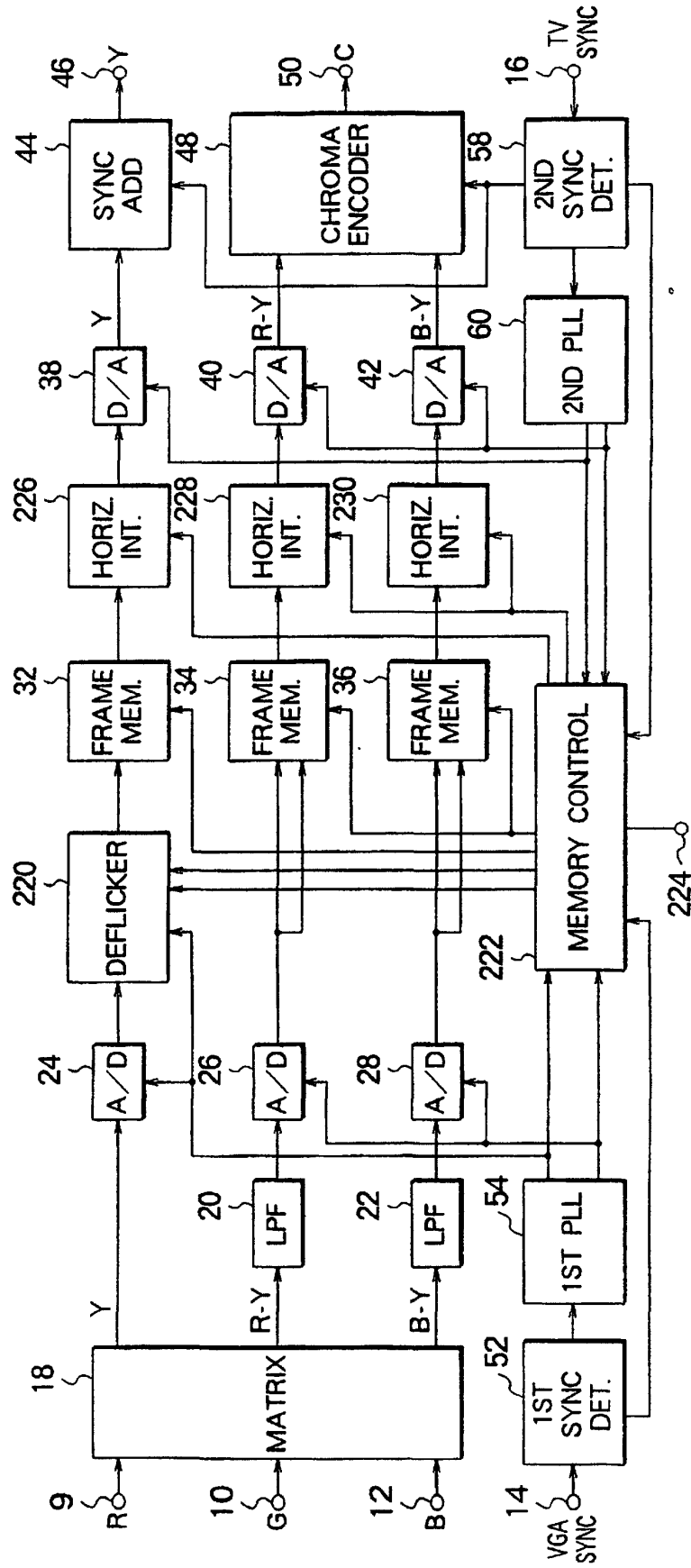


FIG. 30

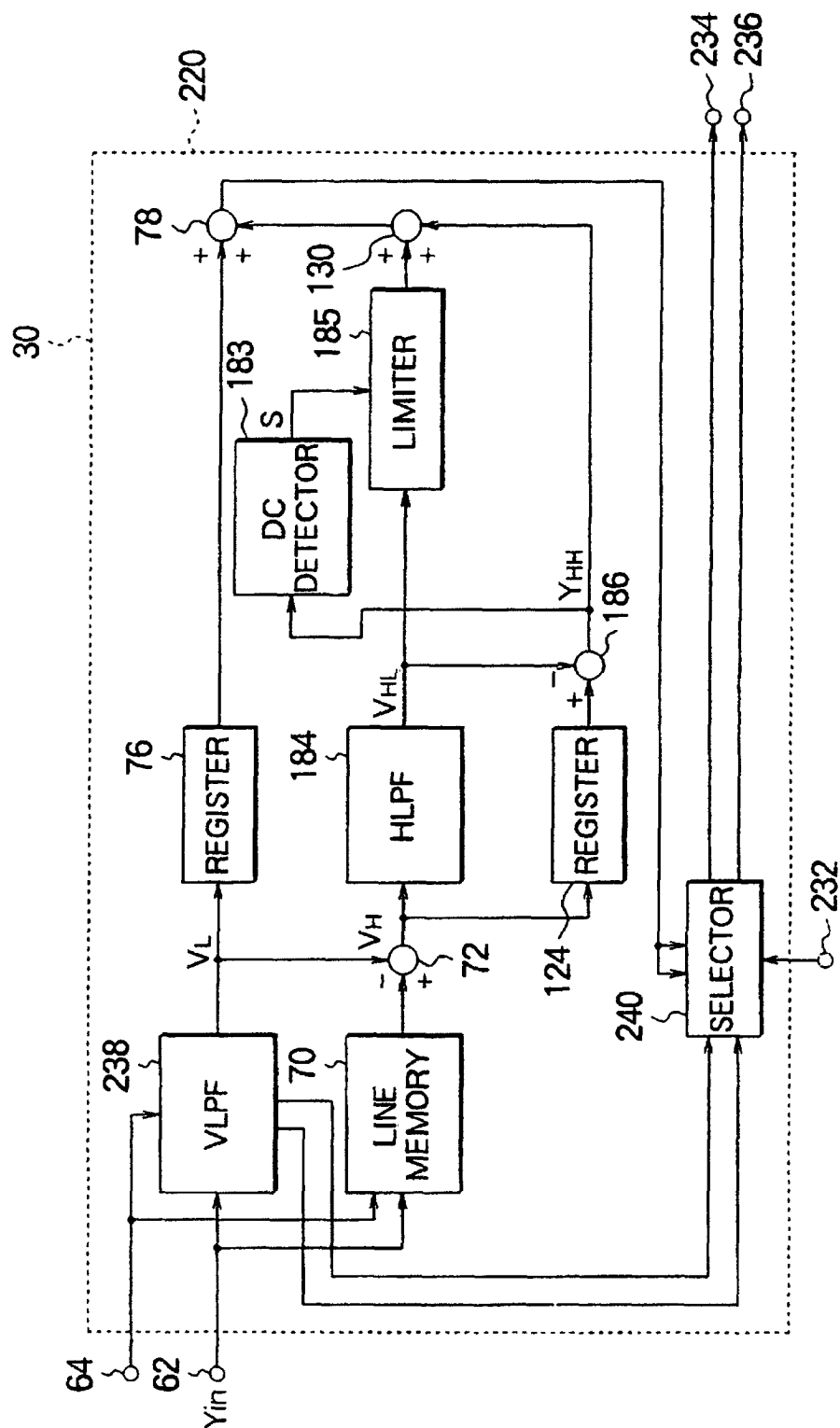


FIG. 31

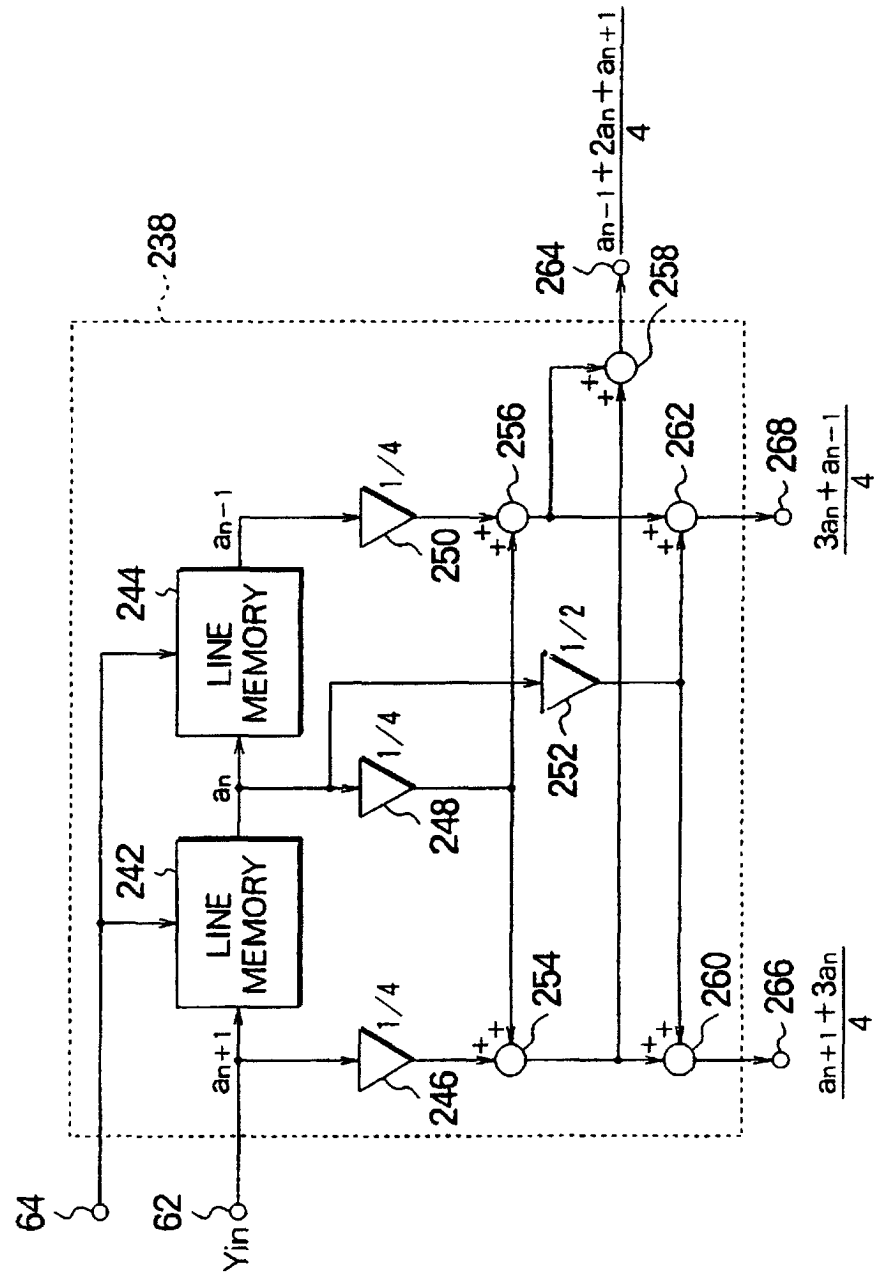


FIG. 32

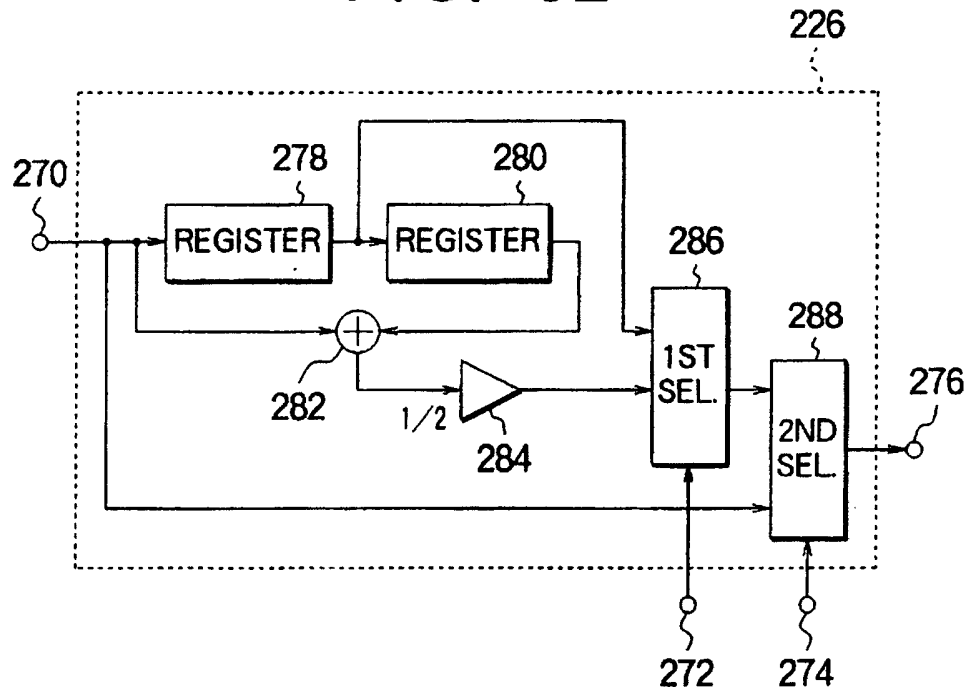


FIG. 33

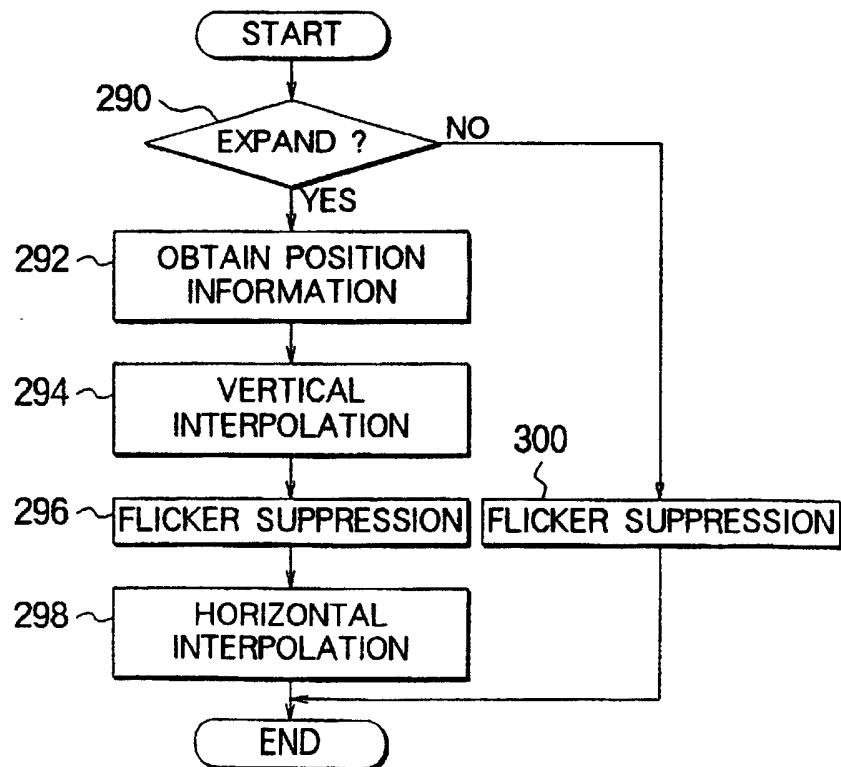


FIG. 34

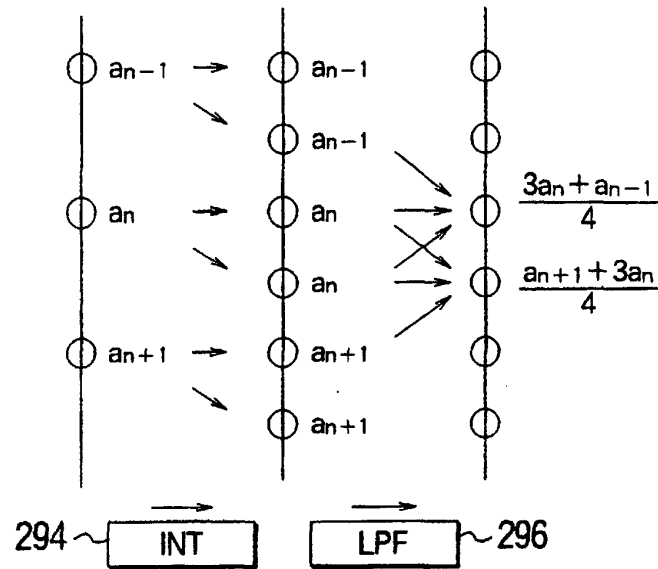


FIG. 35

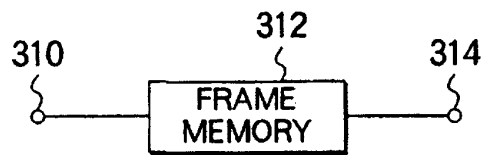


FIG. 36

