(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 766 499 A1

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
02.04.1997 Bulletin 1997/14

(51) Int. Cl.[6]: **H05B 41/00**, H05B 41/29

(21) Application number: **95830396.8**

(22) Date of filing: **27.09.1995**

(84) Designated Contracting States:
DE FR GB IT

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(54) Timing of different phases in an ignition circuit

(57) The need of implementing a second local oscillator beside the drive oscillator, for timing the different phases of the starting process of a half-bridge or bridge stage driving an external load such as a fluorescent lamp, is avoided by employing a timing counter to count the number of oscillations produced by the drive oscillator and a digital-to-analog converter for controlling the frequency of oscillation of the drive oscillator.

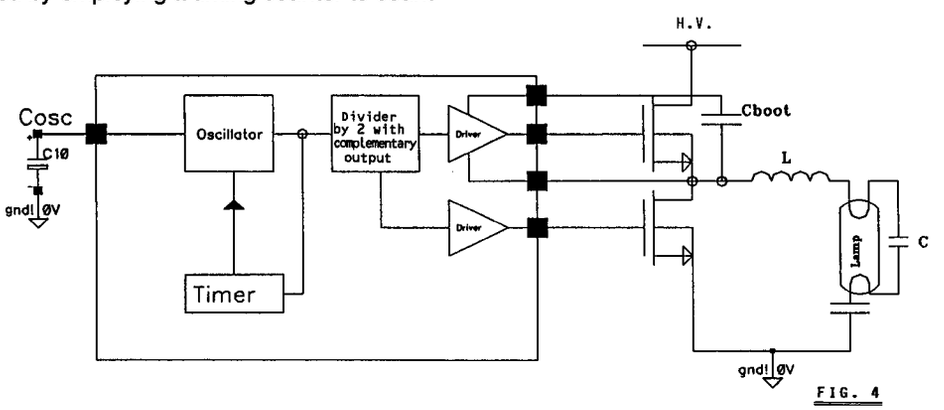

FIG. 4

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Description

The present invention refers to a driving circuit of a bridge or half-bridge stage that comprises means for timing the different operating phases. More in particular, this invention refers to a timing device for the preconditioning (preheating) phases of the bridge or half-bridge load. The invention is particularly useful for driving fluorescent lamps.

Usually, the optimal ignition procedure of a fluorescent lamp requires the preheating of filaments for a period of time that may vary between hundreds of milliseconds to a few seconds. The driving of the lamp occurs by exploiting an appropriate resonant LC circuit as schematically shown in the diagram of Fig. 1. The frequency of oscillation imposed by the driving circuit during the preheating phase is higher than the resonant frequency of the LC circuit (that is of the load of the bridge). Once the preheating phase is completed, the driving frequency of the bridge or half-bridge stage is diminished for increasing the voltage on the capacitor C and therefore at the lamp terminals, up to a point of reaching the arching voltage, thus igniting the lamp.

The preheating time may be preestablished in various ways.

In the specific case of resonant loads as in the illustrated case of a fluorescent lamp, analog devices may be employed, for example of the PTC type (Positive Temperature Coefficient) or otherwise it is possible to exploit the charge and discharge of external capacitors that may be connected to a pin of the device which will not interfere with the oscillating frequency of the driving circuit of the power bridge stage.

Fig. 2 shows the example of a resonant load circuit of a fluorescent lamp provided with a PTC device. Initially, the current flows through the PTC device, heating the lamp electrodes by Joule effect, thus stimulating thermoionic emission. As the current increases, the resistance of the PTC device increases and the bridge's load gradually becomes more similar to an LC circuit, whose impedance tends to rapidly decrease thus increasing the voltage on the lamp until it eventually ignites. The timing of the preheating phase using a PTC device is not very precise since it strongly depends on the ambient temperature at which the system is operating (for example, it may depend on when and for how long the lamp was previously turned on and on the heat dissipation characteristics of the system).

The usual solution when a higher timing precision is required for the preheat ignition sequence is that of employing a timing counter (Timer) capable of counting the oscillations of an auto-oscillating circuit (Oscillator) and of producing an output signal that modifies the oscillating frequency of the local oscillator of the driving circuit. The adjustment of the duration of the preheating period is obtained by modifying the value of an external capacitor (CT) that regulates the oscillation frequency of such a second oscillator, dedicated to this auxiliary timing function. This alternative way to regulate preheating time is more precise than that of the system shown in Fig. 2 because it does not directly depend directly on the temperature. However, it involves the integration of a second oscillator as well as requiring a dedicated pin (typically provided with a relative protection from electrostatic discharges (ESD)) specifically for this function, in addition to a further external capacitor CT.

Similar requirements may also occur when driving resonant loads different from a fluorescent lamp and for this reason the above discussed problem and the relative solution that is the object of the present invention must be considered in more general terms and not limitatively for the specific instance of a load constituted by a fluorescent lamp.

The circuit arrangement of the present invention allows for controlling the duration of the different preconditioning or preheating phases, the timing of the start-up or ignition and of attaining steady state operating conditions of a resonant load of a bridge or half-bridge stage neither the integration of a second oscillating circuit nor the use of a pin of the device for connecting an external capacitance for regulating the frequency of oscillation of such a second or auxiliary oscillator.

The system of the invention is based on the use of an n-bit digital counter that can be started up by a command generated by the logic circuitry of the control system and capable of counting the oscillations generated by the same oscillator of the driving circuit of the bridge or half-bridge stage. The duration of the preheating phases may be preestablished in the design stage or programmable by means of suitable memories (PROM, EPROM or EEPROM) or similar devices.

According to an important aspect of the circuit of the invention, the n outputs of the timing digital counter drive a digital-to-analog converter DAC, whose output current is used for regulating a current controlled oscillator (CCO) of the driving circuit.

By increasing the number of bits of the timing counter and the corresponding number of current generators of the digital-to-analog converter, it is possible to increase the number of steps through which the adjustment of the driving circuit oscillation frequency takes place, thus preventing excessively ample and abrupt variations of the frequency of oscillation.

By modifying, by way of programming, an appropriate decoding circuit, it is then possible to define the different duration intervals corresponding to the different start-up phases, for example the preheating time, the time of the decrement of the oscillation frequency (for eventually determining the arching) and the time of incrementing the frequency until reaching an appropriate value for steady state operation.

Of course, programming can be defined by the fabrication masks or carried out by electric means on the finished device.

The various aspects and relative advantages of this invention will become even more evident through the following description of some important embodiments and by referring to the enclosed drawings, wherein:

Figure 1 shows, as previously mentioned, a typical driving scheme for a fluorescent lamp;

Figure 2 shows, as previously mentioned, the driving scheme of a fluorescent lamp that comprises an analog device for regulating the preheating time;

Figures 3, **3a** and **3b** schematically show, as previously mentioned, a block diagram of a driving circuit employing a second oscillator and a timing counter for controlling the preheating time and the relative operation diagrams of the circuit;

Figures 4, **4a** and **4b**, schematically show a block diagram of a circuit realized according to the present invention and the relative operation diagrams;

Figure 5 is a more detailed diagram of an embodiment of the invention;

Figures 6 and **7** represent the operation diagrams of the circuit of Fig. 5;

Figure 8 shows an alternative embodiment of the circuit.

The system of the invention is diagrammatically shown in Figures 4, 4a and 4b. As it may be observed, the diminishing of the oscillation frequency of the oscillator of the driving circuit, after a certain preheating time and the successive eventual increasing of the frequency toward a steady state value, is realized by a timing counter (Timer) that counts the number of oscillations produced by the same local oscillator (Oscillator) of the driving circuit, without the need of a second oscillator, exclusively dedicated to the timing functions.

As shown in the diagrams of Figures 4a and 4b illustrating the operating characteristics, the digital output of the timer can be advantageously used for making gradual the charge of the frequency from the initial oscillation frequency that is maintained for a certain preheat period toward a typically lower working frequency.

By using a standard digital-to-analog converter (DAC) circuit a signal can be generated whose level is incremented by a constant amount as the counting of the number of oscillations by the counter proceeds.

According to a preferred embodiment of the invention, the circuit can be realized according to a functional scheme as shown in Fig. 5. The timing counter (Timer) is reset by a start-up signal generated by the logic circuit of the control system.

A dedicated coding-decoding circuit CODIF.-DECOD., that may be prearranged in the design stage or programmable (according to methods already mentioned above) defines the time intervals of interest (Tpreheat, Tsweep-down, Tsweep-up). This block, indicated with PROM as a whole, can be realized in various ways, functionally equivalent to each other as it is evident to a technician. The CODIF. block can be intended as a set of programmable connections, whereas the DECOD. blocks may be viewed as a set of a NAND gate.

The output signals (Tpreheat, Tsweep-down, Tsweep-up) can be stored by bistable (Flip-Flops) circuits which attend to the functioning of the timer and enable the DAC through a series of AND gates (A1, A2, ...).

The n outputs of the counter (Q1, Q2, ..., Qn) drive a digital-to-analog converter circuit (DAC) constituted by the MOS transistor MO, M1, ... Mn, M30, M31, M(30+n) and having a current output. The maximum output current value of the of the Iosc converter, which constitutes the control signal of the current controlled oscillator (CCO), is given by the following equation:

$$Imax=Imin+I^{*}\frac{2^{n}-1}{2^{n}},$$

when the counter outputs Q1, Q2, Qn, are all low (i.e. to a logic value "0").

The minimum Iosc value corresponds to the Imin current produced by the first generator MO in a configuration where all the counter outputs interfacing with the DAC assume a high logic value ("1").

It is important to highlight the fact that the n number of timer outputs and the number of the DAC inputs are totally independent and as such, may advantageously be different from each another. It is only for simplicity of description that these were shown equal (equal to n).

As in the example shown, the timer may be realized with an Up-Down Counter. This is reset by the start-up signal.

From the moment the CCO oscillator starts to oscillate to the moment when the Tpreheat signal assumes a logic state "1", thus determining the switching of the output of the Flip-Flop FF1, the Iosc current remains constant and given by the Imax value. Therefore, the frequency of oscillation remains constant.

This phase defines the preheating or preconditioning time of the lamp (or of an equivalent load).

Depending from the programming of the decoding circuit (DECOD.), the digital-to-analog converter DAC is enabled through the logic gates A1, A2, ..., An when Tpreheat switches to a high logic state. The same Tpreheat signal, suitably stored, resets the counter to zero (Reset phase).

From this instant onwards, the oscillating frequency decreases each time the output digital datum of the timer varies.

The duration of the time intervals during which the CCO oscillator oscillates at a constant frequency becomes dependent on the oscillating frequency itself (in other words, it increases as the frequency decreases). This is highlighted in the operating characteristics shown in Figures 6 and 7 by the nonuniform duration of the steps.

This second phase of operation terminates when the Tsweep-down signal becomes high.

At this point, the aforementioned signal, suitably stored by a bistable circuit FF2, commands a charge of the mode of operation of the Counter; namely from an Up-Counter mode to a Down-Counter mode.

In practice, the DAC retraces backward its previous excursion. This means that the oscillator current starts to increase again and with it the frequency of oscillation of the system, always in a stepwise fashion.

The latter phase terminates when the Tsweep-Up signal switches and with it the relative bistable circuit FF3.

Generally, at this point, generally, the control may commonly be assumed by another signal capable of regulating the functioning of the system under normal steady state condition.

Such a steady state control signal is highlighted in the figures with the generic name of Feedback Signal.

In theory, the Tsweep-Up signal and the third bistable circuit FF3 would not be strictly necessary because the Feedback Signal could be enabled by means of the FF2 Flip-Flop output, leaving to the system itself the decision about which control mode to follow (that is the one imposed by the Sweep-Up Signal or that governed by the Feedback Signal).

According to this alternative embodiment shown in Fig. 8, the system follows the curve of frequency increment up to the point of attaining the level determined by the Feedback Signal. At this point, the circuit releases itself from the Sweep-Up control and continues functioning under control of the Feedback Signal, which signal by acting upon the Up/Down Counter and consequently on the DAC, regulates the frequency of oscillation, incrementing or decrementing it depending on the external conditions.

In the embodiments of Figures 5 and 8, the use of Flip-Flops of the JK type is shown, employing an inverted clock signal, that is in phase opposition to the clock signal of the timer, as provided by an appropriate inverter INVC. This technique has the advantage of avoiding the effects caused by spurious switching (glitch) of the timer by ensuring that the bistable circuit switch when the input signal are stabilized. Naturally, this aspect is not strictly necessary to the functioning of the circuit of the invention because the bistable circuits (Flip-Flop) can also be of a different kind, not requiring an inverted clock signal.

Claims

1. A circuit for driving a half-bridge or bridge stage at a certain frequency comprising a local oscillator and means capable of modifying for intervals of time of a programmable duration the frequency of oscillation during distinct phases of preconditioning, ignition and steady state operation, referred to a load driven by the stage, characterized in that said means comprise a timing counter capable of counting the number of oscillations produced by said local oscillator and a digital-to-analog converter capable of generating a control signal of the frequency of oscillation of the local oscillator.

2. The circuit according to claim 1, characterized in that said timing counter is an n-bit reversible counter (Up-Down), whose n outputs are enabled to drive a digital-to-analog converter having a current output, which controls a current controlled local oscillator.

3. The circuit according to claim 2, characterized in that it comprises a programmable memory of the read only, nonvolatile type capable of defining, depending on the programming, the duration of said distinct phases of operation.

4. The circuit according to claim 3, wherein said memory comprises a coding circuit capable of generating at least a first and a second timing signal and a decoding circuit capable of receiving as input the digital datum represented by the configuration of the n-outputs of said counter;

at least a first and a second bistable circuit, both employing as a clock signal a signal at the controlled frequency of said local oscillator and capable of receiving as input said first and said second timing logic signals, respectively;

said bistable circuits being respectively capable of preloading said counter with a programmed value and to enable said n-outputs of the counter to drive the respective stages of said digital-to-analog converter and of transferring the control of said counter to a steady state control signal.

5. The circuit according to claim 4, characterized in that said decoding circuit generates a third timing signal and the circuit comprises a third bistable circuit controlled by said third timing signal capable of defining a phase of increment of the frequency from a minimum value reached at the end of a starting phase to a steady state value, before control is transferred to said control signal.

6. The circuit according to any of the preceding claims, characterized in that said bistable circuits are Flip-Flops of the JK type employing an inverted clock signal as referred to the clock signal that is applied to said counter.

7. An integrated load driving system employing at least a bridge output stage, characterized by comprising a timing circuit of distinct phases of operation as defined in the preceding claims.

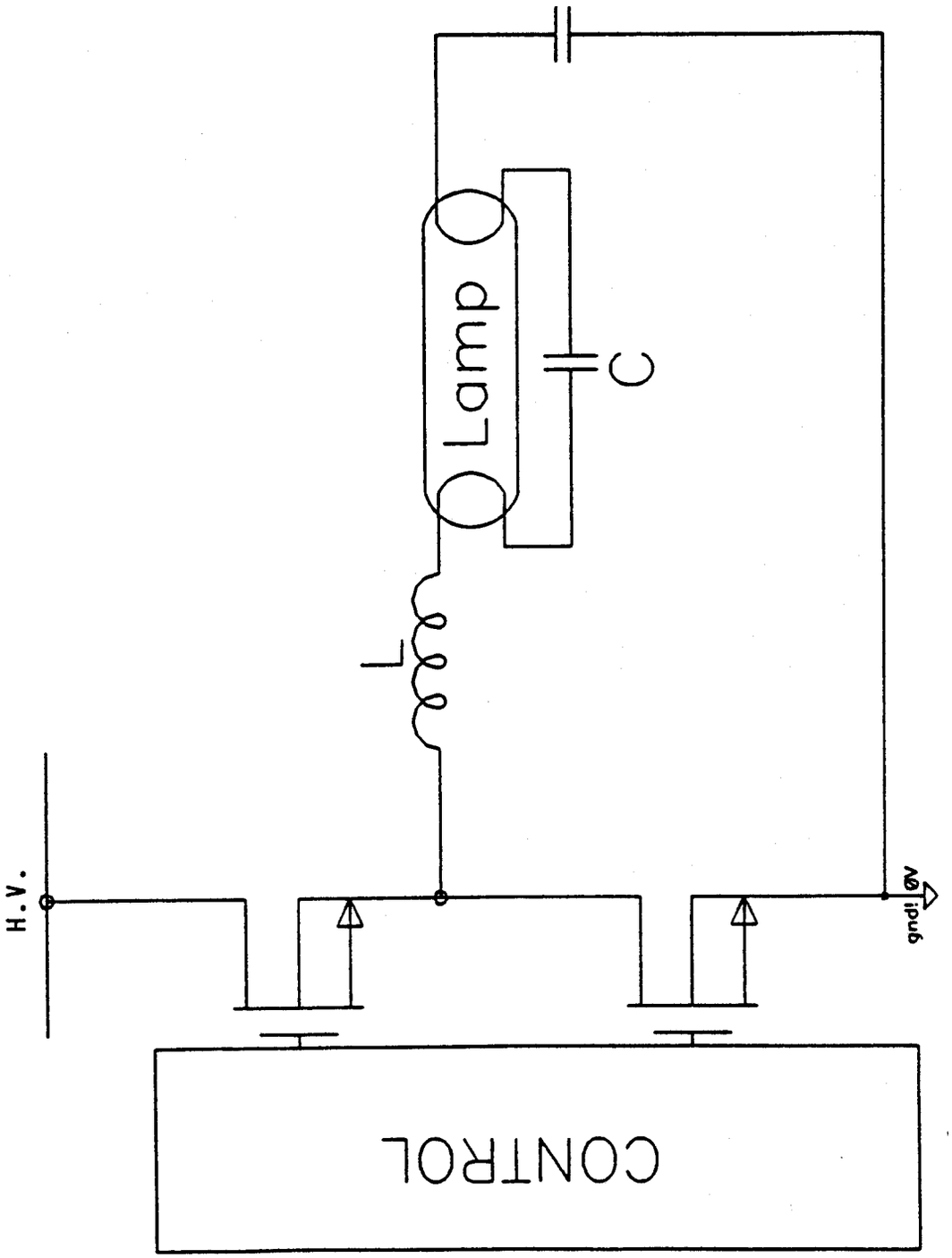

FIG. 1

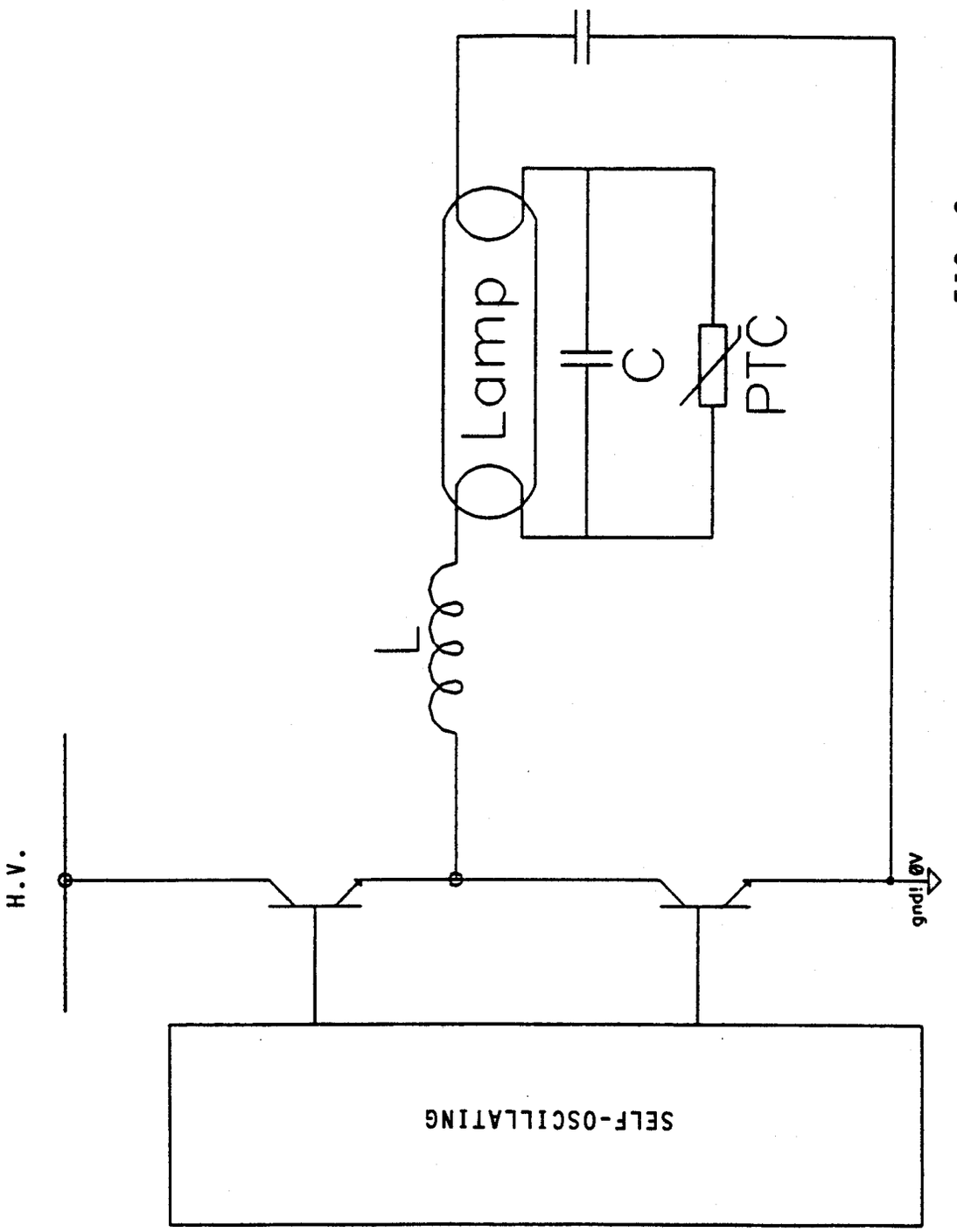

FIG. 2

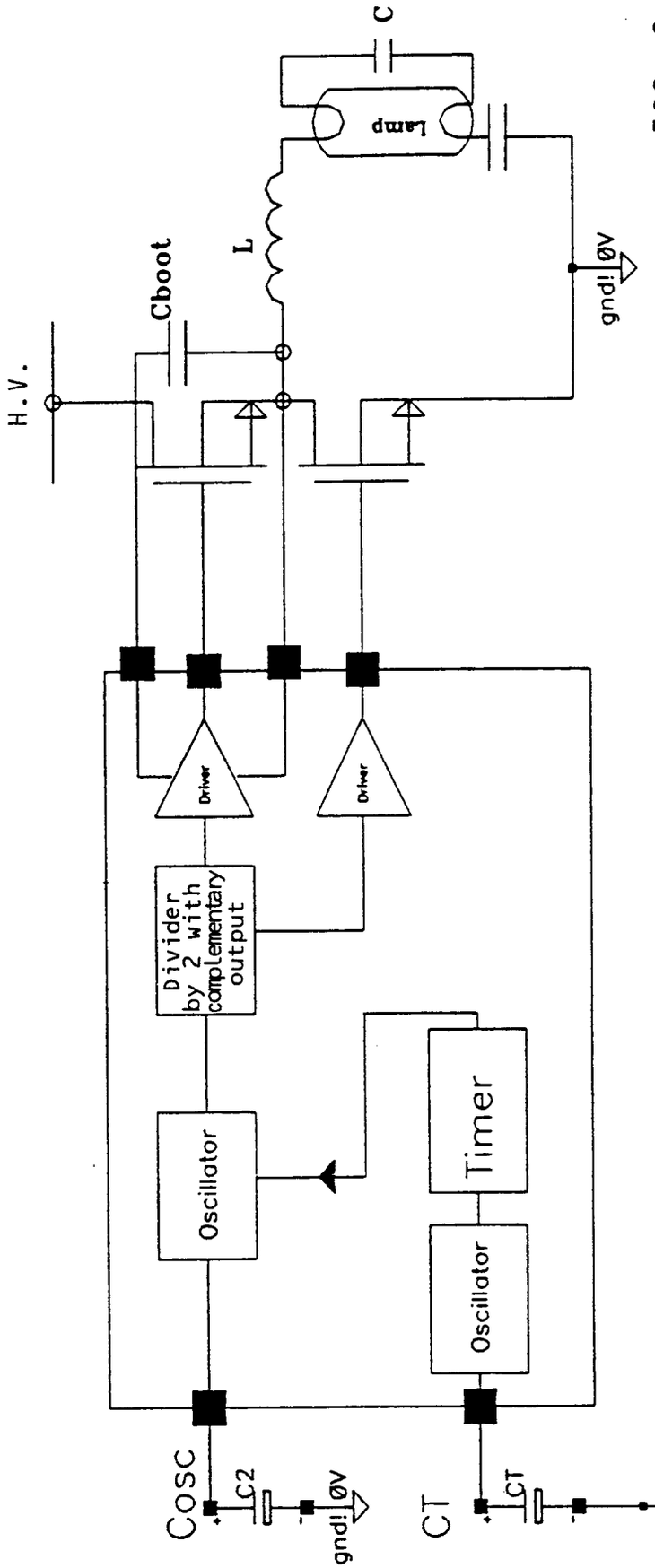

FIG. 3

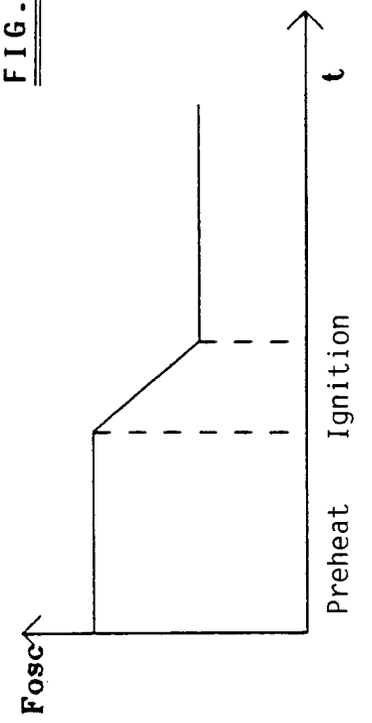

FIG. 3b

or

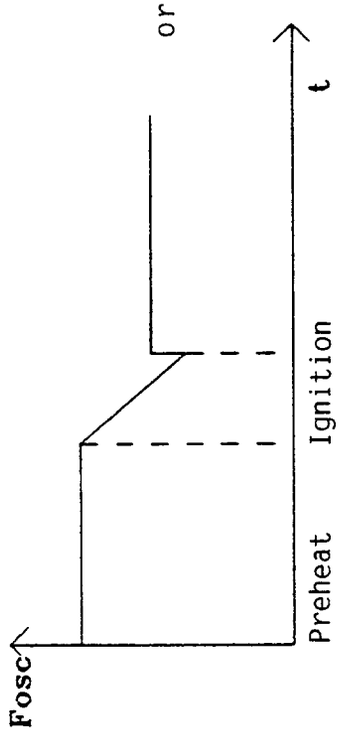

FIG. 3a

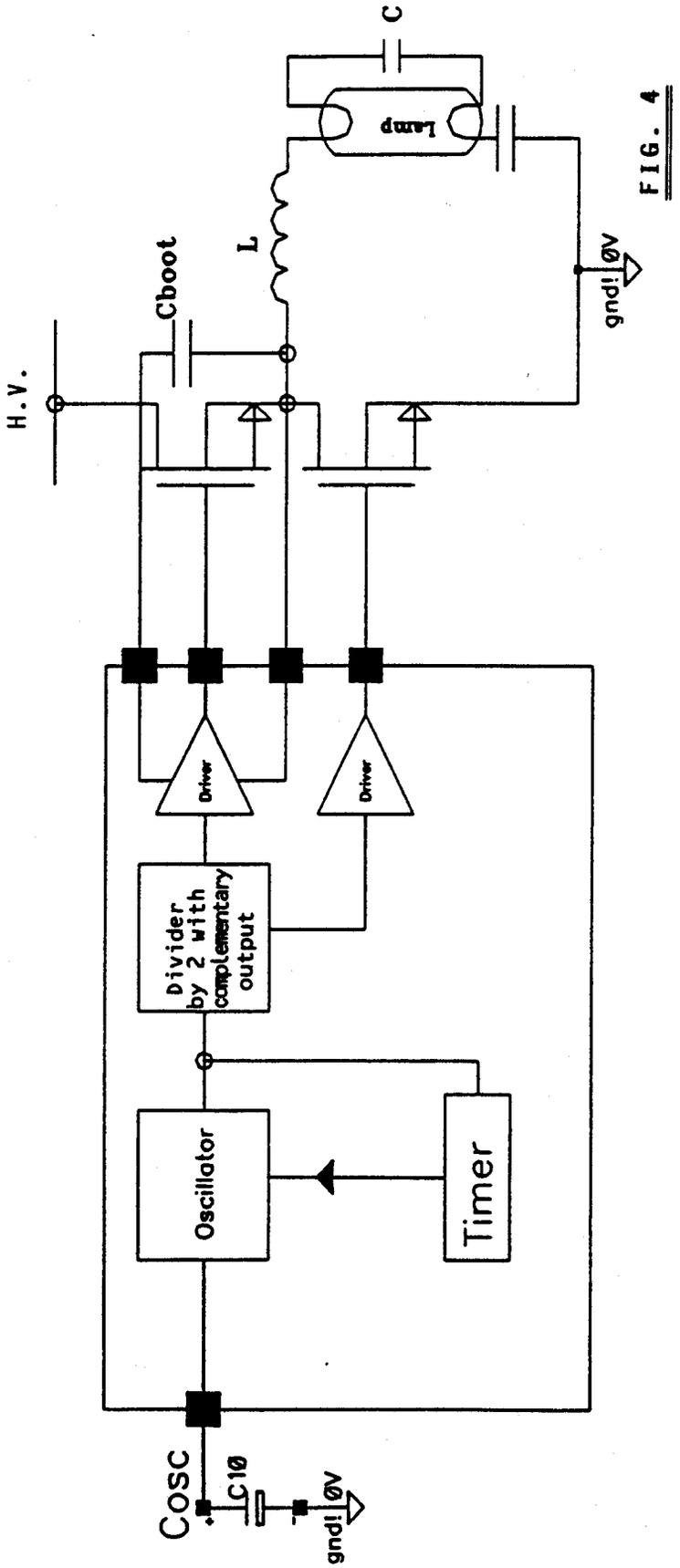

FIG. 4

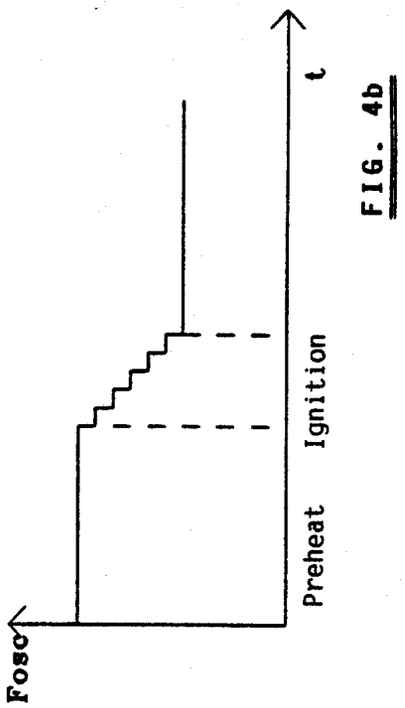

FIG. 4b

or

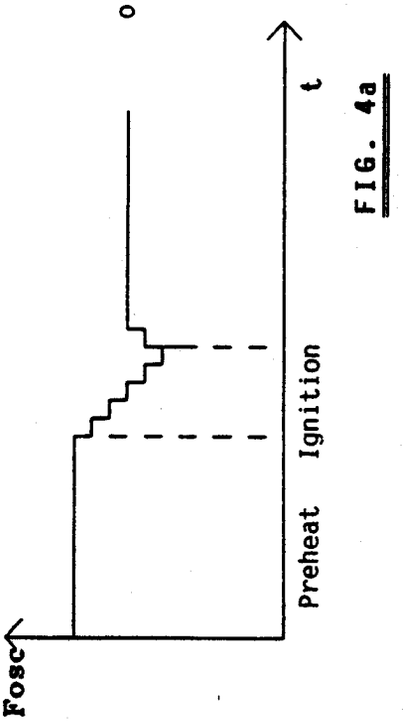

FIG. 4a

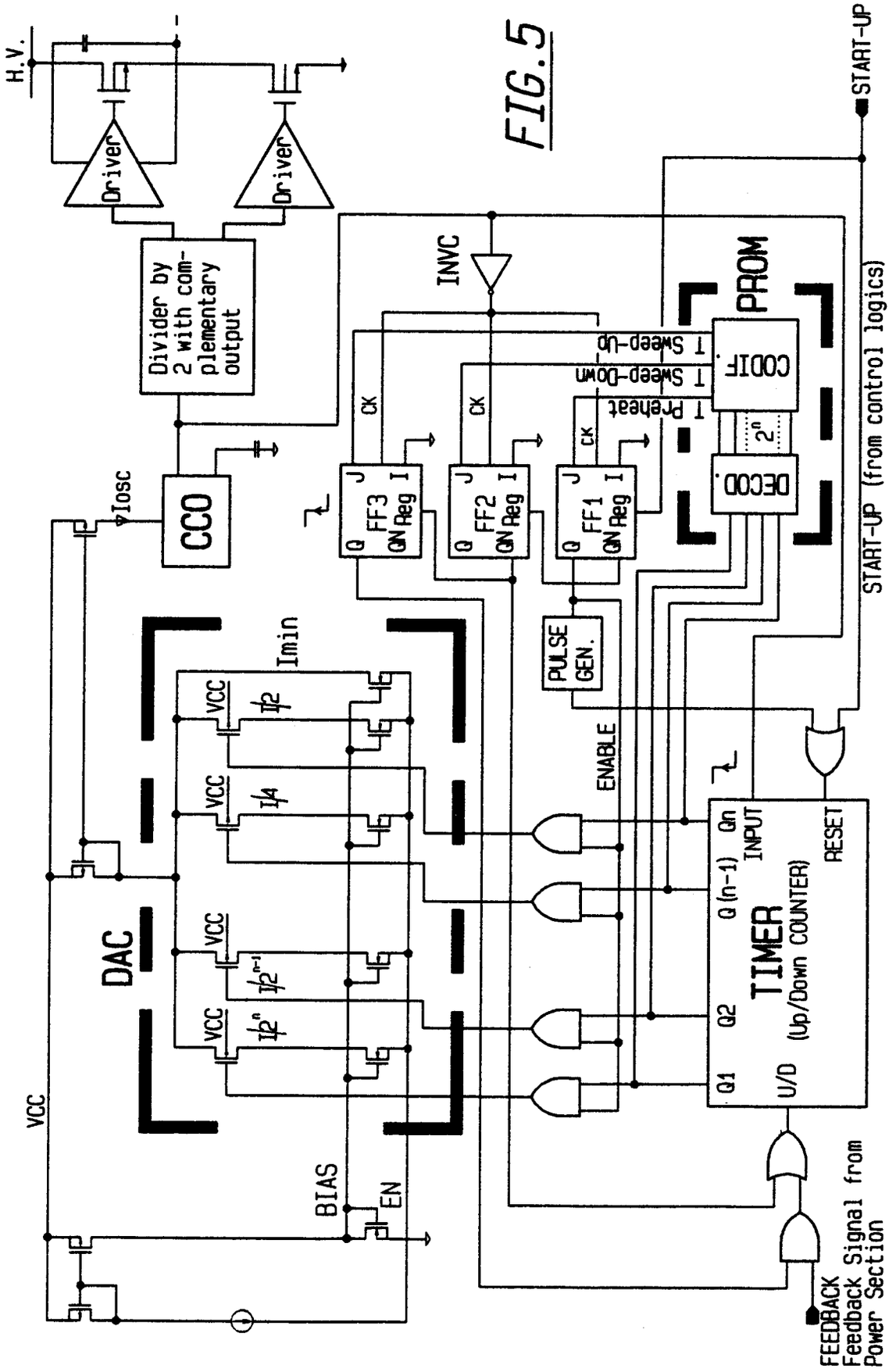
H.V.
Driver
Driver
Divider by 2 with complementary output
CCO
φIosc
INVC
CK
FF3 QN Reg
FF2 QN Reg
FF1 QN Reg
PROM
COUNTER
DECOD.
2^n
T Sweep-Up
T Sweep-Down
T Preheat
START-UP
START-UP (from control logics)
PULSE GEN.
ENABLE
DAC
Imin
VCC
1/2
1/4
1/2^(n-1)
1/2^n
BIAS
EN
TIMER
(Up/Down COUNTER)
INPUT
RESET
Qn
Q(n-1)
Q2
Q1
U/D
FEEDBACK
Feedback Signal from Power Section

FIG.5

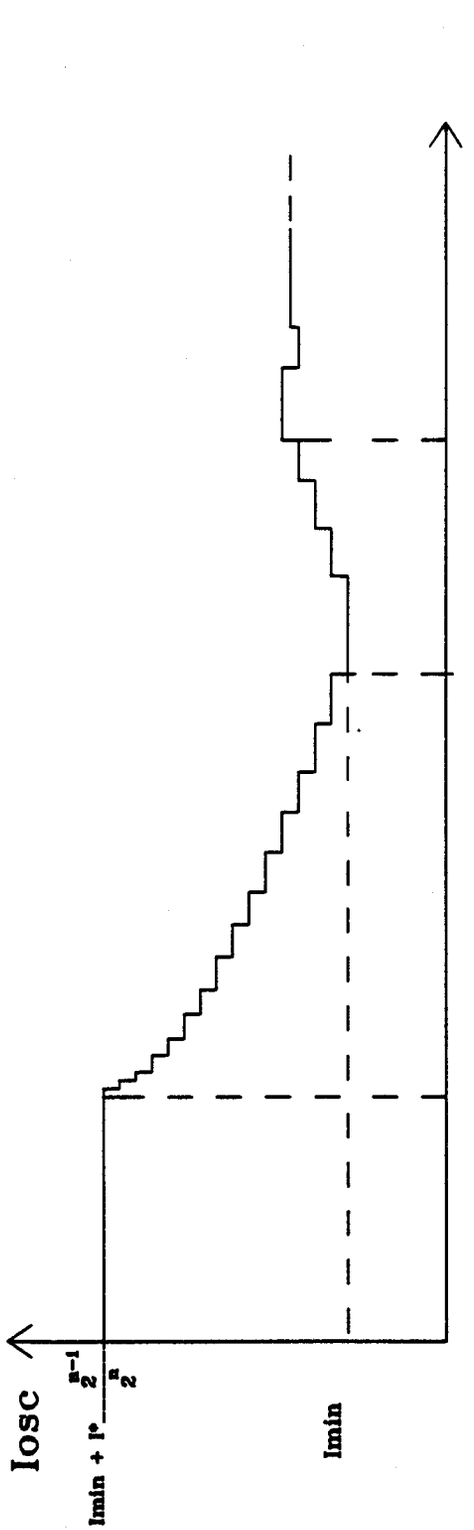
Iosc
Imin + I°
Imin

FIG. 6

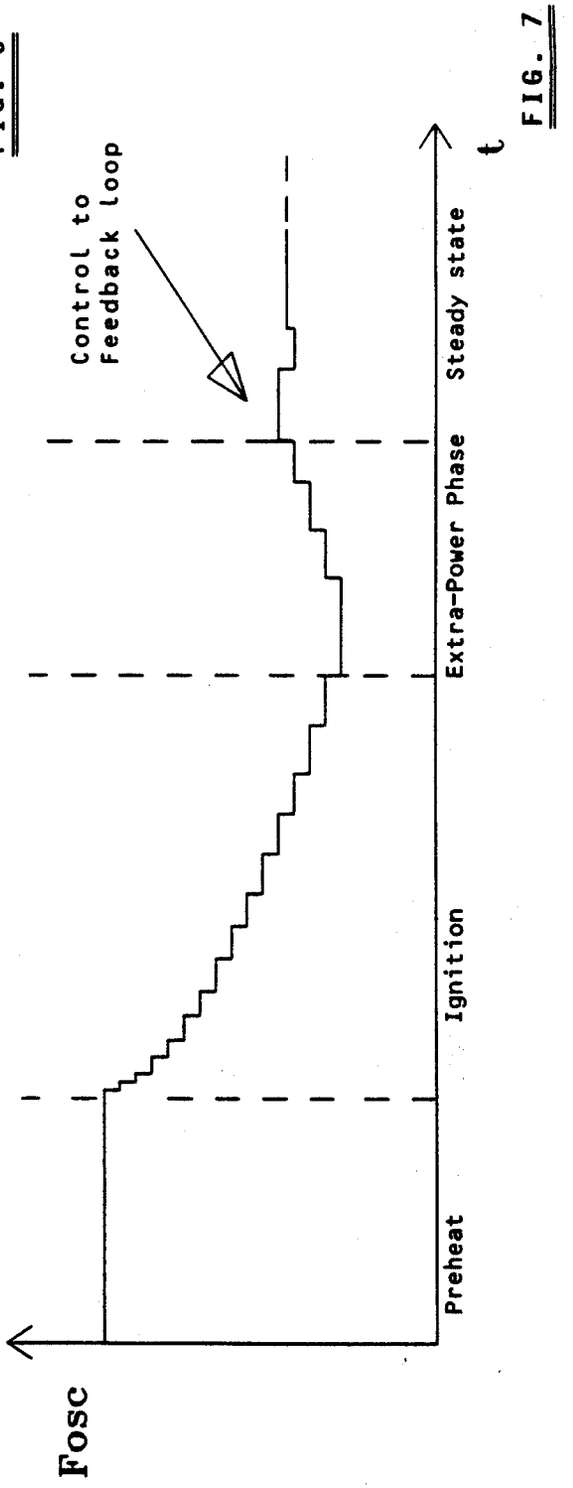
Control to
Feedback loop
Fosc
Preheat
Ignition
Extra-Power Phase
Steady state
t

FIG. 7

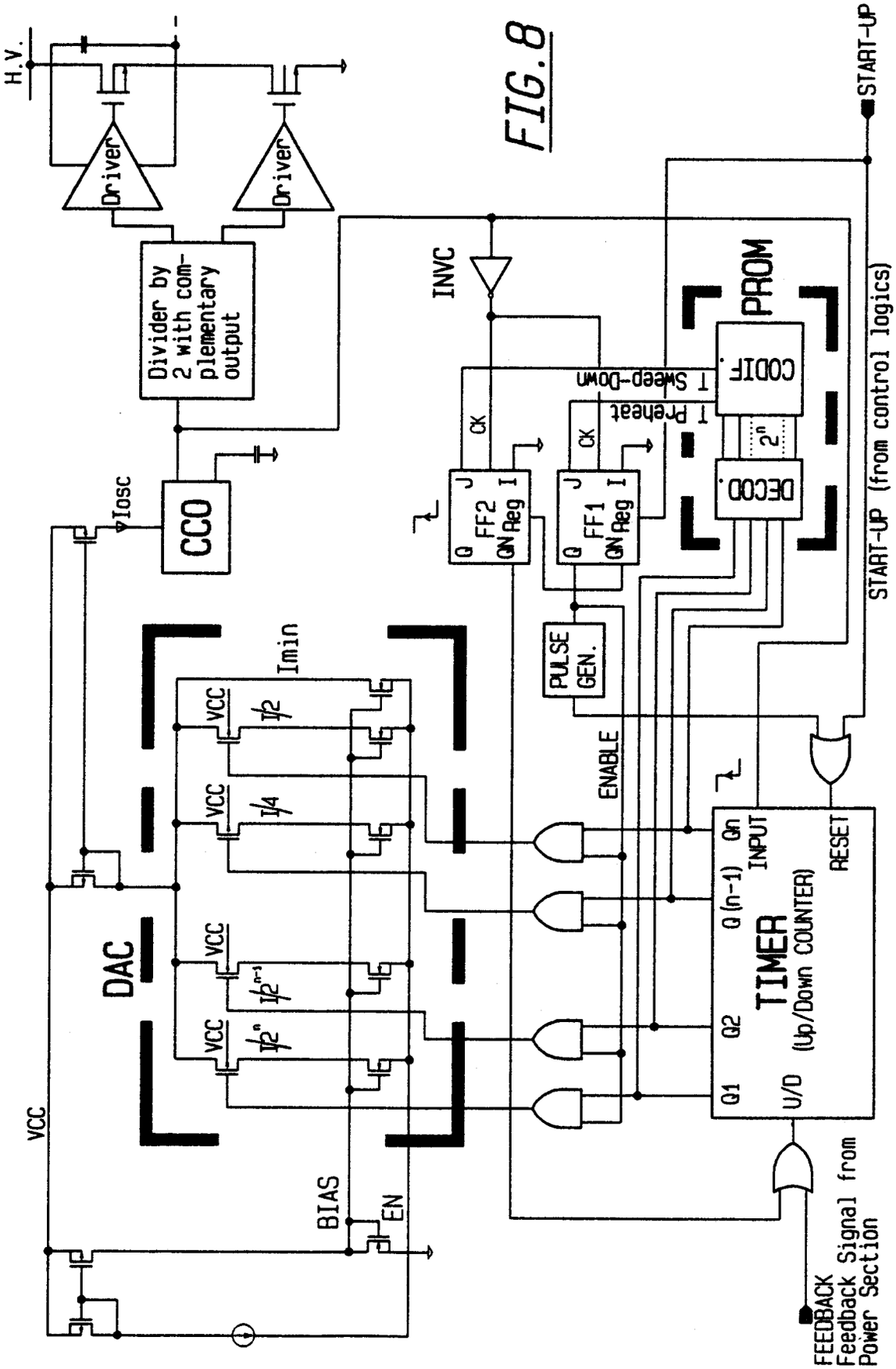
H.V.
Driver
Driver
Divider by 2 with complementary output
CCO
Iosc
INVC
PROM
CODIF.
DECOD.
2^n
T Sweep-Down
T Preheat
CK
J
Q
FF2 QN Reg
K
FF1 QN Reg
PULSE GEN.
ENABLE
START-UP
START-UP (from control logics)
DAC
Imin
VCC
1/2
1/4
1/2^(n-1)
1/2^n
BIAS
EN
TIMER
(Up/Down COUNTER)
Q1
Q2
Q (n-1)
Qn
INPUT
RESET
U/D
FEEDBACK
Feedback Signal from Power Section

FIG.8

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 95 83 0396

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	EP-A-0 338 109 (ZUMTOBEL) * column 5, line 16 - column 5, line 55 * * column 10, line 41 - column 10, line 48; figure 1 * ---	1	H05B41/00 H05B41/29
A	EP-A-0 359 860 (SIEMENS) * column 6, line 17 - column 8, line 19; figures 4,5 * -----	1	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

H05B
H02M

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	7 February 1996	Speiser, P

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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