(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 775 993 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
28.05.1997 Bulletin 1997/22

(51) Int. Cl.[6]: **G09G 3/28**

(21) Application number: **96118196.3**

(22) Date of filing: **13.11.1996**

(84) Designated Contracting States:
DE FR GB

(30) Priority: **17.11.1995 JP 299576/95**

(71) Applicant: **Oki Electric Industry Co., Ltd.**
Tokyo (JP)

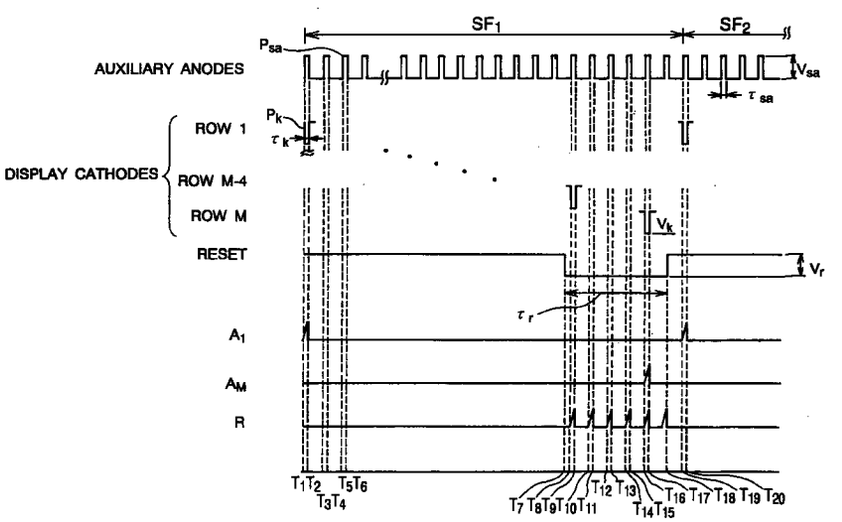
(72) Inventors:
- **Kobayashi, Yoshihiko**
  Minato-ku, Tokyo (JP)
- **Takahashi, Atsushi**
  Minato-ku, Tokyo (JP)
- **Takasaki, Shigeru**
  Minato-ku, Tokyo (JP)
- **Terouchi, Yuji**
  Minato-ku, Tokyo (JP)

(74) Representative: **Betten & Resch**
Reichenbachstrasse 19
80469 München (DE)

(54) Method of driving a DC plasma display panel

(57) A DC plasma display panel has a row-column matrix of display cells and auxiliary cells, and a row of reset cells adjacent to the first row of auxiliary cells. The display cells and auxiliary cells are driven a row at a time in a sequence that starts from the first row and repeats cyclically. The reset cells are driven during a part of this sequence in which display and auxiliary cells in rows other than the first row are driven, preferably including the time during which the display and auxiliary cells in the last row are driven.

FIG. 4



EP 0 775 993 A2

Description

BACKGROUND OF THE INVENTION

This invention relates to a method of driving a direct-current plasma display panel, referred to below as a DC plasma display panel.

DC plasma display panels, also known as gas discharge panels, appear promising for applications such as high-definition television (HDTV). One type of DC plasma display panel has a row-column matrix of display cells with interspersed columns of auxiliary cells, and a single row of reset cells disposed adjacent to the first row of display and auxiliary cells. The auxiliary cells serve to prime the display cells, and the reset cells serve to prime the auxiliary cells in the first row. The cells are driven a row at a time.

When this type of DC plasma display panel is used to display a television picture, the time allotted to each field of the television signal is divided into a number of segments referred to as subfields. The display cells and auxiliary cells are driven in repeated cycles, one cycle per subfield, in a manner that permits different intensity gradations to be displayed. The reset cells are conventionally driven at the beginning of each subfield, before the driving of the display cells and auxiliary cells begins, so that in each subfield, the reset cells are not driven during the time when the display cells and auxiliary cells are being driven.

A problem with the conventional driving method is that if the number of rows of cells in the display is increased to improve the display resolution, less time is left available for driving the reset cells. The subfields have a fixed length determined by the television system and the number of levels on the intensity gradation scale. If the field rate is sixty hertz (60 Hz), for example, and there are two hundred fifty-six gradation levels, then each field must be divided into eight subfields having a duration of substantially two thousandths of a second (more precisely, 2.083 milliseconds) apiece. To ensure a stable discharge of the display cells, a certain minimum time must be allowed for the driving of each row. The maximum time available for driving the reset cells is therefore the fixed subfield duration, less the minimum row-driving period multiplied by the number of rows. Clearly, as the number of rows increases, the time available for driving the reset cells decreases. Eventually a point is reached at which the reset cells cannot be driven long enough to prime the first row of auxiliary cells adequately, causing the operation of the display to become unreliable.

SUMMARY OF THE INVENTION

It is accordingly an object of the present invention to provide adequate time for driving the reset cells in a DC plasma display panel.

The present invention provides a method of driving a DC plasma display panel of the type described above, having a row-column matrix of display cells and auxiliary cells, and a row of reset cells adjacent to the first row of auxiliary cells. The invented method belongs to the general class of methods in which, to enable different intensity gradations to be displayed, an image is displayed as a series of subfields, and in each subfield, the display cells and auxiliary cells are driven a row at a time in a sequence that starts from the first row. The invented method drives the reset cells during a part of the sequence in which the display cells and auxiliary cells in rows other than the first row are being driven. This part preferably occurs near the end of the sequence, and includes the time during which the display cells and auxiliary cells in the last row are being driven.

BRIEF DESCRIPTION OF THE DRAWINGS

An embodiment of the invention will be described with reference to the attached drawings, in which:

FIG. 1 is a cutaway perspective view of part of a DC plasma display panel;

FIG. 2 is a schematic diagram showing the electrical connections of the DC plasma display panel and its driving circuits;

FIG. 3 is a timing diagram illustrating the division of a field into subfields, and the driving of the reset cells according to the embodiment; and

FIG. 4 is a more detailed timing diagram illustrating the driving of auxiliary cells, display cells, and reset cells in the embodiment.

DETAILED DESCRIPTION OF THE INVENTION

The invention will be described by way of example through one embodiment, and some possible variations in this embodiment will be mentioned.

FIG. 1 illustrates a DC plasma display panel driven according to this embodiment, showing the matrix of display cells 11 and auxiliary cells 13 and single row of reset cells 15. The display cells 11 and auxiliary cells 13 overlie a plurality of display cathodes 17, which run parallel to one another in the row direction, while the reset cells 15 overlie a single reset cathode 19, which also runs in the row direction.

These cathodes are formed on a glass backplate 20. The display cells 11 are divided from one another, and from the auxiliary cells 13, by separators 21. The separators 21 define the display cells 11 individually, while an auxiliary cell 13 simply comprises a space between two separator walls, disposed between two display cells 11. A reset cell 15 comprises the space above the reset cathode 19 adjacent to an auxiliary cell 13 in the first row. There are two columns of display cells 11 for every column of auxiliary cells 13. The separators 21 have priming slits 23 that allow charged particles to diffuse from the auxiliary cells 13 into the adjacent display cells 11.

The display cells 11, auxiliary cells 13, and reset cells 15 are covered by a glass faceplate 30, on which are formed a plurality of display anodes 31 and auxiliary anodes 33. These anodes run in the column direction of the cell matrix. The backplate 20 and faceplate 30 are aligned so that the display anodes 31 run over the display cells 11, and the auxiliary anodes 33 run over the auxiliary cells 13.

A plurality of red phosphors 35, green phosphors 37, and blue phosphors 39 are formed on the faceplate 30 in locations such that the phosphors partly overlie corresponding display cells 11 without covering the display anodes 31. The phosphors comprise materials that emit red, green, and blue light when excited by ultraviolet radiation produced by discharges in the display cells 11.

The space between the backplate 20 and faceplate 30 is filled with, for example, a mixture of inert gases, and is sealed at the edges of the backplate 20 and faceplate 30 by a hermetic structure not shown in the drawings.

FIG. 2 is a schematic diagram of this DC plasma display panel and its driving circuits. The same reference numerals are used as in FIG. 1, with subscripts to distinguish different elements of the same type. For simplicity, FIG. 2 shows only part of the display panel, comprising four columns of display cells 11_{11} to 11_{M4}, two columns of auxiliary cells 13_{11} to 13_{M2}, two reset cells 15, four of M display cathodes 17_1 to 17_M, four display anodes 31_1 to 31_4, two auxiliary anodes 33_1 and 33_2, and the reset cathode 19. M is an integer representing the number of rows of display and auxiliary cells.

The display anodes 31_1 to 31_4 are coupled to a write pulse generator 40, which supplies positive voltage pulses individually to the display anodes. The reset cathode 19 is coupled to a reset pulse generator 50, which supplies negative voltage pulses to the reset cathode. The display cathodes 17_1 to 17_M are coupled to a scanning and sustaining pulse generator 60, which supplies negative voltage pulses individually to the display cathodes. The auxiliary anodes 33_1 and 33_2 are coupled to an auxiliary pulse generator 70, which supplies positive voltage pulses collectively to all of the auxiliary anodes.

The reset cells 15 are disposed both above the reset cathode 19 and below the auxiliary anodes 33_1 and 33_2, permitting electrical discharges to take place from the auxiliary anodes 33_1 and 33_2 to the reset cathode 19. These discharges prime the auxiliary cells 13_{11} and 13_{12} in the first row. Similar discharges in the auxiliary cells 13_{11} and 13_{12} in the first row, from the auxiliary anodes 33_1 and 33_2 to the first display cathode 17_1, prime the auxiliary cells 13_{21} and 13_{22} in the second row, and this process continues through the last row. The auxiliary cells in each row discharge when a negative scanning pulse is supplied to the display cathode in that row, this pulse being timed to coincide with a positive voltage pulse supplied to the auxiliary anodes 33_1 and 33_2.

The discharges in the auxiliary cells in a particular row prime the display cells in that row. If a positive writing pulse is simultaneously supplied to the display anode in a particular column, a discharge occurs in the display cell 11 in that particular row and column, igniting the display cell. Thereafter, the display cell can be held in the ignited state for a desired time by further negative sustaining pulses supplied to the display cathode, without requiring simultaneous display anode pulses.

FIG. 3 illustrates the invented method of driving the reset cathode 19 in relation to the driving of the display cathodes 17. The horizontal axis represents the duration of one displayed field, from time t_0 to time t_{16}, substantially 16.67 milliseconds if the field rate is sixty hertz. The field is divided into eight subfields SF_1 to SF_8. In each subfield, the M display cathodes 17 are driven in sequence from row 1 to row M. The number of sustaining pulses supplied to the display cathodes 17 is weighted in each subfield so that after ignition, the display is sustained for the longest time in subfield SF_1, and for the shortest time in subfield SF_8, as indicated by hatching.

The reset cathode 19 is driven during an interval of duration τ_r near the end of each subfield. The symbol V_r represents the height of the reset pulse, which thus goes from ground level to a level of $-V_r$ volts. Reset pulses occur in the interval t_1-t_2 in subfield SF_1, the interval t_3-t_4 in subfield SF_2, and in the intervals t_5-t_6, t_7-t_8, t_9-t_{10}, t_{11}-t_{12}, t_{13}-t_{14}, and t_{15}-t_{16} in subfields SF_3, SF_4, SF_5, SF_6, SF_7, and SF_8, respectively.

FIG. 4 shows in more detail the driving of the cathodes and anodes in subfield SF_1 and part of subfield SF_2. The horizontal axis indicates time, from a time T_1 at the beginning of subfield SF_1 to a time T_{20} in subfield SF_2.

The positive voltage pulses P_{sa} at the top of the diagram are applied to all of the auxiliary anodes 33. These pulses have a height V_{sa} of, for example, one hundred volts (100 V), and occur at intervals of, for example, four microseconds (4 μs), with a pulse width τ_{sa} shorter than this period. Pulses P_{sa} occur in intervals such as T_1-T_2, T_3-T_4, T_5-T_6, T_8-T_9, T_{10}-T_{11}, T_{12}-T_{13}, T_{14}-T_{15}, T_{16}-T_{17}, and T_{19}-T_{20}.

The display cathodes 17_1 to 17_M are driven with negative voltage pulses P_k having a height V_k of, for example, minus two hundred volts (-200 V) and a width τ_k substantially equal, for example, to the width τ_{sa} of the auxiliary anode pulses P_{sa}. The pulses shown are the scanning pulses; sustaining pulses are omitted for the sake of clarity. In each subfield, the display cathodes 17 in different rows are driven in a sequence from the display cathode 17_1 in the first row to the display cathode 17_M in the last row.

The reset cathode 19 is driven during part of this sequence, in a continuous interval from time T_7 to time T_{18}, including the time T_{16}-T_{17} during which the last row of display and auxiliary cells is driven. The height of the reset pulse is, for example, minus two hundred fifty volts (-250 V).

The three waveforms at the bottom of FIG. 4 illustrate discharge current in the first row of auxiliary cells 13 (waveform A_1), the last row of auxiliary cells 13 (waveform A_M), and the reset cells 15 (waveform R). The auxiliary cells 13 discharge whenever the display cathode 17 in the corresponding row is driven. The reset cells 15 discharge during all auxiliary anode pulses P_{sa} occurring in the interval τ_r in which the reset cathode 19 is driven, due to the potential difference $V_{sa} + V_r$ between the reset cathode 19 and the auxiliary anodes 33. That is, the reset cells 15 discharge during times T_8-T_9, T_{10}-T_{11}, T_{12}-T_{13}, T_{14}-T_{15}, and T_{16}-T_{17}, concurrent with the driving of the display and auxiliary cells in five consecutive rows from row M - 4 to row M.

The interval during which the reset cathode 19 is driven can be selected arbitrarily, and is not restricted by the driving of the display cathodes. The interval from T_7 to T_{18} shown in this embodiment is only one of many possible intervals. The reset cathode driving time should be long enough to have an adequate priming effect on the first row of auxiliary cells, without being so long as to shorten the life of the reset cells 15. With a field frequency of sixty hertz, if there are eight subfields and five hundred twelve display cathodes, which are driven at a rate of substantially one display cathode every four microseconds (4 μs), the reset cathode 19 is preferably driven for an interval in the range from one hundred to five hundred microseconds (100 μs to 500 μs) long. If necessary, the reset cathode 19 can be driven discontinuously, for two or more short intervals instead of one long interval. One of the intervals preferably overlaps the driving of the last row at time T_{16}-T_{17}, but this is not a strictly necessary condition, as long as the reset cathode 19 is driven for at least one interval near the end of each subfield.

More precisely, the reset cathode 19 should be driven for an interval closely preceding the start of each subfield. For example, when the DC plasma display panel is powered up, the reset cathode 19 should be driven before the first display cathode 17_1 is driven for the first time, to assure a correct display from the very first field.

The interval during which the reset cathode 19 is driven may extend right up to the beginning of each subfield, or even slightly overlap the beginning, provided this does not interfere with the driving of the display cells 11 in the first row.

The invented driving method thus offers complete freedom in the design of the reset cathode drive timing, and enables an adequate priming effect to be obtained regardless of the number of rows of cells or the minimum driving time of the display cells.

The invented driving system is applicable to both interlaced and progressive scanning systems, and to systems in which interlaced scanning is converted to progressive scanning. In an interlaced scanning system, although the display cells are activated in an interlaced manner, the display cathodes and auxiliary cells are driven progressively. The term subfield as used herein refers to a subdivision of the display duration of one image, regardless of whether the image constitutes one frame of a still picture, or one field or one frame of a moving picture.

The invented driving method is not restricted to the above-described scheme whereby sustaining pulses are supplied to the display cathodes, but applies to DC plasma display panels with other sustaining methods as well. Those skilled in the art will recognized that various further modifications to the embodiment described above are also possible.

Claims

1. A method of driving a DC plasma display panel having a row-column matrix of display cells (11) and auxiliary cells (13), with a row of reset cells (15) disposed adjacent a first row of said display cells and auxiliary cells, in which, to enable different intensity gradations to be displayed, an image is displayed as a series of subfields, and in each subfield, the display cells and auxiliary cells are driven a row at a time in a sequence that starts from said first row, comprising the step of:

   driving said reset cells (15) during a part of said sequence in which the display cells (11) and auxiliary cells (13) in rows other than said first row are being driven, thereby priming the auxiliary cells (13) in said first row.

2. The method of claim 1, wherein said sequence ends with the driving of a certain last row of said display cells (11) and auxiliary cells (13), said first row and said last row being disposed at opposite ends of said matrix, and the part of said sequence during which said reset cells (15) are driven includes a time during which the display cells and auxiliary cells in said last row are driven.

3. The method of claim 1, wherein said part of said sequence comprises a part during which the display cells (11) and auxiliary cells (13) in a plurality of said rows are driven.

4. The method of claim 3, wherein said part of said sequence comprises a part during which the display cells (11) and auxiliary cells (13) in a plurality of mutually consecutive rows are driven.

5. A DC plasma display panel having a row-column matrix of display cells (11) and auxiliary cells (13), with a row of reset cells (15) disposed adjacent a first row of said display cells and auxiliary cells, in which, to enable different intensity gradations to be displayed, an image is displayed as a series of subfields, and in each subfield, the display cells and auxiliary cells are driven a row at a time in a sequence that starts from said first row, comprising:

a reset pulse generator (50) for driving said reset cells (15) during a part of said sequence in which the display cells (11) and auxiliary cells (13) in rows other than said first row are being driven, thereby priming the auxiliary cells (13) in said first row.

6. The DC plasma display panel of claim 5, wherein said sequence ends with the driving of a certain last row of said display cells (11) and auxiliary cells (13), said first row and said last row being disposed at opposite ends of said matrix, and the part of said sequence during which said reset cells (15) are driven includes a time during which the display cells and auxiliary cells in said last row are driven.

7. The DC plasma display panel of claim 5, wherein said part of said sequence comprises a part during which the display cells (11) and auxiliary cells (13) in a plurality of said rows are driven.

8. The DC plasma display panel of claim 7, wherein said part of said sequence comprises a part during which the display cells (11) and auxiliary cells (13) in a plurality of mutually consecutive rows are driven.

FIG. 1

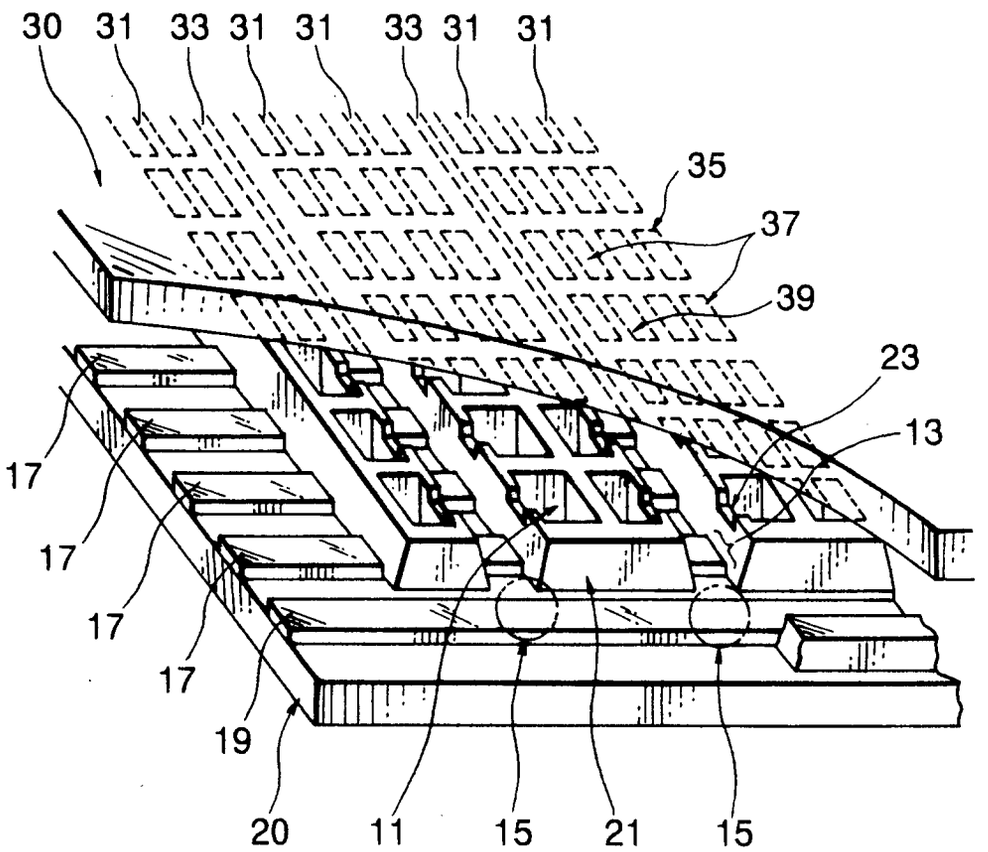


FIG. 2

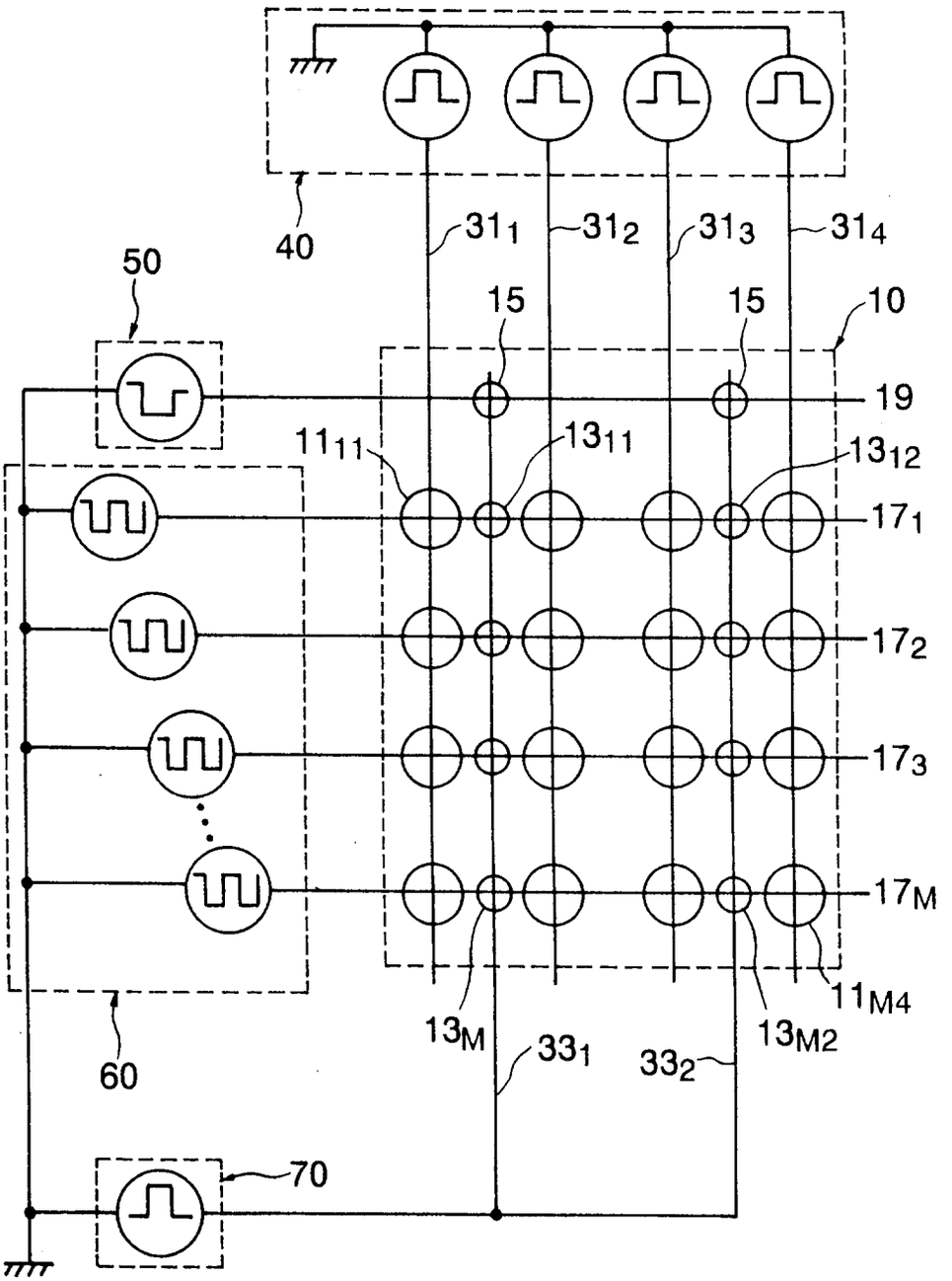

40
31_1
31_2
31_3
31_4
50
15
15
10
19
11_{11}
13_{11}
13_{12}
17_1
17_2
17_3
17_M
11_{M4}
13_M
33_1
33_2
13_{M2}
60
70

FIG. 3

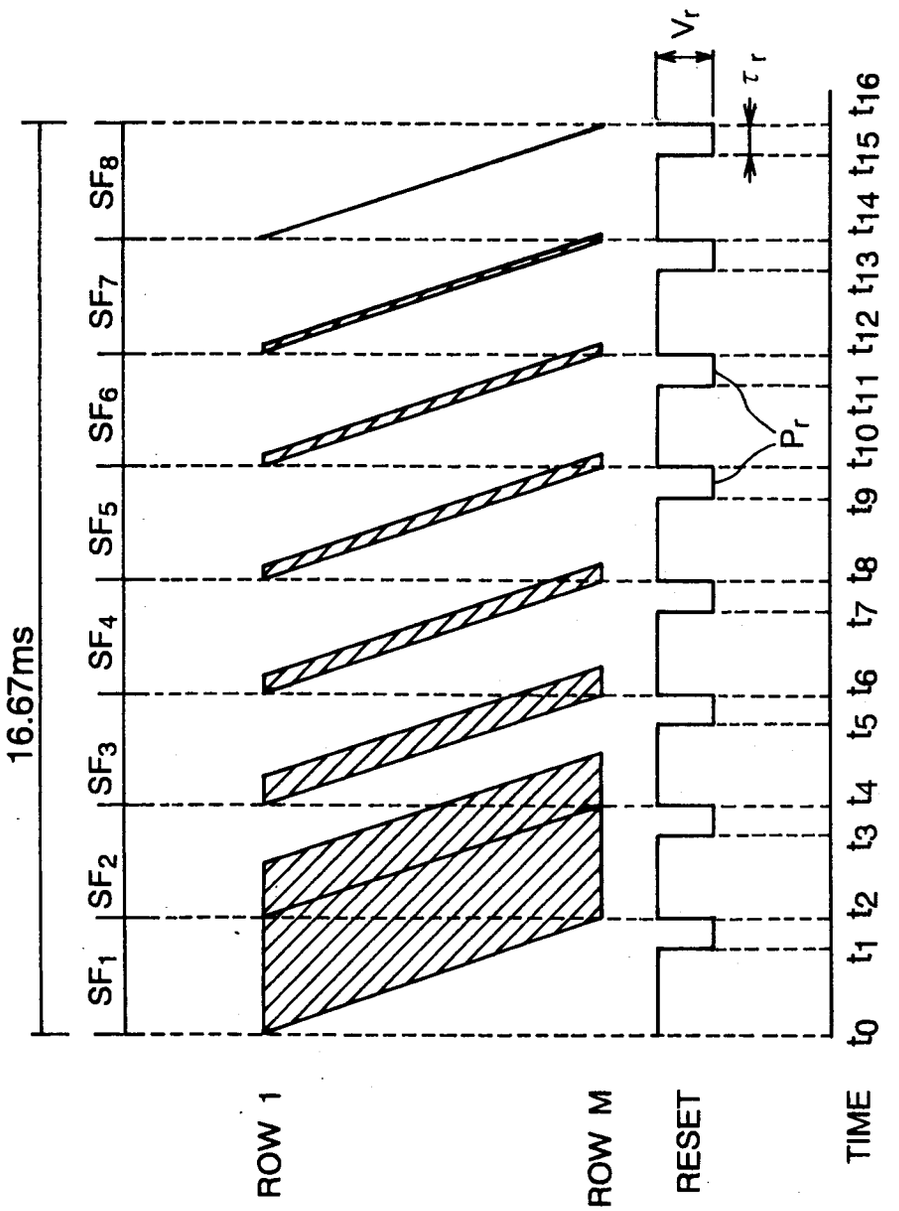
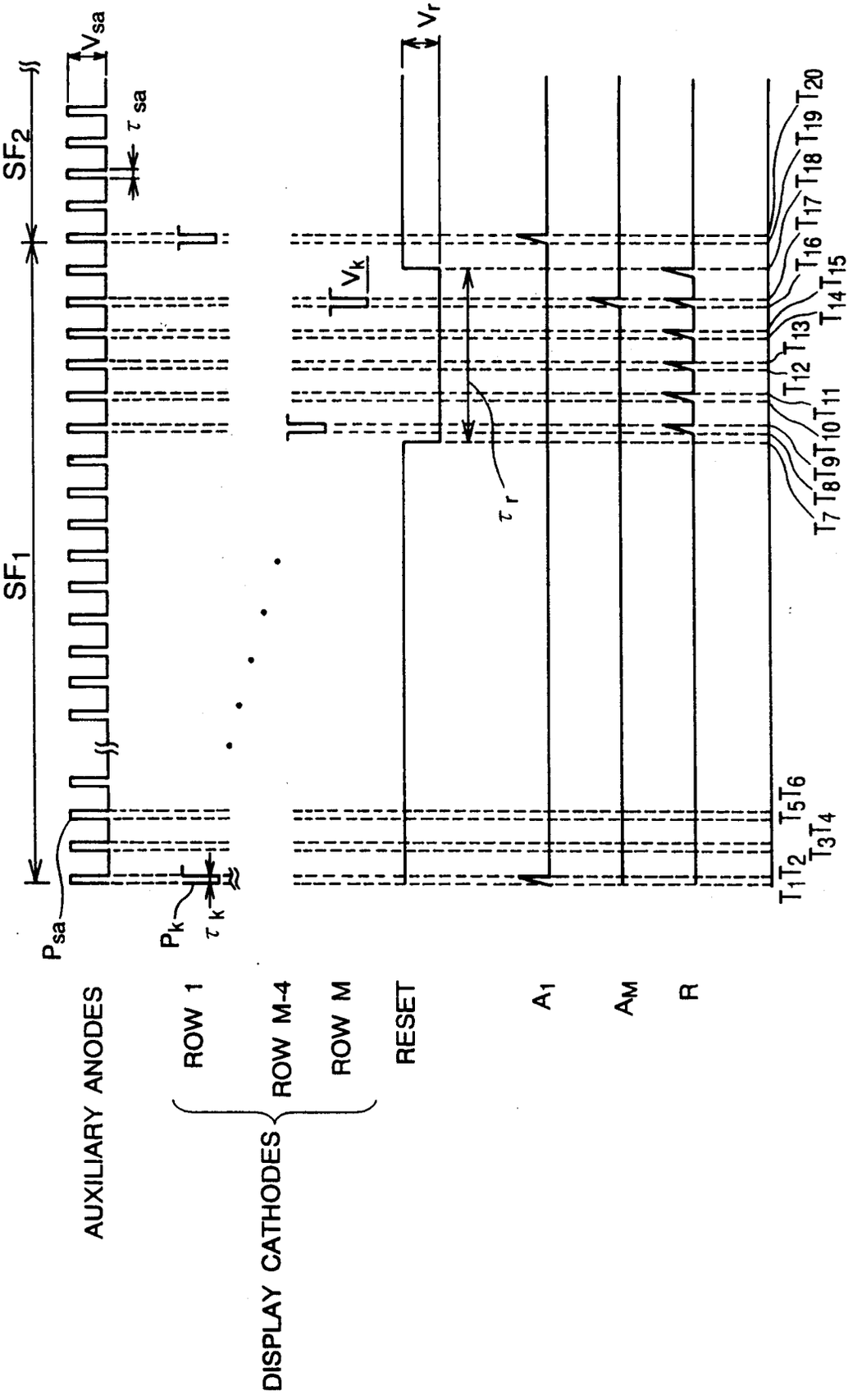

16.67ms
SF1
SF2
SF3
SF4
SF5
SF6
SF7
SF8
Vr
τr
Pr
t0 t1 t2 t3 t4 t5 t6 t7 t8 t9 t10 t11 t12 t13 t14 t15 t16
ROW 1
ROW M
RESET
TIME

FIG. 4


SF1
SF2
Vsa
τ sa
Vr
Vk
τ r
τ k
Psa
Pk
AUXILIARY ANODES
DISPLAY CATHODES
ROW 1
ROW M-4
ROW M
RESET
A1
AM
R
T1T2 T3T4 T5T6 T7 T8T9T10T11 T12 T13 T14T15 T16 T17 T18 T19 T20