(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 789 312 A1

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
13.08.1997 Bulletin 1997/33

(51) Int Cl.[6]: **G06G 7/12**

(21) Application number: **97300828.7**

(22) Date of filing: **07.02.1997**

(84) Designated Contracting States:
DE FR GB

(30) Priority: **08.02.1996 JP 22779/96**

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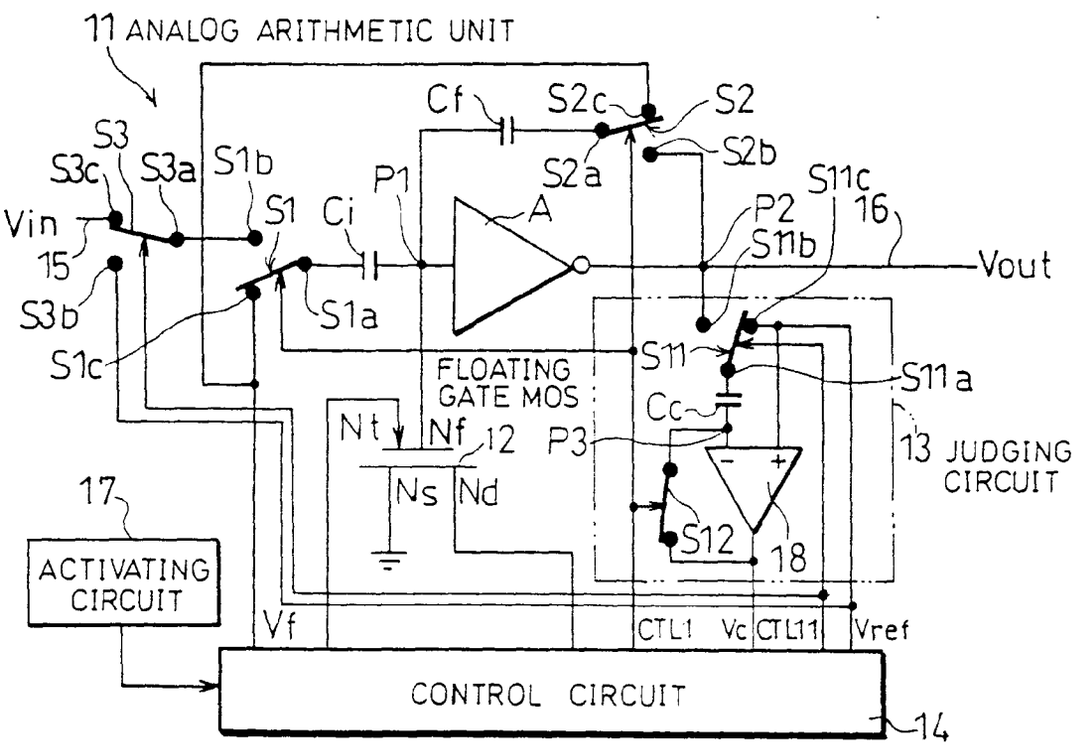
(54) Method of compensating offset voltage caused in analog arithmetic unit and analog arithmetic unit

(57) An analog arithmetic unit furnished with an input capacitor, an amplifier, a floating gate MOS. An input voltage is given to the amplifier through the input capacitor. The amplifier is composed of a CMOS inverter or the like and has a floating gate in a node at its input end. The floating gate MOS controls an amount of charges in the above node by injecting the hot electrons or absorbing the charges through the tunnel effect. Accordingly, it has become possible to maintain an amount of charges at the above node at a constant level over a long period. Thus, a frequency at which an offset voltage caused by charges accumulated at the above floating gate and causing an operation error can be reduced, thereby increasing an overall arithmetic operation.

FIG.1 (a)



EP 0 789 312 A1

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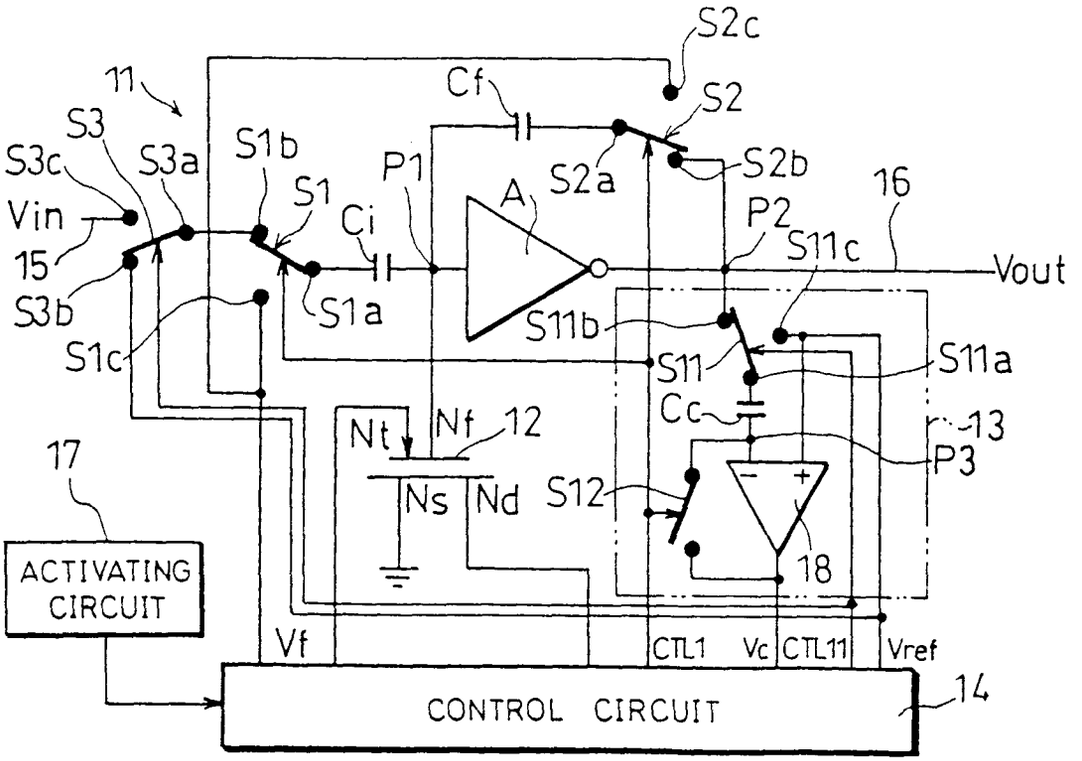
FIG.1 (b)


S2c
11
Cf
S2
S3
S3c
S3a
S1b
P1
S2a
S2b
16
Vin
S1
Ci
A
P2
S11c
15
Vout
S3b
S1a
S11b
S1c
S11
S11a
Cc
13
Nt
Nf
12
17
P3
Ns
Nd
S12
ACTIVATING CIRCUIT
18
Vf
CTL1
Vc
CTL11
Vref
CONTROL CIRCUIT
14

Description

FIELD OF THE INVENTION

The present invention relates to a method of compensating an offset voltage caused in an arithmetic unit furnished with an input capacitor and an amplifier and suitably used as a multiplying circuit, a sample hold circuit, or the like, and to an analog arithmetic unit having an offset voltage compensating function.

BACKGROUND OF THE INVENTION

There have been proposed diversified applications of an analog arithmetic unit for producing an analog or digital output by compressing or filtering an analog input signal through an arithmetic operation. Processing an analog input signal in advance using the analog arithmetic unit can reduce a job amount significantly in the following digital arithmetic operation.

Thus, the analog arithmetic unit is used suitably as a multiplying circuit for multiplying an analog output voltage from an image sensor by a predetermined coefficient as is disclosed, for example, in Japanese Patent Application No. 186766/1996 *(Tokukaihei No. 8-186766)* filed by the inventor of the present invention et al. The above analog arithmetic unit essentially includes an input capacitor and an amplifier, and another example analog arithmetic unit used as the multiplying circuit is disclosed in Japanese Laid-Open Patent Application No. 221503/1996 *(Tokukaihei No. 8-221503).*

Figure 9 is a block diagram depicting a structure of a conventional analog arithmetic unit 1. The analog arithmetic unit 1 comprises an amplifier A for an arithmetic operation, an input capacitor Ci and a feedback capacitor Cf, and a set of three switches S1-S3 and a control circuit 2 for compensating an offset voltage, which will be described below. The amplifier A can be realized by a CMOS (Complementary Metal Oxide Semiconductor) inverter or the like. The amplifier A referred hereinafter means an inverting amplifier composed of the CMOS inverter unless specified otherwise.

Here, let Vi be an input voltage to the amplifier A, Vo be an output voltage from the amplifier A, and G be a gain of the amplifier A, then input/output characteristics of the amplifier A are expressed as:

$$Vo-Vr=-G(Vi-Vr) \quad (1)$$

where Vr is an operating point voltage of the amplifier A, that is, an input voltage when Vo=Vi.

The following can be said as to a node P1 serving as an input end of the amplifier A in the above-structured analog arithmetic unit 1. That is, in the analog arithmetic unit 1, the input capacitor Ci is interposed between the node P1 and an input line 3, while the feedback capacitor Cf is interposed between the node P1 and an output line 4. Also, although it is not illustrated in the drawing, the gate of a MOSFET (Metal Oxide Semiconductor Field Effect Transistor) is provided in the input stage of the amplifier A. However, this arrangement causes the floating of the node P1. For this reason, an offset voltage is caused by charges accumulated at the node P1 when the analog arithmetic unit 1 is manufactured or actually run for an arithmetic operation later. The offset voltage varies with the change in physical properties of the device over years, temperatures, etc.

The switches S1-S3 and control circuit 2 are provided for compensating an offset voltage by removing the above charges. The switching of the switches S1 and S2 is controlled by a control signal CTL1 of Figure 10(a) from the control circuit 2, while the ON/OFF of the switch S3 is controlled by a control signal CTL2 of Figure 10(b) from the control circuit 2.

The switch S1 selectively connects a common contact point S1a connected to the input capacitor Ci to either an individual contact point S1b connected to the input line 3 or an individual contact point S1c to which a predetermined reference voltage Vref is given from the control circuit 2. The switch S2 selectively connects a common contact point S2a connected to the feedback capacitor Cf to either an individual contact point S2b connected to a node P2 serving as an output end of the amplifier A and the output line 4 or an individual contact point S2c to which the above reference voltage Vref is also given.

During a normal arithmetic operation, both the control signals CTL1 and CTL2 remain in a low level before a time t1 under the control of the control circuit 2. Therefore, as shown in Figure 9, the switch S1 connects the common contact point S1a and individual contact point S1b, and the switch S2 connects the common contact point S2a and individual contact point S2b, while the switch S3 goes off. As a result, the input capacitor Ci is provided at the input stage of the amplifier A, while the feedback capacitor Cf is interposed between the input and output of the amplifier A.

In contrast, during the offset voltage compensating operation, both the control signals CTL1 and CTL2 shift to a high level at the time t1 under the control of the control circuit 2. This turns on the switch S3, and upon which a voltage follower that directly connects the input and output ends of the amplifier A is formed. As a result, the charges accumulated at the node P1 are released into the output line 4 and eliminated therefrom. At the same time, the switches S1 and S2 connect the common contact point S1a and individual contact point S1c, and the common contact point S2a and individual contact point S2c, respectively.

The above reference voltage Vref can be any desired operating point voltage. For example, let a power source voltage of the amplifier A be Vdd, then the desired operating point voltage can be Vdd/2. Thus, the output of the amplifier A can be expressed as:

$$Vout=Vref+Vost \quad (2)$$

where Vout is an output voltage from the analog arithmetic unit 1 and Vost is an offset voltage.

Therefore, the reference voltage Vref is impressed respectively on the capacitors Ci and Cf at either end while a voltage Vref+Vost is impressed respectively on the capacitors Ci and Cf at the other end. Accordingly, charges corresponding to the offset voltage Vost, that is, charges which can compensate the offset voltage Vost, are accumulated at the capacitors Ci and Cf, respectively.

Subsequently, the switch S3 goes off when the control signal CTL2 shifts to the low level at a time t2, which causes the floating of the node P1. Then, when the control signal CTL1 shifts to the low level at a time t3, the switches S1 and S2 connect the common contact point S1a and individual contact point S1b, and the common contact point S2a and individual contact point S2b, respectively. As a result, the analog arithmetic unit 1 ends the compensation of the offset voltage and becomes ready for an arithmetic operation.

Let Vin be an input voltage, then the input/output characteristics of the analog arithmetic unit 1 after the offset voltage compensation ends are expressed as:

$$Vout-Vref=-(Ci/Cf)\ (Vin-Vref) \quad (3).$$

Herein, assume that a gain G of the amplifier A has a sufficiently large value and an input impedance of the same has an infinite value.

When the above-structured analog arithmetic unit 1 is manufactured as an integrated circuit, the switch S3 is formed as shown in Figure 11. To be more specific, the switch S3 includes a pair of transistors Q1 and Q2 of a CMOS structure and an inverting buffer B1.

Thus, even when the control signal CTL2 shifts to the low level and the switch S3 should completely go off, a slight leak current, such as a dark current, flows through the switch S3, thereby making it impossible to maintain an amount of charges at the node P1 to a level such that compensates the offset voltage over a long period. Thus, the offset voltage must be compensated frequently as was explained above, which slows down an overall arithmetic operation speed or complicates the structure of the control circuit 2.

Alternatively, an arrangement omitting the switch S3 and strictly regulating an amount of charges at the node P1 instead is proposed. This arrangement can eliminate the above problems caused by the switch S3; however, it is extremely difficult to control an amount of charges strictly when the analog arithmetic unit 1 is composed of an integrated circuit.

Further, since the operation characteristics of the analog arithmetic unit 1 vary at the time of manufacturing, the reference voltage Vref differs from a desired set value of Vref0. More specifically, let the input offset voltage Vost causing the above difference be defined as:

$$Vost=Vref-Vref0 \quad (4).$$

Then, a total amount of charges Q at the node P1 after the above offset voltage compensation is expressed as:

$$Q=Ci\cdot Vost \quad (5).$$

Thus, by taking the total amount of charges Q into account, the input/output characteristics expressed by Equation (3) above can be re-written as:

$$Vout-Vref$$

$$=-(Ci/Cf)\ (Vin-Vref)+(Ci/Cf)\ Vost \quad (6).$$

Therefore, (Ci/Cf)Vost causes an arithmetic operation error and makes the arithmetic operation less accurate.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a method of compensating an offset voltage caused in an analog arithmetic unit and an analog arithmetic unit which are capable of increasing the speed and accuracy of an arithmetic operation.

The above object is fulfilled by a method of compensating an offset voltage caused in an analog arithmetic unit composed of an input capacitor into which an input voltage is inputted and an amplifier having a floating gate connected to the input capacitor at an input end thereof, the method having a step of:

(a) controlling an amount of charges existing at the floating gate by at least one of injecting hot carriers and absorbing charges through a tunnel effect.

According to the above method, in the step (a), an amount of charges at the input end of the amplifier based on a computing result in response to a predetermined input is controlled by at least injecting the hot carriers or absorbing the charges through the tunnel effect. Controlling an amount of charges in the above manner makes it possible to compensate an offset voltage. Consequently, the charges at the floating gate can be maintained at a constant level in a stable manner over a long period without using a switch for shorting the input and output ends of the amplifier.

Thus, the offset voltage does not have to be compensated as frequently as was explained in the prior art column, thereby making it possible to increase the speed and accuracy of the arithmetic operation.

It is preferable to modify the above method of compensating an offset voltage to be further composed of a step of:

(b) judging an amount of the charges existing at the floating gate,

wherein,

the amount of the charges at the floating gate is controlled in such a manner to reduce an offset voltage

caused at the input end of the amplifier to zero based on a judging result in the step (b).

According to the above method, in the step (b), for example, a predetermined reference voltage or the like is inputted into the amplifier through the input capacitor, and an amount of charges is judged based on an output from the amplifier in response to the above input. In the step (a), an amount of charges is controlled based on the amount of charges judged in the step (b). Thus, it has become possible to control an amount of charges at the input end of the amplifier to be maintained at a desired level in a very accurate manner.

When a plurality of the analog arithmetic units are provided in parallel to have a plurality of input channels, an amount of charges in each amplifier is controlled to be equal only by injecting hot carriers in the step (a).

In this case, an amount of charges at the input end of each amplifier is controlled to be equal by injecting the hot carriers in the step (a). For example, to adjust an amount of charges to the level of an amplifier having the largest amount of charges, the hot carriers are injected into the other amplifiers to raise an amount of charges up to the above specific level. As a result, since the offset voltage at each amplifier is equalized, the operating accuracy of the amplifier in all the analog arithmetic units can be equalized as well. Thus, even when a plurality of the analog arithmetic units are provided in parallel, the offset voltage can be readily compensated.

Although, only the hot carriers are injected to control the amount of charges in the step (a), the charges may be absorbed through the tunnel effect to do the same. In this case, to adjust an amount of charges to the level of an amplifier having the smallest amount of charges, the charges are absorbed in the other amplifiers to reduce an amount of charges to the above specific level. Thus, like the above case of hot carrier injection, even when a plurality of the analog arithmetic units are provided in parallel, the offset voltage can be readily compensated.

Further, the step (b) may be combined with the step (a) to set a target value in controlling an amount of charges. This arrangement makes it possible to compensate the offset voltage in each analog arithmetic unit in an accurate manner.

Also, it is preferable that a differential amplifier, whose input offset voltage is compensated by a switched capacitor, is used to judge whether the offset voltage is compensated or not in the step (b). Here, the input offset voltage can be compensated, because the differential amplifier eliminates the charges accumulated at the input end thereof by means of the switched capacitor in advance. Thus, using the differential amplifier makes it possible to judge accurately whether an offset voltage caused in the amplifier is compensated or not.

It is further preferable that the above analog arithmetic unit whose offset voltage is compensated has a feedback capacitor to function as a multiplier. This arrangement makes it possible to compensate an offset voltage caused not only in a comparator having the input capacitor and amplifier, but also in a multiplier.

The above object is also fulfilled by an analog arithmetic unit furnished with:

an input capacitor into which an input voltage is inputted;

an amplifier having a floating gate at an input end thereof, the floating gate being connected to the input capacitor;

a charge adjusting element for adjusting charges existing at the floating gate by at least injecting hot carriers or absorbing charges through a tunnel effect; and

a control circuit for controlling the charge adjusting element to carry out a charge adjusting operation in such a manner to reduce an offset voltage caused at the input end of the amplifier to zero.

According to the above arrangement, an amount of charges at the input end of the amplifier based on an operation result in response to a predetermined input is adjusted by at least injecting the hot carriers or absorbing charges through the tunnel effect by means of the charge adjusting element. Since the charge adjusting operation is controlled by the control circuit to reduce the offset voltage to zero, the charges at the floating gate can be maintained at a constant level in a stable manner over a long period without using a switch for shorting the input and output ends of the amplifier.

Thus, the offset voltage does not have to be compensated as frequently as before, thereby making it possible to increase the speed and accuracy of the arithmetic operation.

It is preferable to modify the above analog arithmetic unit to be further furnished with a judging circuit for judging an amount of the charges existing at the floating gate, so that the control circuit controls the charge adjusting operation by the charge adjusting element based on a judging result by the judging circuit.

According to this arrangement, when the judging circuit judges an amount of charges in the same manner as the step (b) in the above method of compensating an offset voltage, the control circuit controls an amount of charges at the input end of the amplifier based on the judged amount of charges. Therefore, an amount of charges at the input end of the amplifier can be control-

led in a very accurate manner.

In addition, it is apparent that the analog arithmetic unit of the present invention can optionally adopt the arrangements, such as providing a plurality of the analog arithmetic units in parallel, enabling the analog arithmetic unit to function as a multiplier, and using the differential amplifier.

For a fuller understanding of the nature and advantages of the invention, reference should be made to the ensuing detailed description taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1(a) and 1(b) are block diagrams explaining an offset voltage compensating operation of an analog arithmetic unit in accordance with an example embodiment of the present invention;

Figure 2 is a block diagram explaining an arithmetic operation of the above analog arithmetic unit;

Figure 3 is a cross section schematically showing an example structure of a floating gate MOS in the above analog arithmetic unit;

Figures 4(a) through 4(c) are timing charts respectively explaining the offset voltage compensating operation of the above analog arithmetic unit;

Figure 5 is a flowchart detailing the offset voltage compensating operation of the above analog arithmetic unit;

Figure 6 is a block diagram depicting a structure of an analog arithmetic unit in accordance with another example embodiment of the present invention;

Figure 7 is a block diagram depicting a structure of an analog arithmetic unit in accordance with a further example embodiment of the present invention;

Figure 8 is a block diagram depicting a structure of analog arithmetic units of each embodiment of the present invention when connected in parallel;

Figure 9 is a block diagram depicting a typical structure of a conventional analog arithmetic unit;

Figures 10 (a) and 10 (b) are timing charts respectively explaining an offset voltage compensating operation of the analog arithmetic unit of Figure 9; and

Figure 11 is a circuit diagram depicting a structure of a switch provided in the analog arithmetic unit of Figure 9 for compensating an offset voltage.

DESCRIPTION OF THE EMBODIMENTS

Referring to Figures 1 through 5, the following description will describe an example embodiment of the present invention.

Figures 1(a) and 1(b) are block diagrams respectively explaining an offset voltage compensating operation of an analog arithmetic unit 11 in accordance with an example embodiment of the present invention. The analog arithmetic unit 11 is a multiplier comprising an amplifier A for an arithmetic operation, an input capacitor Ci, and a feedback capacitor Cf. To carry out the offset voltage compensation, which will be described below, the analog arithmetic unit 11 further comprises three switches S1, S2 and S3, a floating gate MOS 12, a judging circuit 13, a control circuit 14, and an activating circuit 17.

The amplifier A is realized by a CMOS inverter or the like. Thus, a node P1 of the amplifier A connected to the capacitors Ci and Cf and the floating gate of the CMOS inverter is a floating node. Hereinafter, the amplifier A is explained as an inverting amplifier composed of the CMOS inverter.

Both the switches S1 and S2 are controlled by a control signal CTL1 from the control circuit 14, while the switch S3 is controlled by a control signal CTL11 from the control circuit 14.

The switch S1 selectively connects a common contact point S1a connected to the input capacitor Ci to either an individual contact point S1b in an input line 15 side or an individual contact point S1c to which a pull-in voltage Vf is given from the control circuit 14. The switch S2 selectively connects a common contact point S2a connected to the feedback capacitor Cf to either an individual contact point S2b connected to a node P2 serving as an output end of the amplifier A or an individual contact point S2c to which the pull-in voltage Vf is also given. The input selecting switch S3 selectively connects a common contact point S3a connected to the above individual contact point S1b to either an individual contact point S3c connected to the input line 15 or an individual contact point S3b to which a reference voltage Vref, namely, the operating point voltage, is given from the control circuit 14.

An input voltage Vin to the input line 15 is given to the node P1 serving as an input end of the amplifier A through the switches S3 and S1 and input capacitor Ci. An output voltage Vout from the amplifier A is introduced into the output line 16, and also fed back to the node P1 through the switch S2 and feedback capacitor Cf.

Thus, as shown in Figure 2, during a normal arithmetic operation, the switch S1 connects the common contact point S1a and individual contact point S1b, while the switch S2 connects the common contact point S2a and individual contact point S2b. Further, the input selecting switch S3 connects the common contact point S3a and individual contact point S3c. Assembled under these conditions is a feedback amplifier whose input/output characteristics are expressed by Equation (1) above, where Vi is an input voltage, Vo is an output voltage, G is a gain, and Vr is an operating point voltage of the amplifier A.

The switches S1, S2, and S3 are provided for the above offset voltage compensation. During a charge controlling operation of the capacitors Ci and Cf of Figure 1(a), which will be explained below, the predetermined pull-in voltage Vf from the control circuit 14 is impressed respectively on the individual contact points S1c and S2c when the control signal CTL1 from the con-

trol circuit 14 shifts to the high level.

In contrast, during a judging operation of Figure 1 (b), which will be explained below, the switches S1 and S2 connect the common contact point S1a and individual contact point S1b, and the common contact point S2a and individual contact point S2b, respectively as is shown in Figure 2 when the control signal CTL1 shifts to the low level. Also, during the judging operation, the switch S3 connects the common contact point S3a and individual contact point S3b when the control signal CTL11 from the control circuit 14 shifts to the high level, which will be also described below. As a result, the reference voltage Vref is impressed on the input capacitor Ci.

In connection with the above-structured amplifier A, the floating gate MOS 12, which will be described below, and the control circuit 14 for controlling the same are provided in the present embodiment. This arrangement makes it possible to control the charges at the node P1 causing the offset voltage Vost expressed by Equation (2) above while the node P1 remains in the floating state.

A floating node Nf of the floating gate MOS 12 is connected to the node P1 and nodes Nd and Nt are connected to the control circuit 14, while a node Ns is grounded. Hereinafter, the term "charges" means negative charges unless otherwise specified. Thus, the term "hot carriers" in claims is equivalent to the term "hot electrons" used in the following description.

The input/output characteristics of the analog arithmetic unit 11 of Figure 2 during the arithmetic operation are given by:

$$\text{Vout-Vref} = -(1/Cf)\{Ci(Vin-Vref)+Q-(Ci+Cf)Vost\} \quad (7)$$

where Q is an amount of charges accumulated at the node P1, Vost is an input offset to the amplifier A, and Vr is an operating point voltage of the same. Hence, the offset voltage Vost is defined as:

$$Vost=Vr-Vref \quad (8).$$

Thus, making Q as:

$$Q=(Ci+Cf)Vost \quad (9)$$

makes it possible to accumulate charges at the node P1 to a level such that compensates the offset voltage Vost. Accordingly, it is understood that an accurate arithmetic operation will be possible under the above conditions, and the present embodiment is based on such understanding.

Figure 3 is a cross section schematically showing an example structure of the floating gate MOS 12. Broadly speaking, the floating gate MOS 12 comprises a p-substrate 21, on which a p-base region 22 is formed. Further, a floating gate 23 for injecting hot electrons is formed within the p-based region 22. Also, a floating gate 25 for absorbing charges through the tunnel effect is formed over an n-well region 24. The floating gates 23 and 25 are electrically connected to each other through a connecting line 26.

In the p-base region 22, two n^+ regions are provided spaced apart from each other: one is an n^+ region 31 connected to the grounded node Ns, and the other is an n^+ region 32 connected to the node Nd, which is connected to the control circuit 14 for controlling an inject amount of hot electrons. The floating gate 23 is formed through a gate oxide film 33 over the channel region between the n^+ regions 31 and 32. Also, two control gates 34 and 35 are provided over the floating gate 23 to be capacitive coupled with the same, respectively. The control gates 34 and 35 are connected to the input capacitor Ci and feedback capacitor Cf, respectively.

Further, in the n-well region 24, the floating gate 25 is formed through a gate oxide film 36, and an n^+ region 37 is formed adjacent to the floating gate 25. Also, a control gate 38 is provided over the floating gate 25 to be capacitive coupled with the same. The control gate 38 is connected to an input terminal of the amplifier A serving as the floating gate.

The n^+ region 37 is formed in the p-substrate 21 through the n-well region 24 to improve voltage withstanding. The node Nt, connected to the control circuit 14 for controlling a tunnel current, is connected to the n^+ region 37.

The control circuit 14 controls the charge control operation of the floating gates 23 and 25 of the above-structured floating gate MOS 12 in the following manner with reference to a judging result of the judging circuit 13, which will be described below. The p-base region 22 is made of a p-type semiconductor having an impurity density of, for example, approximately $10^{17}/cm^3$, and each of gate oxide films 33 and 36 is, for example, approximately 100Å thick. According to this arrangement, a threshold voltage of the floating gate MOS 12 becomes approximately 6V.

The control circuit 14 gives 5V to the node Nd when injecting the hot electrons into the floating gate 23. At the same time, the control circuit 14 controls the switch S1 to connect the common contact point S1a and individual contact point S1c and the switch S2 to connect the common contact point S2a and individual contact point S2c as previously mentioned. Thus, the pull-in voltage Vf of, for example, 6V, is impressed on each of the nodes Nf1 and Nf2 respectively from the capacitors Ci and Cf through the control gates 34 and 35, respectively. Thus, the hot electrons absorbed by the voltage impressed on the node Nd pass through the gate oxide film 33, and are injected into the floating gate 23 by the pull-in voltage Vf impressed from the nodes Nf1 and Nf2.

In contrast, when absorbing the charges at the float-

ing gate 25, the control circuit 14 raises the potential of the node Nt, so that it will be higher than the potential of the floating gate 25 by 30-40V. Accordingly, a current developed through the tunnel effct at the floating gate 25 passes through the gate oxide film 36 and flows into the n^+ region 37. This arrangement makes it possible to control an amount of charges at the floating gates 23 and 25 to be maintained at a desired level.

On the other hand, the judging circuit 13 is provided for judging an effect of the offset voltage compensation by the above charge control operation. Thus, the judging circuit 13 compares an output voltage Vout from the analog arithmetic unit 11, namely a voltage at the node P2, with the predetermined reference voltage Vref.

The judging circuit 13 comprises a differential amplifier 18, an input capacitor Cc, and two switches S11 and S12. Either the output voltage Vout from the amplifier A or the reference voltage Vref from the control circuit 14 is selectively inputted into an inverting input terminal of the differential amplifier 18 through the input capacitor Cc and switch S11.

Thus, the switch S11 comprises a common contact point S11a connected to the input capacitor Cc, an individual contact point S11b connected to the node P2, and an individual contact point S11c to which the reference voltage Vref is given. The switch 11 connects the common contact point S11a and individual contact point S11c when the control signal CTL11 is in the low level, and connects the common contact point S11a and individual contact point S11b when the control signal CTL11 shifts to the high level. Note that the reference voltage Vref is also inputted into the other non-inverting input terminal of the differential amplifier 18.

The switch S12 is interposed between the inverting input terminal and output terminal of the differential amplifier 18. The switch S12 stays off when the control signal CTL1 is in the low level, and comes on when the control signal CTL1 shifts to the high level. Thus, the input capacitor Cc serves as a switched capacitor.

The judging circuit 13 comes into a self-compensating mode by disconnecting the switch S11 from the node P2 during the charge control operation of Figure 1(a) to compensate its own offset voltage. Herein, an output from the differential amplifier 18 is fed back either terminal of the input capacitor Cc and the inverting input terminal of the differential amplifier 18, and the reference voltage Vref is impressed on the other terminal and the non-inverting input terminal of the differential amplifier 18. Thus, in the self-compensating mode, a voltage at a node P3, namely, the inverting input terminal of the differential amplifier 18, is expressed as: Vref+Vosta, where Vosta is an input offset voltage of the differential amplifier 18.

When the switch 12 goes off as shown in Figure 1 (b) under these conditions, the charges, Vosta·Cc, corresponding to the input offset voltage Vosta of the differential amplifier 18 remain at the node P3.

After the offset compensation is carried out in the above manner, an input voltage to the inverting input terminal of the differential amplifier 18 during the judging operation of Figure 1(b) is expressed as: Vout+Vosta. Thus, the output voltage Vout of the amplifier A is inputted after the offset voltage Vosta of the differential amplifier 18 is compensated by the input capacitor Cc. This enables the differential amplifier 18 to judge whether the output voltage Vout is equal to or above the reference voltage Vref or not accurately. Accordingly, the differential amplifier 18 outputs a high-level output Vc when the output voltage Vout is equal to or above the reference voltage Vref, and a low-level output Vc when the output voltage Vout is below the reference voltage Vref.

The control circuit 14 comprises a logic circuit composed of, for example, a CMOS element. The control circuit 14 judges that charges are accumulated respectively in the capacitors Ci and Cf to a desired level such that compensates the offset voltage of the amplifier A when the output Vc from the differential amplifier 18 is inverted. Based on the above judgment, the control circuit 14 ends the charge control operation of Figure 1(a) and judging operation of Figure 1(b), so that the analog arithmetic unit 11 can proceed to a normal arithmetic operation of Figure 2.

An activating circuit 17 is provided in connection with the control circuit 14. The activating circuit 17 activates the control circuit 14 to carry out the above offset voltage compensation operation composed of the charge control operation and the judging operation upon detecting the power-up of the analog arithmetic unit 11.

Figure 4 shows timing charts explaining the offset voltage compensating operation of the control circuit 14. As is shown in Figure 4(a), when the power source is turned on at a time t11, the control circuit 14 is activated by the activating circuit 17. To begin with, the control circuit 14 outputs a low-level control signal CTL1 of Figure 4(b) and a high-level control signal CTL11 of Figure 4(c) to carry out the judging operation. As shown in Figure 1(b), under the control of the low-level control signal CTL1, the switches S1 and S2 respectively connect the common contact point S1a and individual contact point S1b, and the common contact point S2a and individual contact point S2b while the switch S12 goes off. On the other hand, under the control of the high-level control signal CTL11, the switches S3 and S11 connect the common contact point S3a and individual contact point S3b, and the common contact point S11a and individual contact point S11b, respectively.

Next, based on the judging result, the control circuit 14 determines whether the hot electrons should be injected or the charges should be absorbed during the charge control operation. Then, at a time t12, the control circuit 14 outputs a high-level control signal CTL1 and a low-level control signal CTL11 to carry out the charge control operation. As shown in Figure 1(a), under the control of the high-level control signal CTL1, the switches S1 and S2 respectively connect the common contact point S1a and individual contact point S1c, and the com-

mon contact point S2a and the individual contact point S2c while the switch S12 comes on. On the other hand, under the control of the low-level control signal CTL11, the switch 11 connects the common contact point S11a and individual contact point S11c.

At a time t13, the charge control on the node P1 starts when a predetermined number of pulses for a certain inject amount or absorption amount are outputted to the node Nd and Nt, and after which the control circuit 14 carries out the judging operation again. When the injection of the hot electrons or absorbing of the charges turns out insufficient from the judging result, the charge control operation and judging operation carried out at times t12-t14 are repeated at a time t14 and beyond.

In this manner, an amount of charges at the node P1 reaches a desired level such that compensates the offset voltage at a time t15, upon which the control circuit 14 outputs the low-level control signals CTL1 and CTL11 and sets the analog arithmetic unit 11 to a ready mode for a normal arithmetic operation of Figure 2.

Figure 5 is a flowchart detailing the above offset voltage compensating operation. When the power source of the analog arithmetic unit 11 is turned on, the control circuit 14 is activated by the activating circuit 17, and the operation proceeds to Step m1. In Step m1, the control signal CTL1 is shifted to the low level while the control signal CTL11 is shifted to the high level at the time t11 to enable the control circuit 14 to start the judging operation and check whether the charges at the node P1 are insufficient or not. When the charges are insufficient, the potential at the node P1, that is, an input voltage Vi to the amplifier A, rises and an output voltage Vo from the amplifier A decreases in turn. This reduces the potential of the inverting input lower than the potential of the other non-inverting input in the differential amplifier 18, thereby shifting the output Vc to the high level.

Upon the judgment of insufficient charges in Step m1, the flow proceeds to Step m2, where the hot electrons are injected into by the floating gate MOS 12 at the time t12. Then, whether the charges are insufficient or not is judged again at the time t13 in Step m3. When the charges are still insufficient, the flow returns to Step m2, and the hot electrons are injected again at the time t14. When the charges are judged to be sufficient in Step m3, a normal arithmetic operation is started at the time t15 in Step m4.

On the other hand, when the charges are judged to be sufficient in Step m1, the flow proceeds to Step m5, where the charges are absorbed at the time t12 by the floating gate MOS 12 (charge control operation). Then, in Step m6, the result of the charge control operation in preceding Step m5 is judged at the time t13. When there are excessive charges, the flow returns to Step m5 at the time t14, so that the charges are absorbed again. When the charges are judged to be insufficient in Step m6, the charge control operation is stopped at the time t15 and the flow proceeds to Step m4.

As has been explained, the analog arithmetic unit 11 of the present invention controls an amount of charges at the node P1, which is in effect the input end of the amplifier A serving as the floating gate. Thus, the analog arithmetic unit 11 of the present invention can accurately compensate the charge accumulation at the node P1 and a displacement (offset voltage Vost) from the reference voltage Vref caused by variance in operation characteristics at the time of manufacturing.

Also, to control an amount of charges at the node P1, the analog arithmetic unit 11 of the present invention employs the floating gate MOS 12 instead of mechanism, such as the switch S3 (see Figure 11), that causes a leak current. Thus, it has become possible to maintain an amount of charges at the node P1 at a level such that compensates the offset voltage Vost over a long period. As a result, since the offset voltage Vost does not have to be compensated as frequently as before, not only an overall arithmetic operation speed is increased, but also the structure of the control circuit 14 can be simplified.

Further, the offset voltage compensating operation is started by the activating circuit 17 upon detection of the power-up. Thus, the arithmetic operation can be carried out accurately while the offset voltage is compensated from the beginning to end without any suspension.

To activate the offset voltage compensating operation periodically, the activating mechanism demands, for example, a timing circuit for activating the above operation at every scheduled timing, which undesirably complicates the structure. In contrast, the analog arithmetic unit 11 of the present embodiment carries out the compensation operation when the power is turned on, it does not demand any timing circuit, thereby making it possible to simplify the control circuit 14 and activating mechanism.

Referring to Figure 6, the following description will describe another example embodiment of the present invention.

Figure 6 is a block diagram depicting a structure of an analog arithmetic unit 41 in accordance with another example embodiment of the present invention. Hereinafter, like components in the analog arithmetic unit 41 are labeled with like reference numerals with respect to the above analog arithmetic unit 11, and the description of these components is not repeated for the explanation's convenience.

It should be noted that the amplifier A in the analog arithmetic unit 41 is incorporated into an integrated circuit 42 together with the capacitors Ci and Cf, switches S1, S2, and S3, floating gate MOS 12, and judging circuit 13, and that a control circuit 43 is an outboard device to the integrated circuit 42. The control circuit 43 having the identical functions as those of the control circuit 14 is connected to the finished integrated circuit 42, and disconnected after the above-mentioned charge control and judging operations for the offset voltage compensation are carried out. In addition, the integrated circuit 42 is mounted on a lead frame and packaged in resin or the like.

Disconnecting the control circuit 43 from the chip of the integrated circuit 42 can reduce both the circuit space and chip cost. This arrangement is advantageous in maintaining the accumulated charges at the floating gates 23 and 25 at a constant level over a long period by controlling the thickness of the gate oxide films 33 and 36 after the analog arithmetic unit 41 is manufactured. Since it is no longer necessary to form the control circuit 43, which has nothing to do with the arithmetic operation, on the chip of the integrated circuit 42, the integrated circuit 42 can be readily downsized while saving the manufacturing cost.

Referring to Figure 7, the following description will describe a further example embodiment of the present invention.

Figure 7 is a block diagram depicting a structure of an analog arithmetic unit 51 in accordance with a further example embodiment of the present invention. Hereinafter, like components in the analog arithmetic unit 51 are labeled with like reference numerals with respect to the above analog arithmetic units 11 and 41, and the description of these components is not repeated for the explanation's convenience.

It should be noted that the analog arithmetic unit 51 omits the feedback capacitor Cf in the above embodiments, and that the analog arithmetic unit 51 per se serves as a comparator. To be more specific, during the offset voltage compensating operation, the switch S1 connects the common contact point S1a and individual contact point S1c under the control of the control circuit 14. Accordingly, the pull-in voltage Vf is impressed on the node Nf of the floating gate MOS 12 through the input capacitor Ci to inject the hot electrons, or the potential of the node Nt rises to absorb the charges through the tunnel effect.

Also, during the judging operation, the switch S1 connects the common contact point S1a and individual contact point S1b and the switch S3 connects the common contact point S3a and individual contact point S3b under the control of the control circuit 14. Accordingly, the control circuit 14 impresses the reference voltage Vref on the input capacitor Ci, and monitors the output Vc from the judging circuit 13 under these conditions. The control circuit 14 carries on the above offset voltage compensating operation and charge control operation until the output Vc from the judging circuit 13 inverts. Thus, an amount of charges in the node P1 when the offset voltage compensation ends is zero (0).

Thus, after the offset voltage compensation, the analog arithmetic unit 51 can judge whether the input voltage Vin is equal to or above the reference voltage Vref or not accurately. The output voltage Vout conveying the judging result shifts to the low level when $Vin \geq Vref$, and shifts to the high level when $Vin < Vref$.

As has been explained, the present invention can be suitably adopted to a structure where the input end of the amplifier A serves as the floating gate. The present invention is particularly advantageous when a plurality of each of the analog arithmetic units 11, 41, and 51 are used in parallel, respectively. In this case, as is illustrated in Figure 8, if a multiplexer 61 is used, the control circuits 14 or 43 and the judging circuit 13 can be shared by the plurality of the analog arithmetic units. According to this arrangement, a plurality of arithmetic circuits 62, each of which is the analog arithmetic unit 11, 41, or 51 omitting the control circuit 14 or 43, judging circuit 13, and activating circuit 17, are connected in parallel.

Also, in this case, an amount of charges at the node P1 does not have to be zero (0) as long as the node P1 in each analog arithmetic unit has an equal amount of charges. That is to say, the above arrangement can be realized when the offset voltage Vost in each analog arithmetic unit is equal. To be more specific, the hot electrons are injected into or the charges are absorbed from the analog arithmetic units to adjust an amount of charges thereof to the largest or smallest amount among all the analog arithmetic units. Thus, the offset voltage of each analog arithmetic unit can be compensated by either injecting the hot electrons or absorbing the charges. This facilitates the offset voltage compensation.

Note that the amplifier A is not limited to the inverting amplifier as was disclosed in the above, and the same can be any other type of amplifiers having the input end serving as the floating gate, such as a differential amplifier. The judging circuit 13 is arranged to judge whether the output voltage Vout is equal to or above the reference voltage Vref herein. However, the same can be arranged to introduce an output corresponding to a balance between the output voltage Vout and reference voltage Vref. Accordingly, the control circuit 14 can be arranged to inject the hot electrons or absorb the charges through the tunnel effect for a number of times corresponding to the output level from the differential amplifier 18.

In addition, the judging circuit 13 of the present invention is arranged to detect that an amount of charges at the node P1 reaches an optimal level when the output Vc from the differential amplifier 18 inverts. However, the same can be composed of a so-called window comparator, having two differential amplifiers into which two reference voltages $Vref+\Delta V$ and $Vref-\Delta V$ are respectively inputted. In this case, the control circuit judges the end of the charge control by converging the output voltage Vout into a range between $Vref+\Delta V$ and $Vref-\Delta V$.

Further, the floating gate MOS 12 can be arranged to have conductivity in a polarity opposite to the polarity shown in Figure 3. In this case, hot holes are injected into the floating gate 23 as hot carriers, so that positive charges are absorbed in the floating gate 25.

The invention being thus described, it will be obvious that the same may be varied in many ways. Such variations are not to be regarded as a departure from the spirit and scope of the invention, and all such modifications as would be obvious to one skilled in the art are intended to be included within the scope of the fol-

lowing claims.

Claims

1. A method of compensating an offset voltage caused in an analog arithmetic unit comprising an input capacitor into which an input voltage is inputted and an amplifier having a floating gate connected to said input capacitor at an input end thereof, said method comprising a step of:

   (a) controlling an amount of charges existing at said floating gate by at least one of injecting hot carriers and absorbing charges through a tunnel effect.

2. The method of compensating an offset voltage as defined in Claim 1 further comprising a step of:

   (b) judging an amount of said charges existing at said floating gate,

   wherein,

   in said step (a), the amount of said charges at said floating gate is controlled in such a manner to reduce an offset voltage caused at the input end of said amplifier to zero based on a judging result in said step (b).

3. The method of compensating an offset voltage as defined in Claim 2, wherein a differential amplifier, whose input offset voltage is compensated by a switched capacitor, is used to judge whether said offset voltage is compensated or not in said step (b).

4. The method of compensating an offset voltage as defined in Claim 2, wherein:

   said step (a) is carried out by a control circuit, said control circuit being connected to an integrated circuit, into which said input capacitor, amplifier, and a charge adjusting element for adjusting an amount of said charges are incorporated, to control an operation of said charge adjusting element; and

   said method further comprises a step of:

   (c) packaging said integrated circuit after disconnecting said control circuit from said integrated circuit when said offset voltage is compensated.

5. The method of compensating an offset voltage as defined in Claim 2, wherein said analog arithmetic unit includes a feedback capacitor connected across an input end and an output end of said amplifier to function as a multiplier.

6. The method of compensating an offset voltage as defined in Claim 1, wherein, when a plurality of said analog arithmetic units are provided in parallel, an amount of charges in said each amplifier is controlled to be equal only by injecting hot carriers in said step (a).

7. The method of compensating an offset voltage as defined in Claim 6 further comprising a step of:

   (b) judging an amount of said charges existing at said floating gate of said each amplifier,

   so that, in said step (a), the amount of said charges is controlled in such a manner to equalize an offset voltage caused at an input end of said each amplifier based on a judging result of said step (b).

8. The method of compensating an offset voltage as defined in Claim 7, wherein a differential amplifier, whose input offset voltage is compensated by a switched capacitor, is used to judge whether said offset voltage is compensated or not in said step (b).

9. The method of compensating an offset voltage as defined in Claim 7, wherein:

   said step (a) is carried out by a control circuit, said control circuit being connected to an integrated circuit, into which said input capacitor, amplifier, and a charge adjusting element for adjusting an amount of said charges are incorporated, to control an operation of said charge adjusting element; and

   said method further comprises a step of:

   (c) packaging said integrated circuit after disconnecting said control circuit from said integrated circuit when said offset voltage is compensated.

10. The method of compensating an offset voltage as defined in Claim 7, wherein said analog arithmetic unit includes a feedback capacitor connected across an input end and an output end of said amplifier to function as a multiplier.

11. The method of compensating an offset voltage as defined in Claim 1, wherein, in said step (a), when a plurality of said analog arithmetic units are provided in parallel, an amount of charges in said each amplifier is controlled to be equal only by absorbing charges through a tunnel effect.

12. The method of compensating an offset voltage as defined in Claim 11 further comprising a step of:

   (b) judging an amount of said charges existing at said floating gate of said each amplifier,

   so that, in said step (a), the amount of said charges is controlled in such a manner to equalize an offset voltage caused at an input end of

said each amplifier based on a judging result of said step (b).

13. The method of compensating an offset voltage as defined in Claim 12, wherein a differential amplifier, whose input offset voltage is compensated by a switched capacitor, is used to judge whether said offset voltage is compensated or not in said step (b).

14. The method of compensating an offset voltage as defined in Claim 12, wherein:

said step (a) is carried out by a control circuit, said control circuit being connected to an integrated circuit, into which said input capacitor, amplifier, and a charge adjusting element for adjusting an amount of said charges are incorporated, to control an operation of said charge adjusting element; and
said method further comprises a step of:
(c) packaging said integrated circuit after disconnecting said control circuit from said integrated circuit when said offset voltage is compensated.

15. The method of compensating an offset voltage as defined in Claim 12, wherein said analog arithmetic unit includes a feedback capacitor connected across an input end and an output end of said amplifier to function as a multiplier.

16. An analog arithmetic unit comprising:

an input capacitor into which an input voltage is inputted;
an amplifier having a floating gate at an input end thereof, said floating gate being connected to said input capacitor;
a charge adjusting element for adjusting charges existing at said floating gate by at least injecting hot carriers or absorbing charges through a tunnel effect; and
a control circuit for controlling said charge adjusting element to carry out a charge adjusting operation in such a manner to reduce an offset voltage caused at the input end of said amplifier to zero.

17. The analog arithmetic unit as defined in Claim 16 further comprising a judging circuit for judging an amount of said charges existing at said floating gate, so that said control circuit controls said charge adjusting operation by said charge adjusting element based on a judging result by said judging circuit.

18. The analog arithmetic unit as defined in Claim 17, wherein said judging circuit includes a differential amplifier for compensating an input offset voltage by a switched capacitor to judge whether said input offset voltage is compensated or not.

19. The analog arithmetic unit as defined in Claim 17, wherein:

said input capacitor, amplifier, charge adjusting element are incorporated into an integrated circuit; and
said control circuit is made attachable to and detachable from said integrated circuit.

20. The analog arithmetic unit as defined in Claim 17 further comprising a feedback capacitor connected across an input end and an output end of said amplifier to function as a multiplier.

21. The analog arithmetic unit as defined in Claim 16 further comprising an activating circuit for activating said control circuit to carry out an offset compensating operation upon detection of power-up of said analog arithmetic unit.

22. The analog arithmetic unit as defined in Claim 16, wherein said charge adjusting element is a floating gate MOS having a floating gate connected to said floating gate of said amplifier.

23. The analog arithmetic unit as defined in Claim 16, a plurality of said analog arithmetic units being provided in parallel,
wherein said control circuit in said each analog arithmetic unit controls its own charge adjusting operation using its own charge adjusting element only by injecting hot carriers to equalize an offset voltage of said each amplifier.

24. The analog arithmetic unit as defined in Claim 23 further comprising a judging circuit for judging an amount of said charges existing at said floating gate, so that said control circuit controls said charge adjusting operation by said charge adjusting element based on a judging result by said judging circuit.

25. The analog arithmetic unit as defined in Claim 24, wherein said judging circuit includes a differential amplifier for compensating an input offset voltage by a switched capacitor to judge whether said input offset voltage is compensated or not.

26. The analog arithmetic unit as defined in Claim 24, wherein:

said input capacitor, amplifier, charge adjusting element are incorporated into an integrated circuit; and

said control circuit is made attachable to and detachable from said integrated circuit.

27. The analog arithmetic unit as defined in Claim 24 further comprising a feedback capacitor connected across an input end and an output end of said amplifier to function as a multiplier.

28. The analog arithmetic unit as defined in Claim 23 further comprising an activating circuit for activating said control circuit to carry out an offset compensating operation upon detection of power-up of said analog arithmetic unit.

29. The analog arithmetic unit as defined in Claim 23, wherein said charge adjusting element is a floating gate MOS having a floating gate connected to said floating gate of said amplifier.

30. The analog arithmetic unit as defined in Claim 23, wherein:

a single control circuit is shared by the plurality of said analog arithmetic units; and
said analog arithmetic unit further comprises a switching circuit for switching said single control circuit to control said charge adjusting operation separately for said each charge adjusting element.

31. The analog arithmetic unit as defined in Claim 16, a plurality of said analog arithmetic units being provided in parallel,

wherein said control circuit in said each analog arithmetic unit controls its own charge adjusting operation using its own charge adjusting element only by absorbing charges through the tunnel effect to equalize an offset voltage of said each amplifier.

32. The analog arithmetic unit as defined in Claim 31 further comprising a judging circuit for judging an amount of said charges existing at said floating gate, so that said control circuit controls said charge adjusting operation by said charge adjusting element based on a judging result by said judging circuit.

33. The analog arithmetic unit as defined in Claim 32, wherein said judging circuit includes a differential amplifier for compensating an input offset voltage by a switched capacitor to judge whether said input offset voltage is compensated or not.

34. The analog arithmetic unit as defined in Claim 31, wherein:

said input capacitor, amplifier, and charge adjusting element are incorporated into an integrated circuit; and
said control circuit is made attachable to and detachable from said integrated circuit.

35. The analog arithmetic unit as defined in Claim 32 further comprising a feedback capacitor connected across an input end and an output end of said amplifier to function as a multiplier.

36. The analog arithmetic unit as defined in Claim 31 further comprising an activating circuit for activating said control circuit to carry out an offset compensating operation upon detection of power-up of said analog arithmetic unit.

37. The analog arithmetic unit as defined in Claim 31, wherein said charge adjusting element is a floating gate MOS having a floating gate connected to said floating gate of said amplifier.

38. The analog arithmetic unit as defined in Claim 31, wherein:

a single control circuit is shared by the plurality of said analog arithmetic units; and
said analog arithmetic unit further comprises a switching circuit for switching said single control circuit to control said charge adjusting operation separately for said each charge adjusting element.

FIG.1 (a)

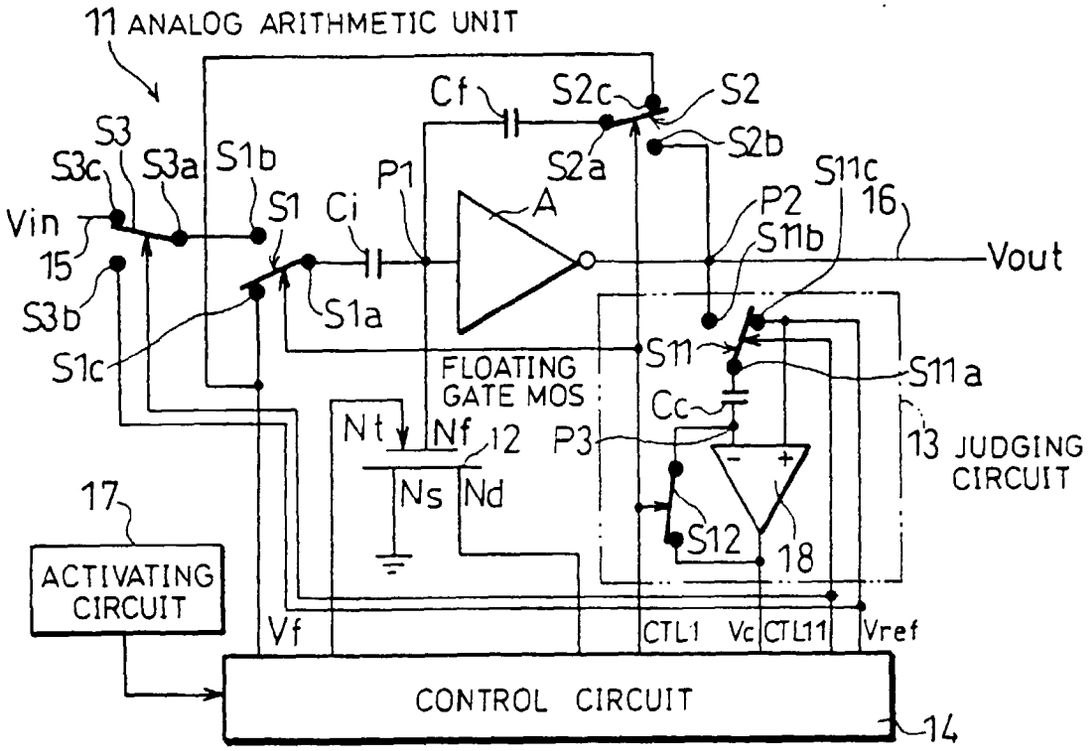

11 ANALOG ARITHMETIC UNIT
Cf
S2c
S2
S2b
S2a
S3
S3c
S3a
S1b
S1
Ci
P1
A
P2
S11c
16
Vin
15
S3b
S1c
S1a
S11b
Vout
S11
S11a
FLOATING GATE MOS
Cc
Nt
Nf
12
P3
13 JUDGING CIRCUIT
Ns
Nd
17
S12
18
ACTIVATING CIRCUIT
Vf
CTL1
Vc
CTL11
Vref
CONTROL CIRCUIT
14

FIG.1 (b)

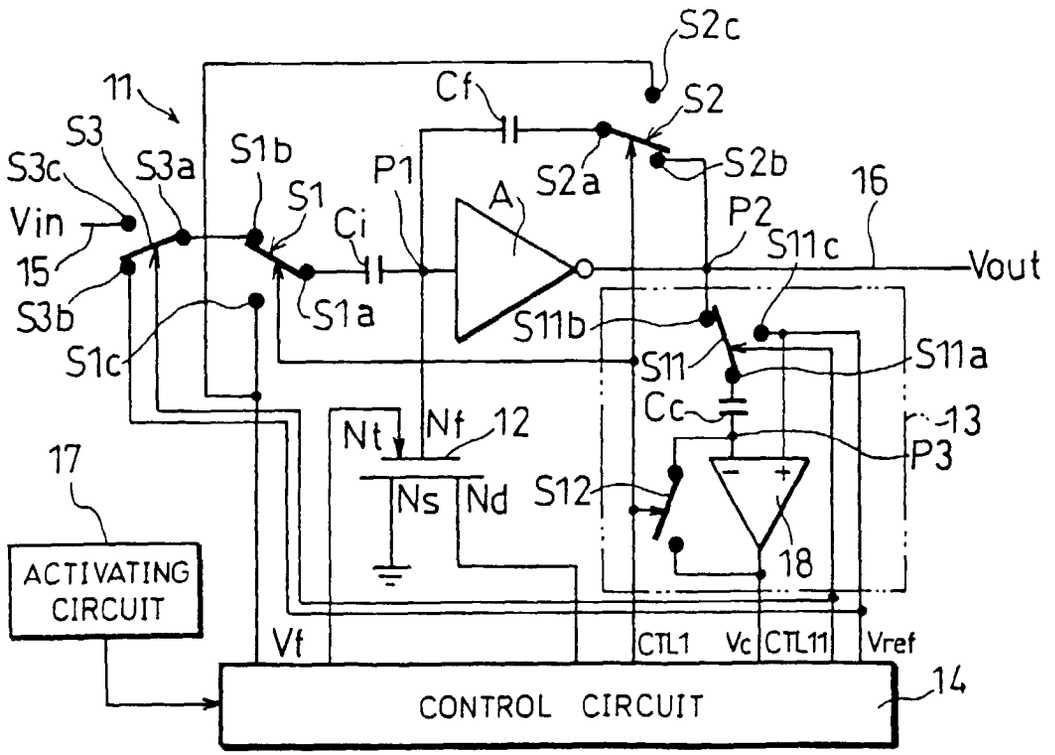

S2c
11
Cf
S2
S3
S1b
S3c
S3a
P1
S2a
S2b
16
A
S1
Ci
P2
S11c
Vin
15
Vout
S3b
S1a
S11b
S1c
S11
S11a
Cc
13
Nt
Nf
12
P3
17
Ns
Nd
S12
18
ACTIVATING CIRCUIT
Vf
CTL1
Vc
CTL11
Vref
CONTROL CIRCUIT
14

FIG. 2

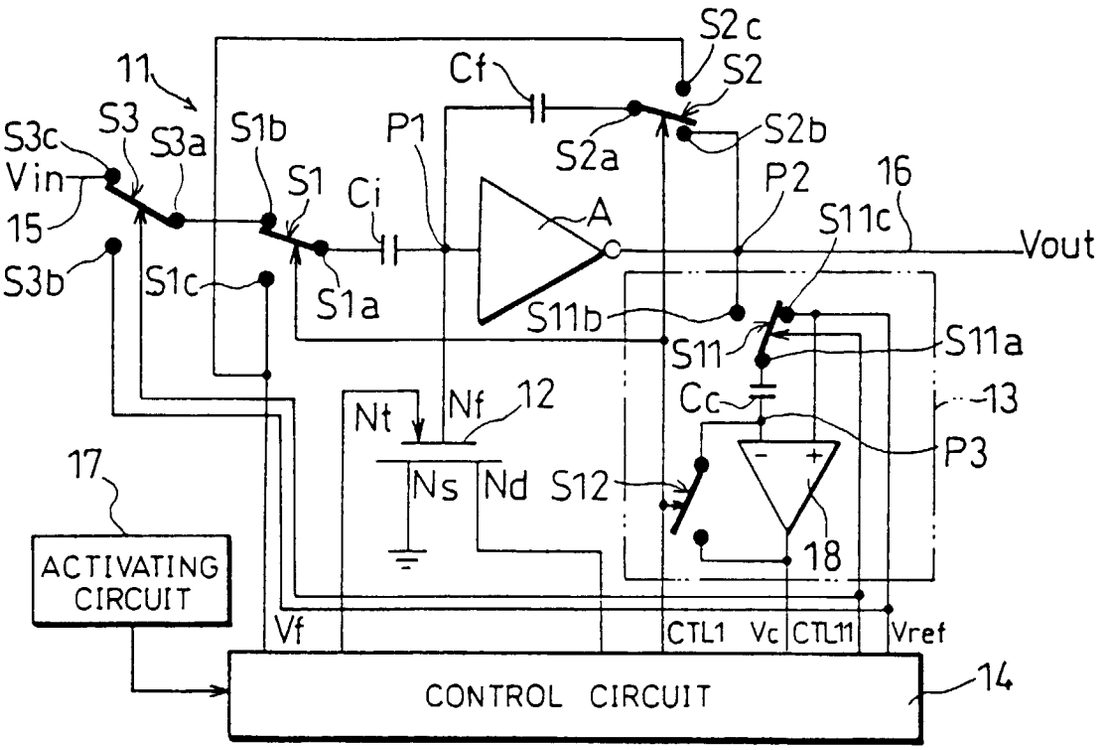
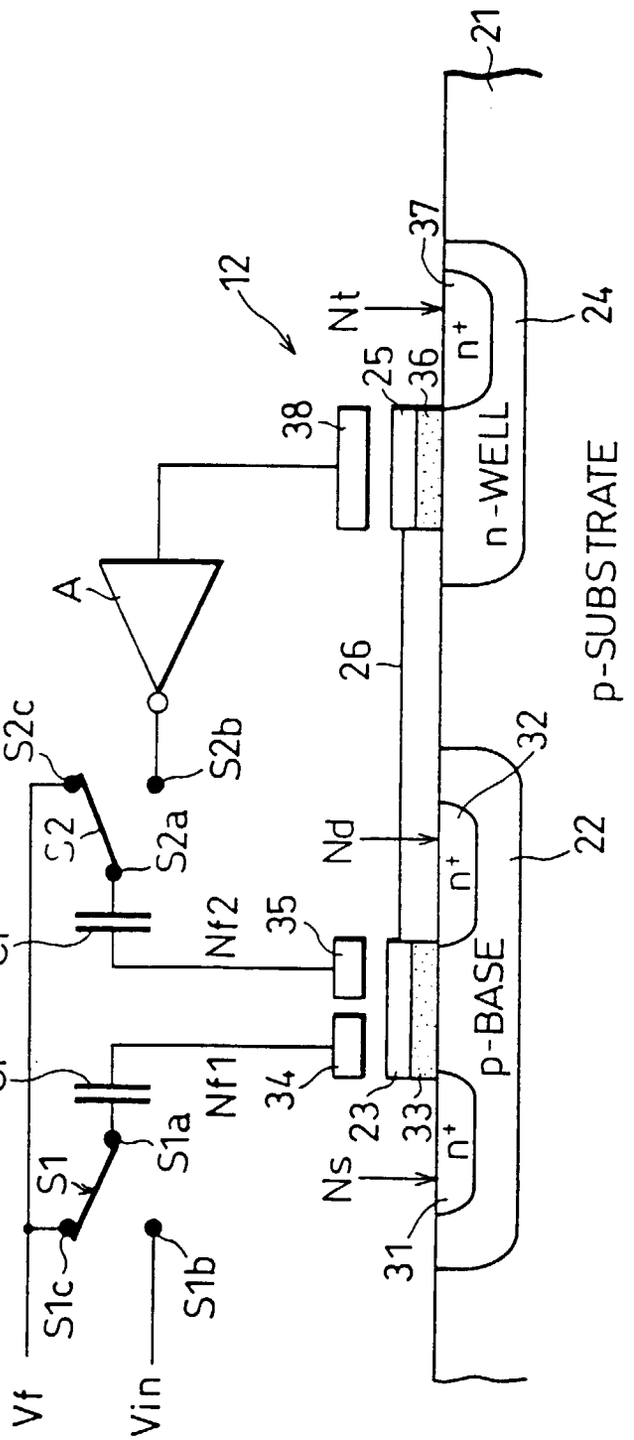

11
S3
S3c
S3a
Vin
15
S3b
S1b
S1
S1c
S1a
Ci
P1
Cf
S2c
S2
S2a
S2b
P2
16
S11c
Vout
A
S11b
S11
S11a
Cc
13
P3
Nt
Nf
12
Ns
Nd
S12
17
ACTIVATING CIRCUIT
18
Vf
CTL1
Vc
CTL11
Vref
CONTROL CIRCUIT
14

FIG. 3


12
21
37
Nt
24
25
36
n+
38
n-WELL
A
26
p-SUBSTRATE
S2c
S2b
S2
S2a
Nd
32
22
Cf
Nf2
35
n+
Ci
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Ns
n+
S1c
S1b
31
Vf
Vin

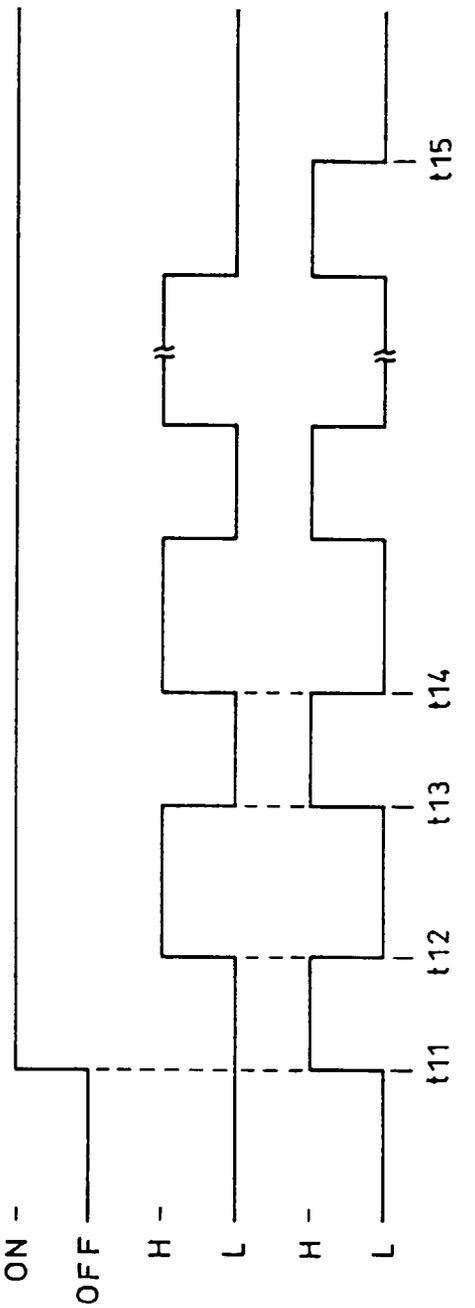


FIG. 4 (a)

FIG. 4 (b)

FIG. 4 (c)

FIG. 5

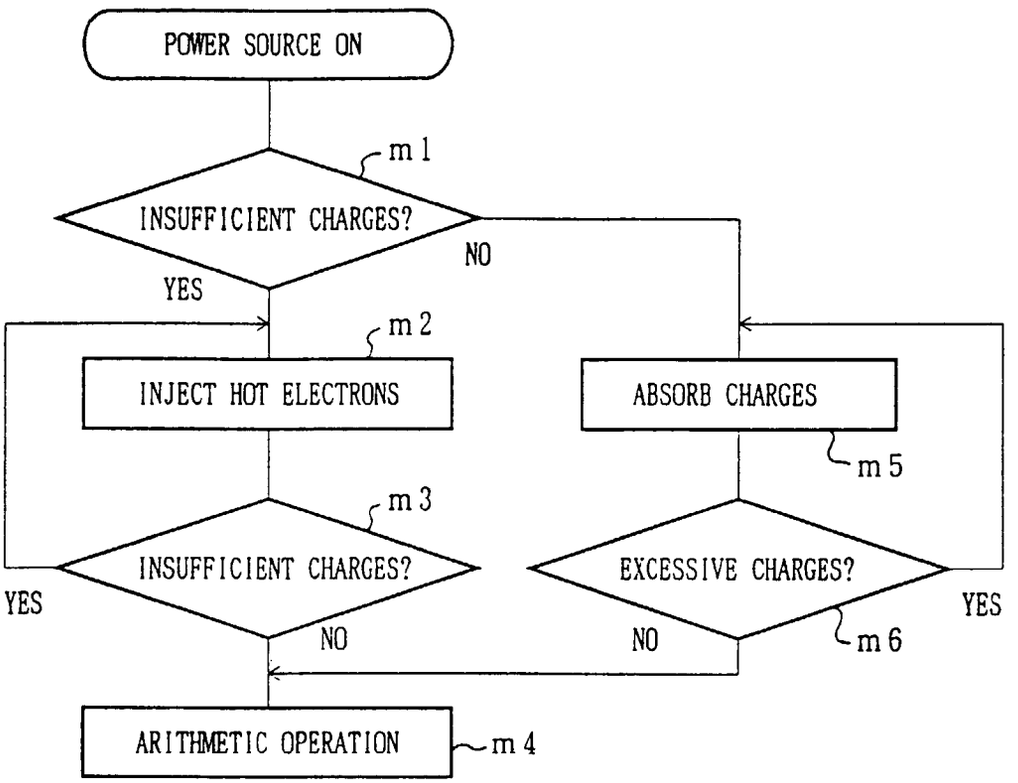

POWER SOURCE ON
m 1
INSUFFICIENT CHARGES?
NO
YES
m 2
INJECT HOT ELECTRONS
ABSORB CHARGES
m 5
m 3
INSUFFICIENT CHARGES?
EXCESSIVE CHARGES?
YES
YES
NO
NO
m 6
ARITHMETIC OPERATION
m 4

FIG. 6

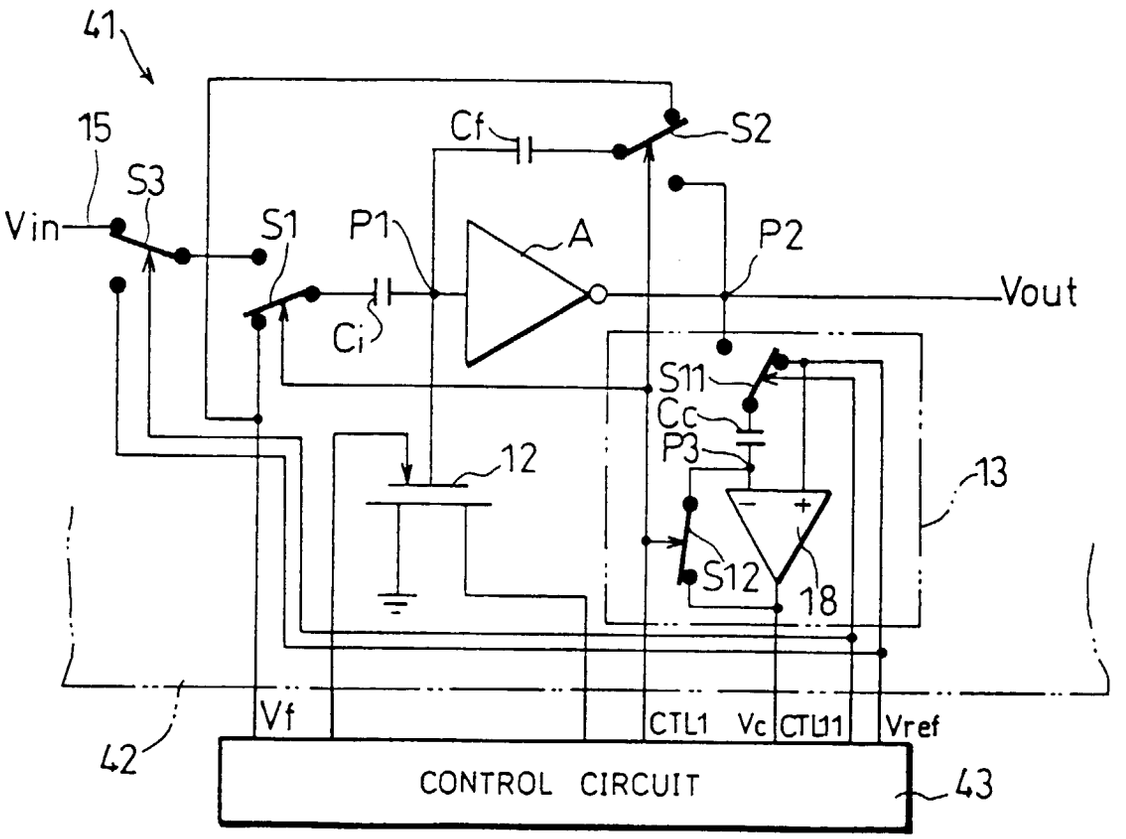

41
15
S3
Vin
S1
P1
A
Cf
S2
P2
Vout
Ci
S11
Cc
P3
12
13
S12
18
Vf
CTL1
Vc
CTL11
Vref
42
CONTROL CIRCUIT
43

FIG. 7

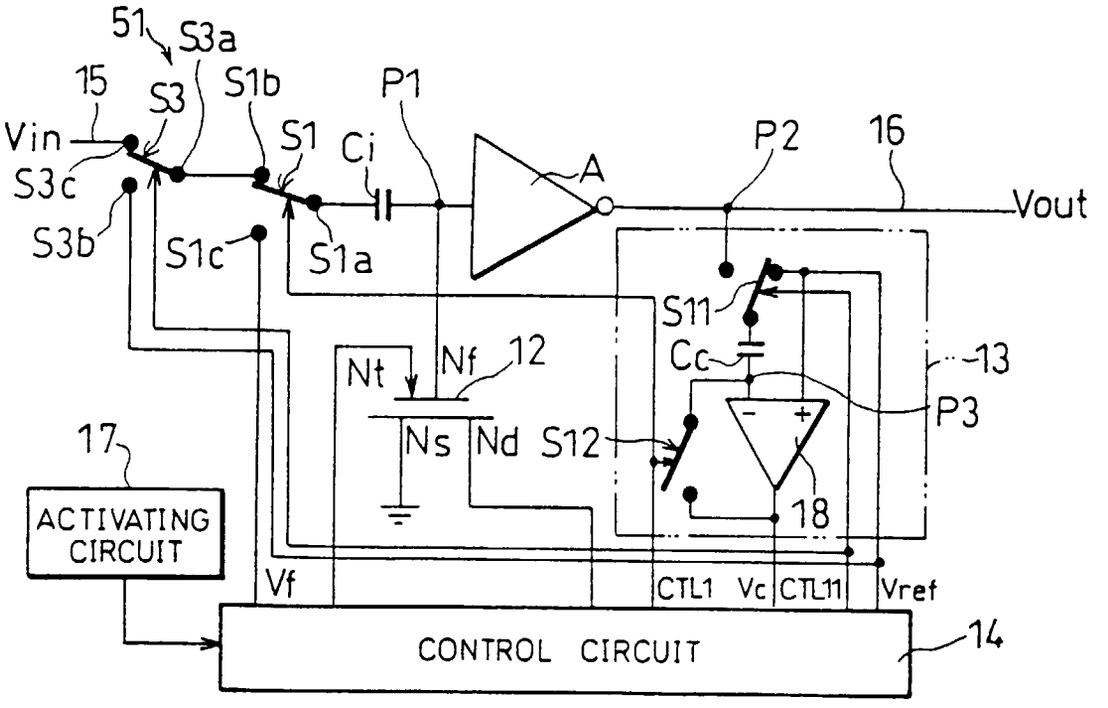

51
S3a
15
S3
S1b
P1
Vin
S1
Ci
P2
16
S3c
A
Vout
S3b
S1c
S1a
S11
Cc
13
Nt
Nf
12
P3
17
Ns
Nd
S12
18
ACTIVATING CIRCUIT
Vf
CTL1
Vc
CTL11
Vref
CONTROL CIRCUIT
14

FIG. 8

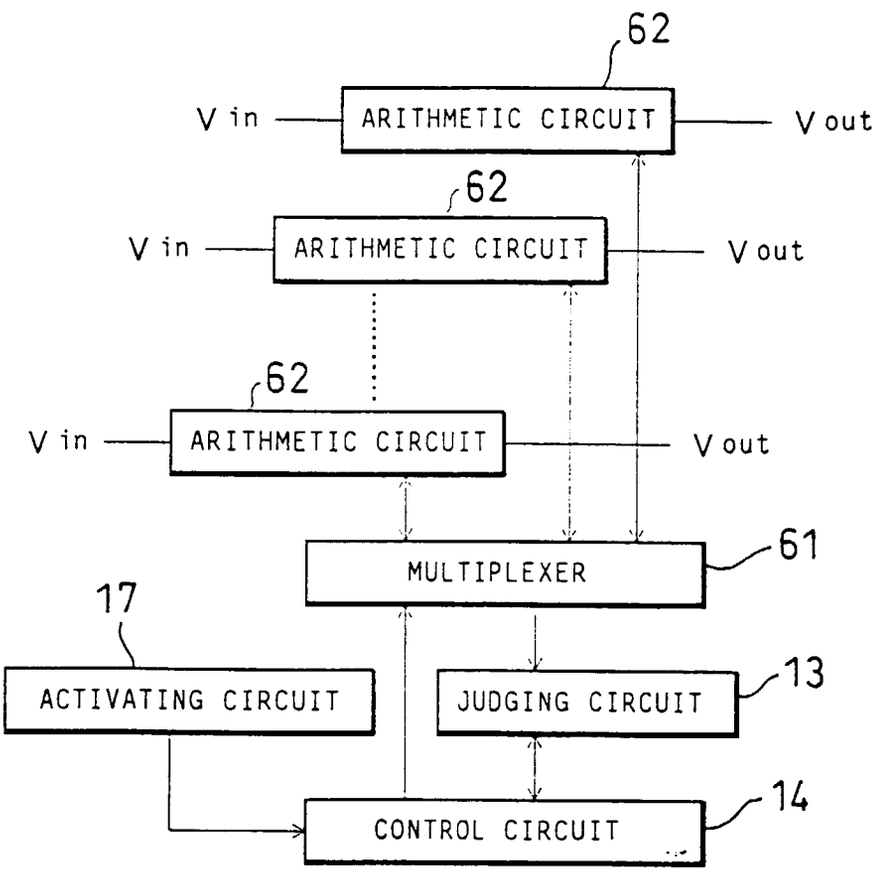
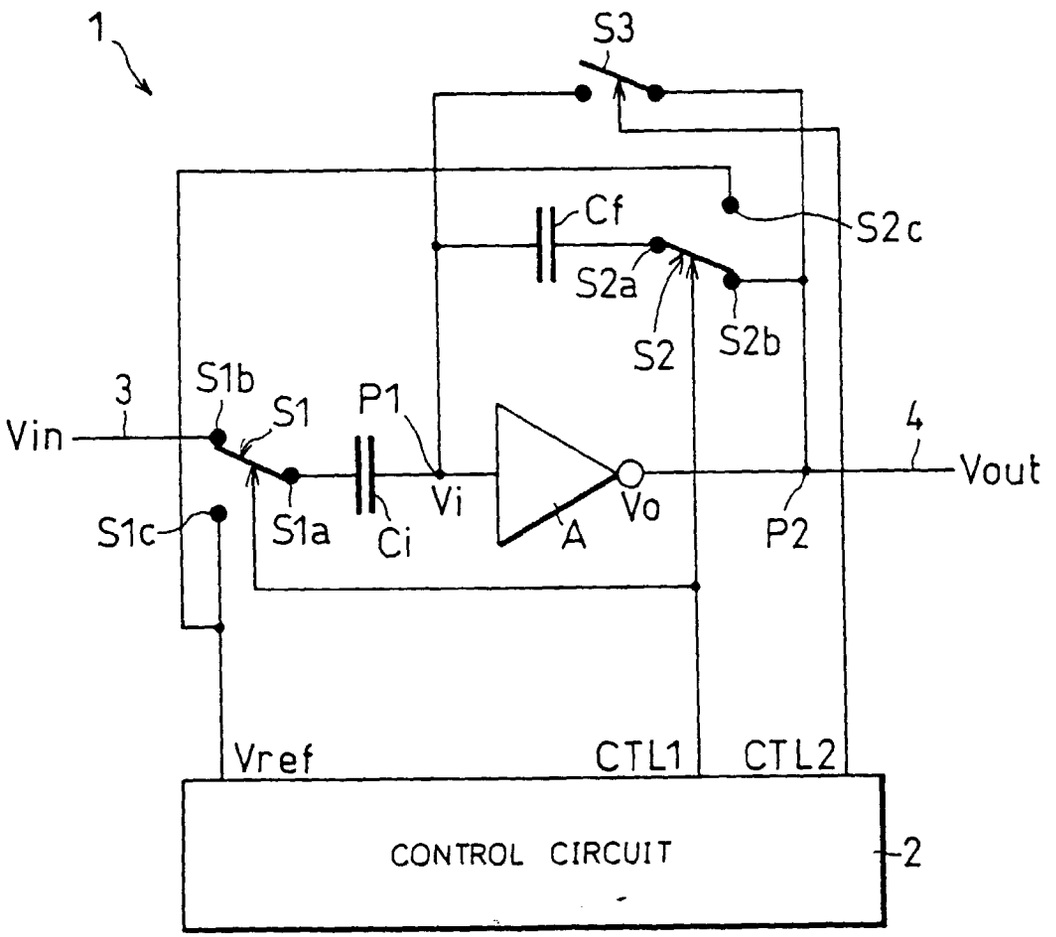

62
V in
ARITHMETIC CIRCUIT
V out
62
V in
ARITHMETIC CIRCUIT
V out
62
V in
ARITHMETIC CIRCUIT
V out
MULTIPLEXER
61
17
ACTIVATING CIRCUIT
JUDGING CIRCUIT
13
CONTROL CIRCUIT
14

FIG. 9

PRIOR ART



PRIOR ART

FIG.10(a)

FIG.10(b)

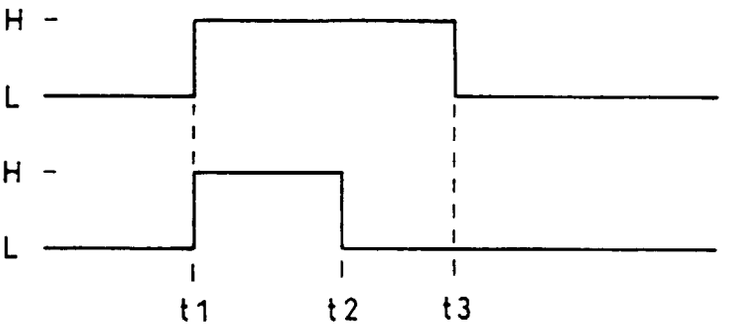
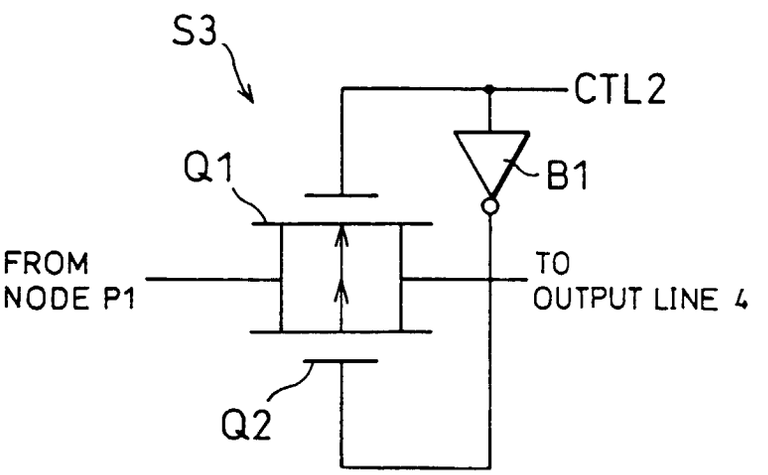


FIG.11

PRIOR ART



European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 97 30 0828

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X Y	US 5 059 920 A (ANDERSON JANEEN D W ET AL) 22 October 1991 * column 7, line 53 - column 9, line 11; figures 5D-5F * ---	1,16 2,3,17, 18	G06G7/12
Y	EP 0 047 409 A (AMERICAN MICRO SYST) 17 March 1982 * page 12, line 36 - page 14, line 26; figure 8 * ---	2,3,17, 18	
A	PROCEEDINGS OF THE MIDWEST SYMPOSIUM ON CIRCUITS AND SYSTEMS, DETROIT, AUG. 16 - 18, 1993, vol. VOL. 2, no. SYMP. 36, 16 August 1993, INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS, pages 1212-1216, XP000499795 YANG K ET AL: "MULTIPLE INPUT FLOATING-GATE MOS DIFFERENTIAL AMPLIFIERS AND APPLICATIONS FOR ANALOG COMPUTATION" * page 1215, right-hand column, line 20 - page 1216, left-hand column, line 3; figure 8 * -----	22	TECHNICAL FIELDS SEARCHED (Int.Cl.6) G06G

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	16 April 1997	Ledrut, P

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
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O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
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EPO FORM 1503 03.82 (P04C01)