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(71) Applicant: **CADDOCK ELECTRONICS, INC.**
Riverside, California 92507 (US)

(72) Inventor: **Caddock Jr.,Richard E.**
Winchester, Oregon 97495 (US)

(74) Representative: **Rackham, Stephen Neil**
GILL JENNINGS & EVERY,
Broadgate House,
7 Eldon Street
London EC2M 7LH (GB)

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(54) A resistor capable of acting as a circuit breaker

(57) An apparatus and method by which a flat film-type resistor (10) is intentionally caused to thermal-shock fracture (Figure 1) in response to a predetermined high-voltage overload condition. The resistor includes flat film-type resistor coatings (28, 29) connected to traces (16, 18, 52). Preferably a stressed spring wire (71, 72) is mounted on such film-type resistor and connected in circuit with it. A predetermined solder (76) and temperature gradient are employed to hold the spring wire in bent condition until the solder (76) melts, whereupon the spring (71, 72) flexes and the circuit breaks. Heatsink portions (43-46) are provided in the circuit board for such resistor and receive pins (33-40) thereof.

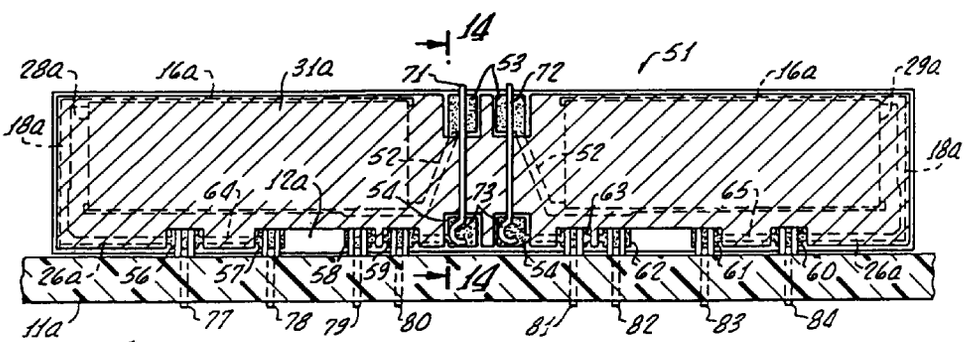

FIG. 10.

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Description

It is important that the balancing resistors used in line cards in telephone systems have precise values. Precision resistors permit proper line balancing, and proper balancing causes better voice transmission fidelity and better data transmission accuracy and reliability. Precision resistance values, however, are only one of the factors determining whether or not particular balancing resistors are looked upon favorably by telephone companies.

It is essential that the balancing resistors, and the line cards, perform in certain ways demanded by the telephone companies, at three specified or standard levels of adverse conditions. The first level is one where the line card will survive and continue to function properly despite certain conditions, one being lightning transients. The second level relates to a condition where the balancing resistors are continuously overheating, for example because the line card is overheating due to being improperly connected by a technician. Relative to this second level, there must be a thermal cutoff action to discontinue flow of current before the line-card circuit board starts to burn. The third level is one where there is a sudden application of high voltage, for example when a power line drops on the telephone line. Relative to this third level, current flow must be substantially instantaneously discontinued or small-diameter wires in the telephone system may melt.

The combined requirements for precision balancing, and for the ability to either withstand or fail safely relative to specified types of adverse conditions, must be satisfied by resistors that are physically smaller and smaller in comparison to prior-art resistors, and by resistors having resistance values that are often only a fraction of the values of prior art resistors. A great problem relative to the needs for physically small balancing resistors, and low resistance balancing resistors, is that low resistance resistors have much more power introduced therein during lightning transients and during overload conditions than is the case relative to high value resistors. For example, if the resistance value is cut in half, the introduced power doubles. Handling high power caused by lightning transients, etc., with physically smaller resistors, is extremely difficult. It is emphasised that physically small resistors inherently have less heat dissipating surface area and thus are harder to cool in comparison to the physically larger resistors of the prior art.

In sum, telephone companies want the line cards to be small so that there can be more cards in a given space. They therefore want the components on the cards to be small, and they also want the minimum number of components to be employed, while still meeting strict performance requirements.

Relative to the above mentioned second level of adverse conditions, it is customary to use fuses or thermal cutoffs that are separately manufactured and separately mounted components. These require separate operations to assemble them to the circuit board; furthermore, they require considerable room on the board.

Relative to the above mentioned third level of adverse conditions, various approaches are employed in the art. These include fuses, voltage management circuits, etc. These require separate components, and separate mounting operations, as well as needing additional space on the board.

GB-A-2,163,307 discloses a thin film resistor formed on a thin substrate which fractures in response to an excessive power level. As the disclosed substrate may fracture at any position, and therefore an adhesive tape is provided on the substrate to keep this intact.

In EP-A-0,395,231, a thick film resistor is disclosed mechanically connected to a first conductor. Due to the provision of a resistive film on only one side of the substrate, or films of different resistivity on opposite sides of the substrate, it is disclosed that the substrate will bend and crack. The resistor substrate must crack vertically at around its mid-point for the fuse conductor to be broken, and accordingly an excess power will not necessarily result in the power being cut off.

In accordance with the present invention, a resistor comprises a substrate with a resistive film applied to a surface, and termination traces connected to the film for connection to an electrical circuit, each of the termination traces being in the same circuit with the film and being provided at opposed end regions of the surfaces of the substrate and spaced from outer end portions of the resistive film, the substrate being arranged to fracture substantially instantaneously in response to thermal shock when a high voltage is applied to the resistive film to break the termination traces substantially instantaneously, to break the circuit through the resistive film and thus through the resistor.

Particular embodiments of this invention will now be described with reference to the accompanying drawings, in which:-

Fig. 1 is an isometric view showing a fractured substrate in combination with the underlying portion of the circuit board;

Fig. 2 is a front plan view of the resistor (network) for Fig. 1, before the fracture occurred, the board being unshown;

Fig. 3 is an end elevational view of the showing of Fig. 2;

Fig. 4 is a plan view showing the termination traces on both the front and back of the substrate of the resistor of Figs. 1-3;

Fig. 5 is a plan view of the front and back of the resistor after application of resistive film thereto, the film being schematically represented by hatching;

Fig. 6 is a plan view of the front and back of the resistor after application of overglaze thereto, the overglaze being schematically represented by different hatching;

Fig. 7 is a bottom and top plan view of the showing of Fig. 1, illustrating the circuit board region

beneath the balancing resistor, the pins being unshown;

Fig. 8 is a front plan view showing the traces of a balancing resistor according to a second embodiment, having means thereon for discontinuing current flow when a second-level adverse condition occurs;

Fig. 9 is a front plan view corresponding to Fig. 8 and showing the resistive film;

Fig. 10 is a front plan view corresponding to Fig. 9 and also showing overglaze and circuit-breaking spring means, as well as the pins and (in section) the underlying region of the circuit board, the heat-sinks and solder being unshown;

Fig. 11 is a back plan view showing the termination traces on the back of the resistor of Figs. 8-10;

Fig. 12 is a back plan view showing showing the resistive film on the back of such resistor;

Fig. 13 is a back plan view showing the overglaze on the back of such resistor, this being the rear view of Fig. 10 but with the pins and circuit board portion being unshown, the solder being unshown;

Fig. 14 (sheet 1 of drawings) is a greatly enlarged view, partially in cross section and partially in side elevation, taken on line 14-14 of Fig. 10; and

Fig. 15 (sheet 1 of drawings) is a view corresponding to Fig. 14 but showing the spring in its position assumed after interruption of the circuit.

Referring first to the embodiment of Figs. 1-7, a resistor 10 is mounted on a circuit board 11, the latter being shown only in small part, namely that part which provides the mounting region for the resistor 10. The circuit board has not only resistor 10 but also other telephone line-card components thereon; all together form a line card in a telephone system. Each line card conventionally has two to four channels therein, each channel being connected to an above-ground or below-ground subscriber line.

Figs. 4, 5 and 6 show both the front and back of the substrate. Fig. 7 shows both the bottom and top of the underlying circuit board region.

As shown in Figs. 2-7, the resistor 10 is a film-type resistor having an elongate rectangular substrate 12 that is so constructed and related as to fracture, in a certain general way, when subjected to predetermined thermal-shock conditions, as set forth below.

As shown in Fig. 4, a pattern of termination traces (metallization) 13 is formed on both the front and back of substrate 12. The traces 13 are, for example, formed of a palladium-silver composition and are screen-printed onto the substrate and then fired.

As described below, there are two resistive films on each side of substrate 12. The two films on one half (for example) of the substrate form one resistor; the two films on the other half form another resistor. Such one and such other resistor are balanced (vis-a-vis resistance values) relative to each other, normally in a fifty-fifty manner.

For such a resistor network, the traces 13 preferably have the following pattern: two lower traces 14 in axial alignment and separated by a central gap 15; two upper traces 16 in axial alignment and separated by a central gap 17; and two end traces 18 connected to upper traces 16 but not to lower traces 14. End traces 18 are spaced a relatively short distance from lower traces 14, the short spacing being to minimize the length of the substrate. Traces 14,16 are parallel to each other and to the upper and lower edges of substrate 12, while end traces 18 are parallel to each other and to the ends of the substrate, being perpendicular to traces 14,16.

The trace pattern further comprises four sets of double pin (solder) pads. Thus, there are two sets of outer pads 20,21 preferably spaced about one third of the way from the substrate ends to the substrate center. There are also two sets of inner pads 22,23 that are spaced outwardly from the substrate center. Thus, the inner ends of lower traces 14 are spaced inwardly from inner pads 22,23. The two pads in each set 20,21 and 22,23 are spaced from each other and connected together by a trace region 24. The pads are closely adjacent the horizontal lower edge of substrate 12.

Outer pads 20,21 are connected by trace regions 26 to the lower ends of end traces 18. Inner pads 22,23 are connected by trace regions 27 to lower traces 14.

Two resistive films 28,29 are applied, by screen-printing, to each side of substrate 12 and in identical relationship to the termination traces 13, as shown in Fig. 5. Thus, each film 28,29 has its upper and lower edges printed over traces 16 and 14, respectively. The ends of films 28,29 are located close to but preferably not over opposite ends of traces 14 and 16. Films 28,29 are electrically-conductive complex metal oxides in a glass matrix.

Referring next to Fig. 6, an arc-preventing and environmentally protective coating 31 is provided over both sides of substrate 12 and over the traces and resistive films thereon. The coating is not applied over the pads 20-23, or (preferably) to the spaces between adjacent sets 20-21 and 22-23 of pads. The composition and thickness of coating 31 are described below.

Pins 33-40, inclusive, are respectively connected to the pads 20-23 as shown in Figs. 2 and 3, there being one pin (for example, pin 40 in Fig. 2) connected to two pads on directly-opposite side regions of substrate 12. Each pin has an elongate shank connected integrally, at a shoulder, to jaws 41 that grip the lower edge of substrate 12. For example, there are two jaws on one side of the substrate and one jaw on the other side thereof. The shank of each pin is, for example, 0.010 inch (0.25mm) front-to-back and 0.020 (0.5mm) inch wide. The pins are preferably phosphor bronze, plated and stamped.

Proceeding next to a description of the circuit board 11, only a portion of which is shown in Figs. 1, 7 (and 10), this is a conventional epoxy and glass board having copper traces thereon for connection of many compo-

nents (not shown) in the circuit. In the preferred embodiment of the present combination, board 11 not only has copper traces thereon but also has copper heatsink regions 43-46 on both sides thereof for reception of pins 33-40. Referring to Figs. 1 and 7, there are (in the present example) four heatsink regions 43-46 on each side of board 11, each region on the top of the board being (preferably) directly in registry with a corresponding region on the bottom side thereof. Eight holes 47 are formed in regions 43-46, there being two holes in each region. The holes 47 are through-hole plated.

The heatsink regions 43-46 are formed by etching during the manufacture of the board, just as the circuit traces on the board are formed. Soldermask coatings 48 are formed on the top and bottom sides of the board 11.

The pins are inserted into the respective holes 47 until the shoulders at the bottoms of jaws 41 engage the upper board surface. Then, solder is applied at each hole 47 to solder the shanks of the pins therein. Preferably, there is no solder present except adjacent the pin shanks, the heatsink regions 43-46 being covered by the soldermask portions.

Description of Method, and Further Description of Article, First Embodiment of the Invention (Figs. 1-7)

According to a first aspect of the method relative to the first embodiment, a substrate 12 is--intentionally--employed that will substantially instantaneously fracture, as the result of thermal shock, in response to application of a high-voltage overload to either resistor on the substrate, or to both resistors thereon. In accordance with a second aspect of the method, the termination traces, resistive films, and other factors are intentionally caused to be such that, reliably, the thermal-shock fractures will break the circuits substantially instantaneously, terminating all current flow with little or no arcing.

It is to be understood that the presently-described resistors are respectively in circuit with other components of the line card, so that breaking of the circuit through one or both resistors also stops current flow in respective components connected to these resistors.

Thus, the fracture of the substrate satisfies the above-stated third-level adverse condition. When, for example, falling of a high-voltage power line on the telephone line creates an instantaneous high-voltage overload, current flow is terminated so fast that fine wires in the telephone circuit will not melt.

In accordance with another aspect of the method, the termination traces and other factors are caused to be such that the instantaneous thermal-shock breakage occurs at predetermined regions of substrate 12, and not at other regions thereof. This not only reduces debris but, as described below relative to the second embodiment, assures that no significant length of metal element will fall on other components of the circuit board and tend to create arcs or short circuits.

The substrate 12 is sufficiently thin to instantaneously fracture in response to sudden application of a high-voltage (such as 600 volts) overload, but sufficiently thick to satisfy the following two requirements: (1) effect thermal conduction of a substantial amount of heat through the substrate from the resistive films 28,29 to pins 33-40 and thus into the heatsink regions 43-46, and (2) provide sufficient resistance to mechanical breakage that the line card is not fragile.

The material of substrate 12 is selected to satisfy the above-stated criteria. Very preferably, it is a ceramic. The preferred ceramic is aluminum oxide. More specifically, it is preferably 96% aluminum oxide, (available as No. ADS 96R, from Coors Ceramics Co. of Grand Junction, Colorado).

The preferred thickness of the substrate is about 0.040 inch (0.1mm).

Referring to Fig. 1, it is pointed out that the upper-outer regions of the substrate and films thereon are not present. These regions have broken away as a result of the thermal shock fracture. Referring to Fig. 4, it is pointed out that--in the preferred embodiment of the present method--current is conducted to the upper traces 16 by traces 18 located at the ends of substrate 12. Such flow is through pads 20,21 and trace regions 26. The current flows through the films 28,29 and through trace regions 14 and 27 to the remaining pads 22,23 and thus to the circuit board.

By causing the traces 18 to be at the outer ends of the substrate, it is assured that breakage will be at the upper-outer corners and that the traces 18 will break and thus interrupt the circuits through components respectively connected to the resistors. (As noted above, the overload may be applied to only one of the resistors, on only one half of the substrate 12, in which case only one of the traces 18 will break.)

Referring again to Fig. 1, it is pointed out that the central region of the substrate, and all the lower edge of the substrate, are intact. This is the typical condition resulting from the present method and apparatus.

It is emphasized that the thermal-shock fracture of the present resistor is intentional, being for the combined purposes of (1) preventing damage to other elements of the telephone system and (2) eliminating the need for a separate component or circuit adapted to protect against instantaneously-applied high voltages.

Resistors have "exploded" for years due to thermal shock caused by power overload, and this was generally regarded as undesirable. Here, on the other hand, applicant is creating controlled conditions such that a predetermined desired type of "failure" will occur and create a beneficial result. The resistive film and termination traces are so shaped and correlated as to create the necessary stress pattern. The resistive film is made such that application of the voltage being guarded against will generate enough power and heat to fracture the substrate. Conjointly, the substrate is caused to have such composition, and physical shape, that it will properly fracture when the heating occurs.

The breaking of the termination traces 18 as the

result of the thermal-shock fracture creates momentary arcing and ionization at the points where such traces initially break. Although the arcing is only of short duration, since the corners of the substrate 12 fall away, the air is ionized in the surrounding regions. This increases greatly the tendency toward arcing at regions of the circuit where the voltage differential is greatest. It is an additional aspect of the present method to provide the coating 31, to prevent arcing between such high voltage-differential regions despite the ionized air thereat.

As shown in Figs. 4-6, there is a relatively small gap G between the outer ends of lower traces 14 and the lower regions of end traces 18. The gap G is caused to be small in width because every increment that it is enlarged increases the length of substrate 12 by two increments, in the present double resistor. Preferably, the width of each trace 18 opposite trace 14 is somewhat narrower than is the width of each trace 18 at regions spaced above traces 14. This increases gap G without lengthening the substrate and thus the entire resistor, but there are severe limits relative to increasing gap G in this manner.

The additional aspect of the invention comprises providing the arc-resisting coating 31 on the resistor, at least at regions over and relatively near the gaps G, and preferably at all regions except the pads 20-23 and substrate regions between such pads (Fig. 6).

Stated more specifically, the arc-preventing coating--and which is additionally an environmentally-protective coating--31 is a glass layer having a thickness correlated to the width of gap G. Where the gap G is to be small for minimized resistor size, the glass coating is made thick. On the other hand, where the size of the substrate is not such that each gap G must be small, the thickness of the glass coating 31 is made less in order to minimize cost.

To state specific examples, a O.OOl inch (25μm)-thick layer of glass has been found to substantially completely protect against failures (for a 600 volt suddenly-applied test voltage) when the gap is 0.032 inch (0.8mm) wide. When the deposited glass is 0.0008 inch (20μm) in thickness, there are some failures for the same gap width. For a glass deposit 0.0006 inch (15μm) thick, there are a substantial number of failures for a gap of the specified width. Therefore, for such a gap applicant employs a glass deposit 31 having a thickness of 0.001 inch (25μm).

The glass is screen printed onto the substrate above the traces and above the resistive films, as stated above. Glass frit, having a relatively low melting point, is screen-printed onto the region shown in Fig. 6, following which the part is fired in order to fuse the glass particles.

It is important that the glass not degrade the resistive films 28,29. For resistive films that are fired at temperatures of 800 degrees C and above, the glass frit is caused to have a melting point slightly below 500 degrees C. Thus the firing in order to fuse the layers 31 is at 500 degrees C.

The resistor 10 of the first embodiment will also satisfy the above-stated first level of adverse conditions, namely that the resistor will survive and operate properly under adverse conditions, such as those created by lightning transients. This is because of reasons including the good heat transfer characteristics from the resistor 10 to the circuit board and outwardly from the pins 33-40. This, however, is described below relative to the second embodiment of the invention.

Resistor Combination and Method of the Second Embodiment of the Invention, Figs. 7-15. Inclusive.

An exemplary length for the above-described resistor 10 is 1.8 inches (46mm). By making it (for example) 2 inches (50mm) long, namely by adding 0.2 inch (4mm) to the length of the substrate, the resistor combination is made to satisfy all three of the levels of adverse conditions. This eliminates the need for a separate thermal cutoff element in order to satisfy the second level.

The front side and back side of the above-described resistor of Figs. 1-6 are preferably identical, as previously stated. In the resistor of the second embodiment, the front and back sides are normally not identical to each other and thus, relative to some regions thereof, are separately described. With the major exceptions stated below, the resistor (and circuit board) of the second embodiment is identical to resistor 10 of the first embodiment. Elements in the second embodiment that substantially correspond to elements in the first embodiment are given the same reference numerals, except followed in each instance by the letter "a".

The resistor combination of the second embodiment is numbered 51 (Fig. 10). Referring to Fig. 8 (front view) and Fig. 11 (back view), the substrate 12a has upper traces 16a and end traces 18a as well as lower traces 14a. The inner ends of traces 16a and 14a on each half of the resistor are spaced further apart than is the case relative to the resistor of the first embodiment. On both sides of the resistor, trace sections 52 connect to the inner ends of lower traces 14a and extend upwardly and inwardly to pads 53, respectively. The two pads 53 on each side of the substrate are spaced apart, and are adjacent the upper edge of substrate 12a. Adjacent the bottom edge of the substrate, on only the front of the resistor, are pads 54 (Fig. 8). Such pads 54 are respectively directly below the pads 53 on the substrate front.

Pads 56-63 (Fig. 8) are provided along the bottom edge of substrate 12a, the pads 56-59 on one half of the substrate 12a being, respectively, the mirror images of the pads 60-63 on the other half of the substrate. Pads 56 and 60 are respectively connected to trace regions 26a and thus through end traces 18a to upper traces 16a. Trace portions 64 and 65 respectively connect pads 56,57 and pads 60 and 61 together.

Pad 56 is spaced a substantial distance from the end of the substrate and from the next pad 57. Corre-

spondingly, pad 60 is spaced a substantial distance from the end of the resistor and from pad 61. On the other hand, pads 58,59 are quite close to each other, as are pads 62,63. The pad pair 58,59 is close to the inner end portion of trace 14a, which inner end portion is relatively wide as shown. Correspondingly, the pad pair 62,63 is relatively close to the inner end of the right lower trace 14a, which inner end portion is relatively wide as shown.

Trace region 66 connects together the pads 58,59; trace region 67 connects together pads 62,63. Trace region 68 connects pad 59 to pad 54, while trace region 69 connects pad 63 to the other pad 54.

There are no pads 54 or trace regions 68 or 69 on the back of the substrate (Fig. 11). Elements 56, 64, 57, 58, 66, 59, 63, 67, 62, 61, 65 and 60 have corresponding elements on the back of the substrate, and these are given the same reference numerals except followed in each instance by the letter "b".

Resistive films 28a and 29a are applied between the upper and lower termination strips 16a and 14a, as shown in Figs. 9 and 12. A layer of overglaze 31a, Figs. 10 and 13, is applied over each side of each resistor, except (in the example) at the various pads and except between pads 57-58 and 61-62 (and 57a-58a and 61a-62a).

The Spring-Wire Cutoff

An electrically conductive spring wire 71 is soldered between the pads 53,54 on the front of the left resistor (Fig. 10). An electrically conductive spring wire 72 is soldered between pads 53,54 on the front of the right resistor. Each wire 71,72 is not in its free condition but instead is in stressed or flexed condition, the relationships being such that the lower end of each wire will spring away from its pad 54 in response to melting of the solder at such pad. (The solder is not shown in Figs. 10 or 13, but is shown in Figs. 14 and 15, first sheet of drawings.)

The upper ends of spring wires 71,72 are bent in hairpin relationship around the upper edge of substrate 12a, and are soldered to the pads 53 on the back of the substrate (Figs. 13 and 14). Thus, the relationships are such that current flow from both resistive films 28a--on the front and back of the substrate 12a--flows through traces 52 and thence through the spring wire 71 to pad 54 and its associated pins. The same current flow pattern occurs--in mirror-image relationship to that just described--relative to the films 29a, the current flowing in series through spring wire 72.

The lower end of each wire 71,72, at its associated pad 54, is bent ("kinked") in semi-circular relationship so as to increase the amount of wire metal associated with the solder on each pad 54, reference being made to Fig. 10.

Referring next to Figs. 14 and 15 (first sheet of drawings), these show spring 71 in two positions; it is to be understood that the same views apply also to spring 72 and its associated attachments. Spring 71 has a U-shaped upper end 71a the arms of which seat (due to spring bias) against pads 53 on directly-opposite sides of substrate 12a. Such arms are secured to such pads by solder 74,75.

Below solder 74, which is on the front side of substrate 12a, spring 71 is bent along a flex region 71b, which is under stress tending to spring it to the position of Fig. 15. When in normal position, Fig. 14, the lower end of portion 71b is secured to pad 54 by solder 76, the latter being associated with the kink 73 shown in Fig. 10.

Eight pins 77-84 are connected, at their jaws, to the respective pads 56-59, 63, 62, 61 and 60. As described relative to the first embodiment, these pins are passed through and soldered in through-hole plated holes in circuit board 11a (Fig. 10). Around the holes on both sides of the board are heatsink regions corresponding to those described above, except for location. There are two heatsinks, directly opposite each other at each pin or pair of pins, as shown in Fig. 7 except for the spacing of the pin holes to correspond to and receive the pins shown in Fig. 10.

The material employed by applicant for the spring wires 71,72 is stainless steel, 17-7 PH, condition C. The diameter of each wire is 0.012 inch (0.3mm). The preferred range of diameters for the spring wires 71,72 is about 0.005 inch (0.125mm) to about 0.020 inch (0.5mm).

Each spring wire is silver plated. The solder employed at pads 54 on the front side of the substrate 12a, and preferably also at all other pads on the substrate, is 96.5% tin and 3.5% silver. The melting point of this eutectic is 221 degrees C.

The solder which connects the pins to the circuit board 11a is 63% tin--37% lead, which melts at 183 degrees C, namely 38 degrees C lower than the melting point of the specified tin-silver solder.

In accordance with one aspect of the present method and apparatus, although the melting point of the solder on the substrate is distinctly higher than that of the solder that connects the pins to the circuit board, the latter solder does not melt until (if at all) after solder 76 (Figs. 14 and 15) melts to release the springs 71,72 from the Fig. 14 position to the open-circuit Fig. 15 position.

Because of the close proximity of pads 58,59 and 54, and 62,63 and 54, to the lower-inner corners of resistive films 28a and 29a, these pads and the solder thereon become relatively hot. This is especially true since the substrate 12a is a relatively good thermal conductor (for a ceramic) and conducts heat from the corner regions of the resistive films to the specified pads. Much of this heat is dissipated not only into the circulating air in the chamber containing the line card, but (importantly) down the pins 79,80 and 81,82 to the circuit board 11a and the copper heatsinks thereon on both sides thereof.

The distinct thermal gradients down such pins, and

through the heatsinks away from the pin portions in the circuit, are such that the conventional solder at the circuit board does not melt before the springs 71, and/or 72, release or "trip".

Additional Disclosure and Discussion

The same thermal-gradient action, with temperature decreasing down the pins from the pads to the circuit board, is also present in the above-described first embodiment, and makes such embodiment--and the present one--better able to withstand the first level of adverse conditions.

The present second embodiment also withstands the second level of adverse conditions, because the springs (one or both) trip and discontinue current flow to thus protect the board and insure that it does not burn. To again adapt the line card for operation, the technician replaces the present resistor combination with one identical to it.

Relative to the third level, instantaneous high-voltage overload, the springs 71,72 do not trip. Instead, the upper regions of the substrate 12a fracture away due to thermal shock. The pattern may be, for example, similar to that shown in Fig. 1. The central region of the substrate 12a does not break; thus, the springs 71,72 and their associated elements do not fall onto other portions of the board and possibly create arcs.

To manufacture the resistor combination of the present embodiment, the pins 71-84, which are all connected to a tie bar (not shown), at the jaws of such pins are mounted over the bottom edge of substrate 12a at the respective pads. The lower portions of spring wires 71,72 are initially much longer than shown, and project downwardly from the substrate to regions behind the tie bar. Thus, the tie bar holds the spring regions in contact with pads 54, the springs then being in the flexed relationship of Fig. 14.

Then, the assembly is dipped into a molten bath of the specified solder or (less preferably) another solder, to simultaneously secure all of the jaws to the respective pads and to secure the springs to pads 54. The spring portions adjacent upper pads 53 may be soldered in a separate dipping operation conducted later, or at the same time by dipping the entire resistor into the solder bath. Thereafter, the tie bars and the projecting spring regions are cut off.

Exemplary resistors embodying the present invention have a value of fifty ohms, that is to say a total of fifty ohms on each side of the center of the substrate. Such 50-ohm resistors have a rating of 3.125 watts each, with application of 12.5 volts, and operate continuously up to 85 degrees C ambient temperature in the chamber containing the line cards. Above 85 degrees C, the combination of ambient temperature and the temperature generated by the resistors at the lower ends of springs 71,72 causes the springs 71,72 to trip and discontinue current flow.

It is to be understood that, with film resistors having certain ohm values, there may be films on only one side of the subtrate instead of both sides thereof.

Claims

1. A resistor (10) comprising a substrate (12) with a resistive film (28,29) applied to a surface, and termination traces (14, 16, 18, 26) connected to the film (28,29) for connection to an electrical circuit, each of the termination traces (18) being in the same circuit with the film and being provided at opposed end regions of the surfaces of the substrate and spaced from outer end portions of the resistive film (28,29), the substrate (12) being arranged to fracture substantially instantaneously in response to thermal shock when a high voltage is applied to the resistive film (28,29) to break the termination traces (18) substantially instantaneously, to break the circuit through the resistive film (28,29) and thus through the resistor (10).

2. A resistor according to claim 1, in which resistive films (28,29) and termination traces (14, 16, 18, 26) are applied to the front and back surfaces of the substrate (12), such that the thermal shock fracture breaks the circuit through both of the resistive films (28, 29).

3. A resistor according to claim 2, in which the termination traces include lower traces (24) applied to both the front and back surfaces of the substrate (12) and pin means (33-40) mounted on the substrate (12) and soldered to the lower traces (24) for connection to a circuit board.

4. A resistor according to claim 2 or 3, in which the resistive films (28,29) on the front and back surfaces of the substrate have substantially the same shape and are substantially registered with each other.

5. A resistor according to any one of the preceding claims, in which the resistive film (28, 29), the substrate (12), and a trace portion (18), are arranged to fracture at the corner portion of the substrate as the result of a high voltage overload.

6. A resistor according to any one of the preceding claims, and further comprising a heat responsive circuit with the resistive film (28, 29), the circuit breaker (71, 72) being adapted to break the circuit through the resistive film (28, 29) in response to sustained excessive flow of current through the resistive films.

7. A resistor according to claim 6, in which the heat responsive circuit breaker means (71, 72) is mounted on a portion of the substrate (12) not at the corner portion thereof.

8. A resistor according to claim 6 or 7, in which the circuit breaker means include a stressed spring wire (71, 72) soldered to the substrate (12), the solder (76) being adapted to melt at one end (73) of the stressed spring wire (71, 72) so that the one end (73) springs away from the substrate (12) to break the circuit when excessive heating occurs.

9. A resistor according to claim 8, in which the spring wire is a hook end conductive spring wire, the hook end (71a) of which extends around an edge of the substrate (12) in the vicinity of connection pads, and solder (75, 74) connects the extreme end of the hook end to a connection pad (53), the spring wire (71, 72) being stressed when the hook end is thus soldered to the pads (54), so as to spring away from the substrate (12), and solder (76) connects a free end (73) of the spring wire (71, 72), remote from the hook end thereof, to another pad (54).

10. A resistor according to any one of the preceding claims, in which resistive films (28, 29) are applied to the front and back surface of each half of the substrate (12), the resistive films on each surface being separated from each other by a gap regions (15, 17), the resistive films on each side of the gap region forming one of two resistors, balanced in value relative to the resistor on the other side of the gap regions (15, 17), and having four pin means (33, 34; 35, 36; 37, 38; 39, 40) mounted along the lower edge of the substrate (12), there being two pin means for the resistive films on the front and back surfaces of the substrate (12) on opposite sides of the gap regions (15, 17), and in which termination traces (24) applied to the substrate (12) are connected between the pins and the films (28, 29), the termination traces (24) and the two pin means (33-36) on one side of the gap regions (15,17) connecting in parallel with each other the films (28 or 29) on the front and back surfaces of the substrate (12) on the one side of the gap regions (15,17) and the termination traces (24) and the two pin means (37,40) on the other side of the gap regions (15,17) connecting in parallel the films (29) on the front and back surfaces of the substrate (12) on the other side of the gap regions (15,17), and arranged so that the fracture occurs only at parts of the substrate that do not include the gap regions (15,17).

11. A resistor according to any one of the preceding claims, in which the substrate (12) is flat and formed of a ceramic, and has continuous flat surfaces.

12. A resistor according to any one of the preceding claims, in which the resistive films (28,29) are applied by thick film screen printing, and in which an arc minimising overglaze (31) is screen printed onto the substrate (12) over the films (28,29) and the traces (14, 16, 18, 26).

13. A resistor according to any one of the preceding claims, and arranged for use in a telephone circuit, wherein, in response to a sudden application of a voltage overload to the termination traces, the fracture of the substrate is so fast that fine wires in the telephone circuit are not damaged.

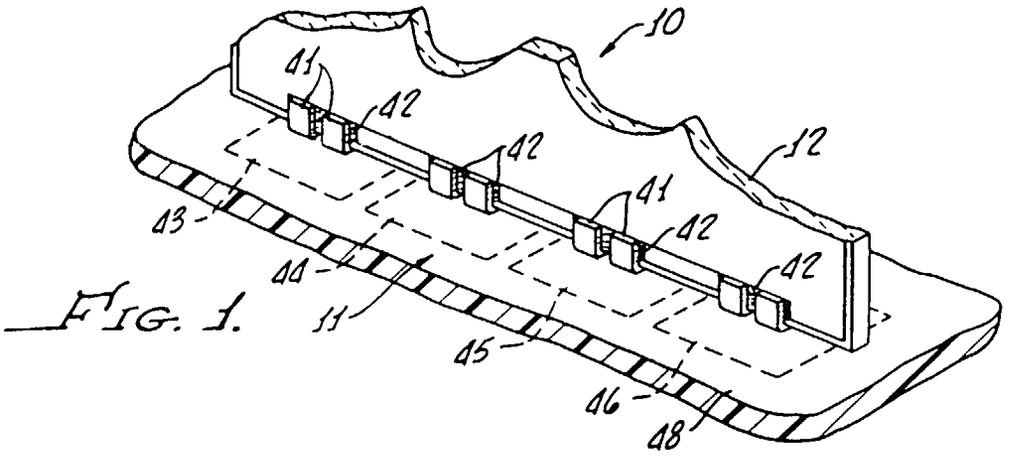


FIG. 1.

FIG. 2.

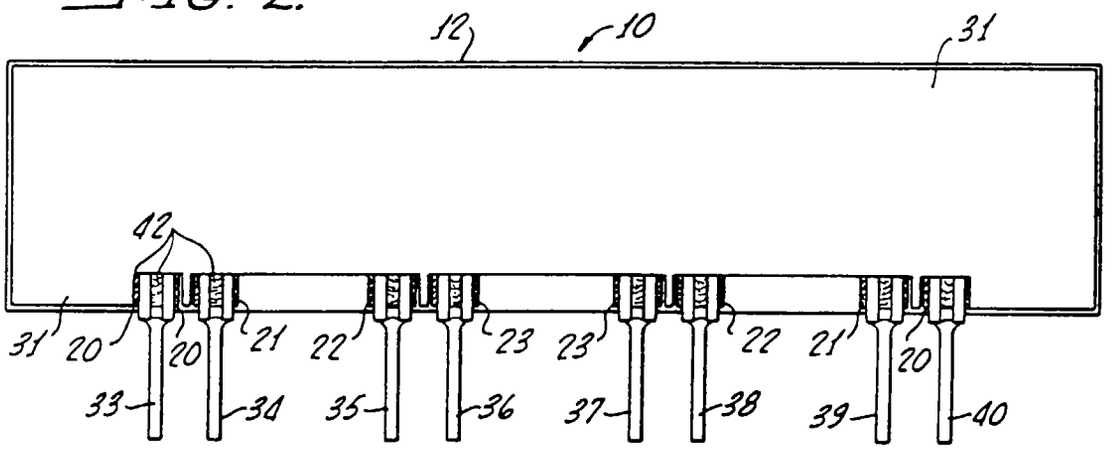


FIG. 3.

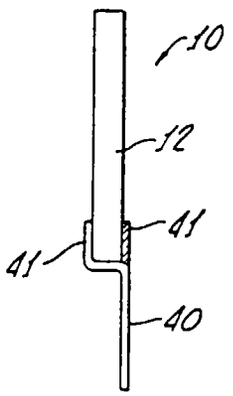


FIG. 14.

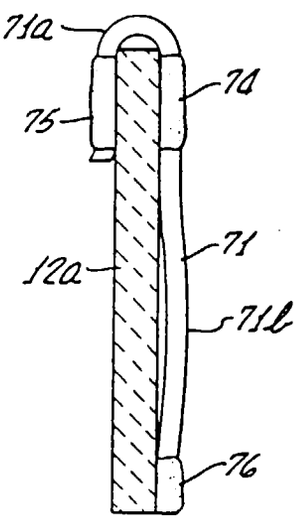


FIG. 15.

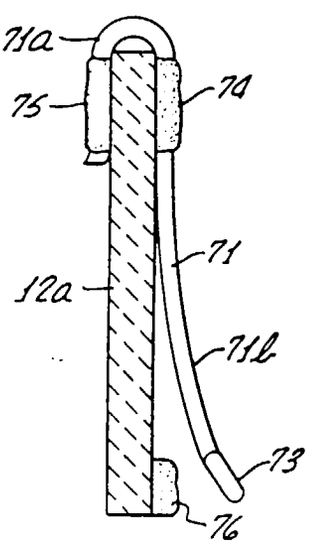


FIG. 4.

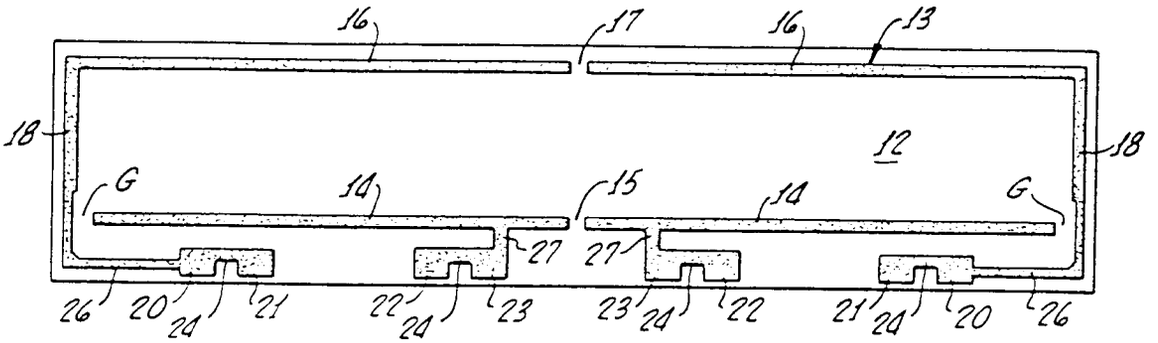


FIG. 5.

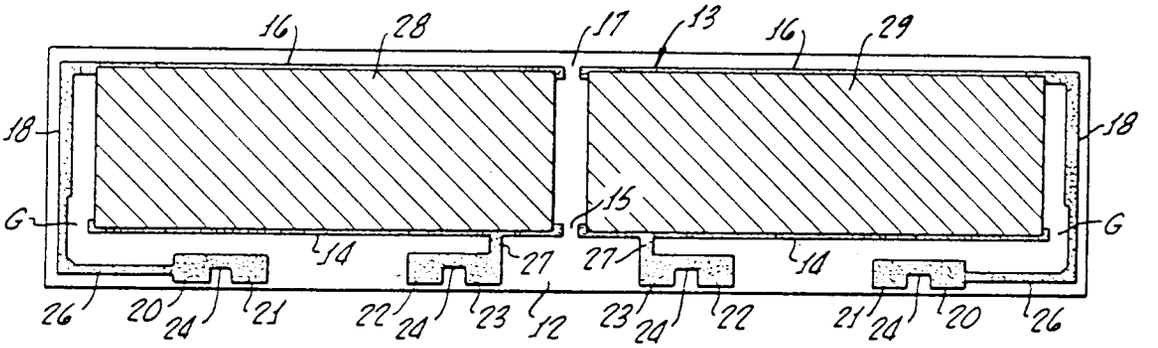
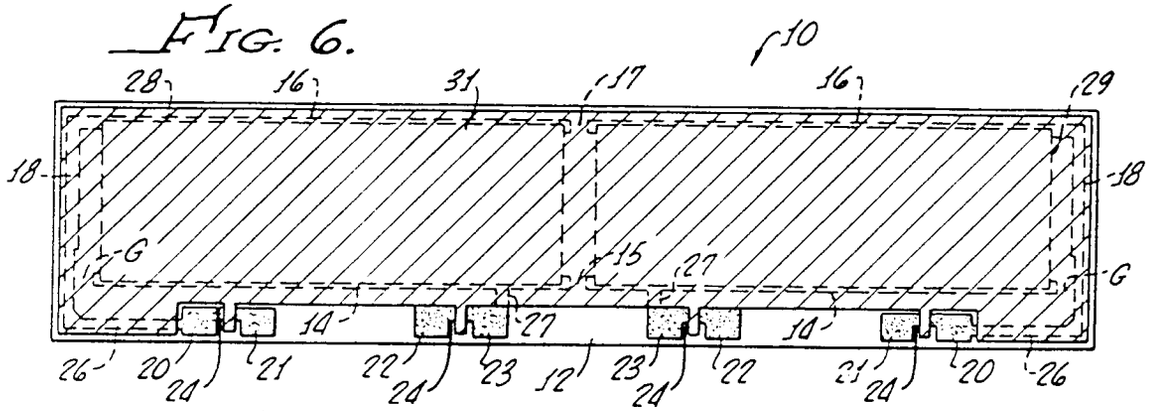


FIG. 6.



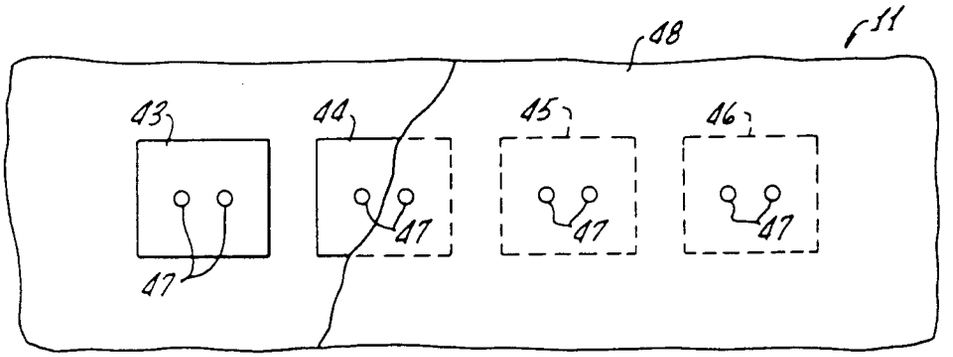


FIG. 7.

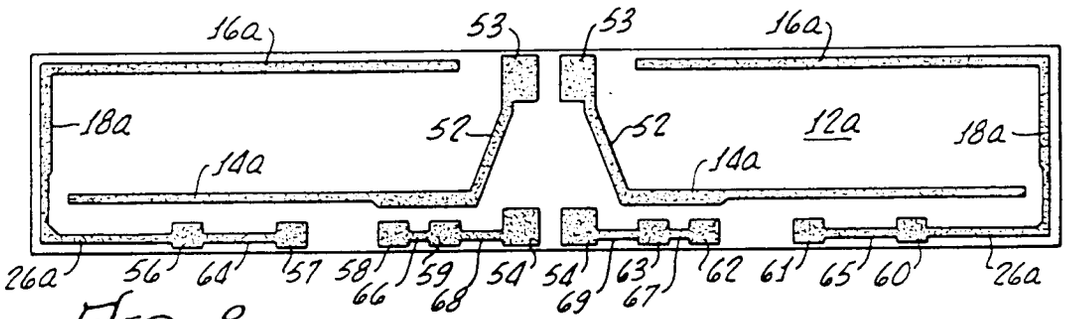


FIG. 8.

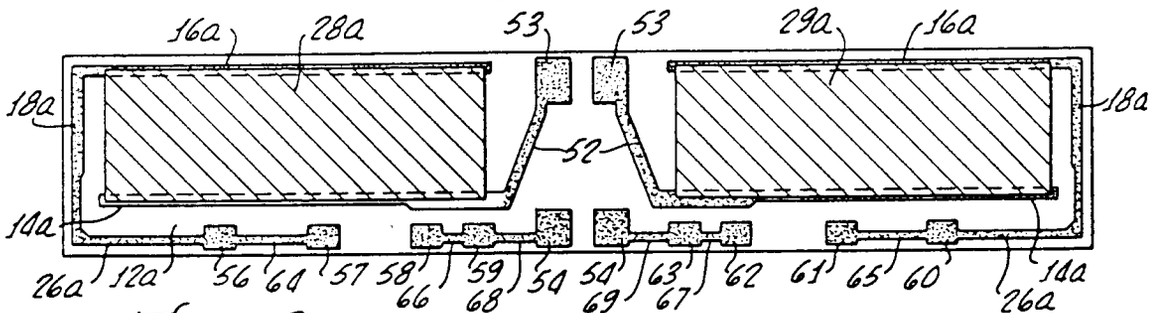


FIG. 9.

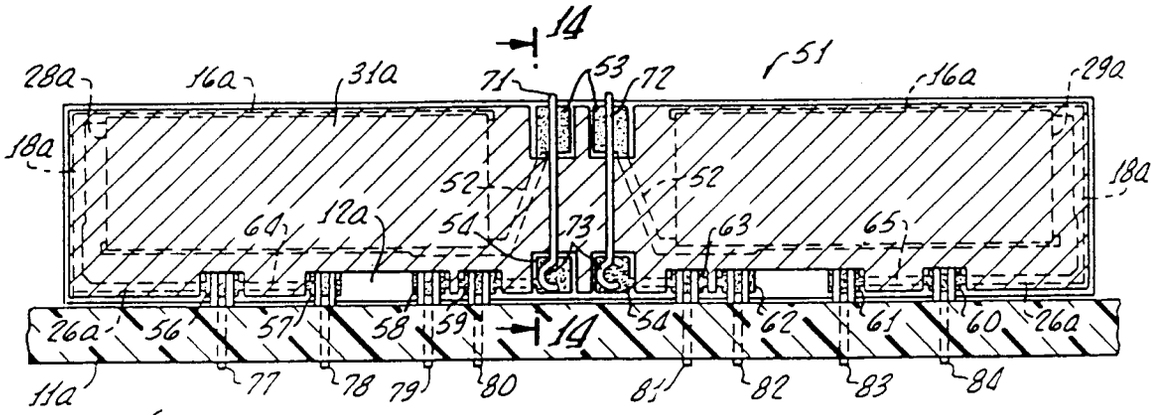


FIG. 10.

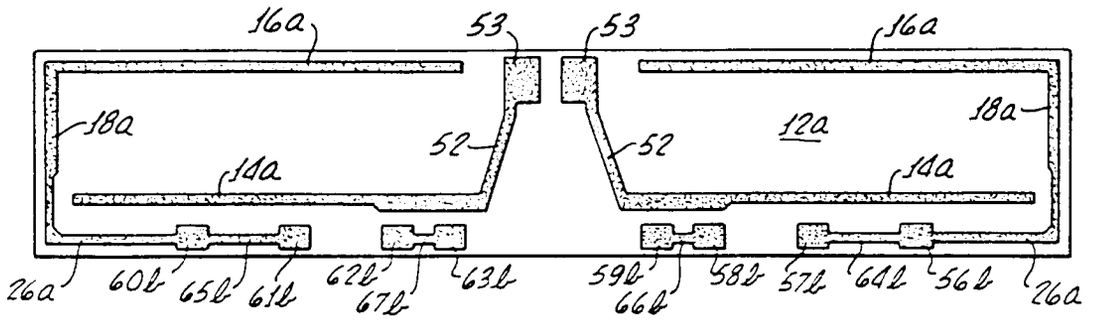


FIG. 11.

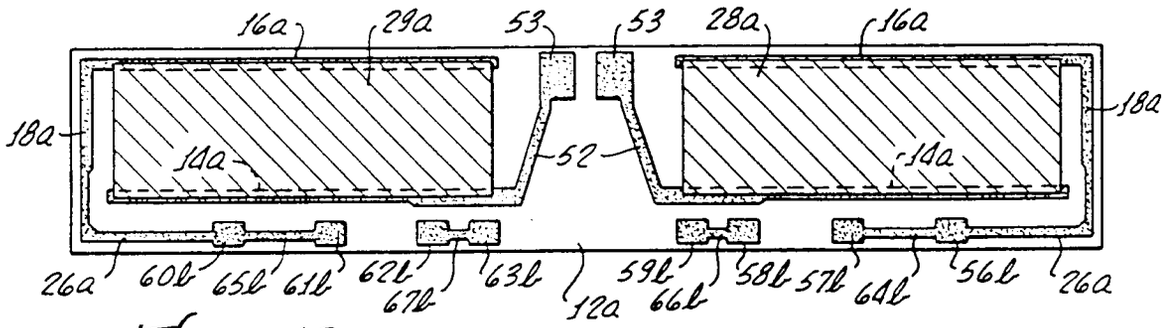


FIG. 12.

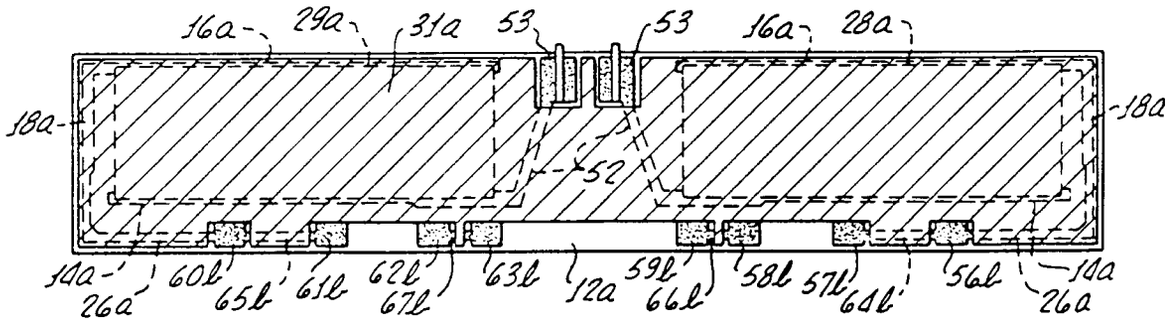


FIG. 13.

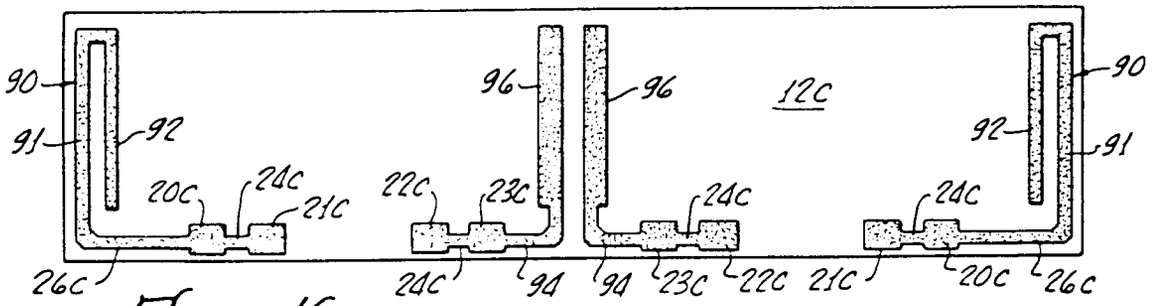


FIG. 16

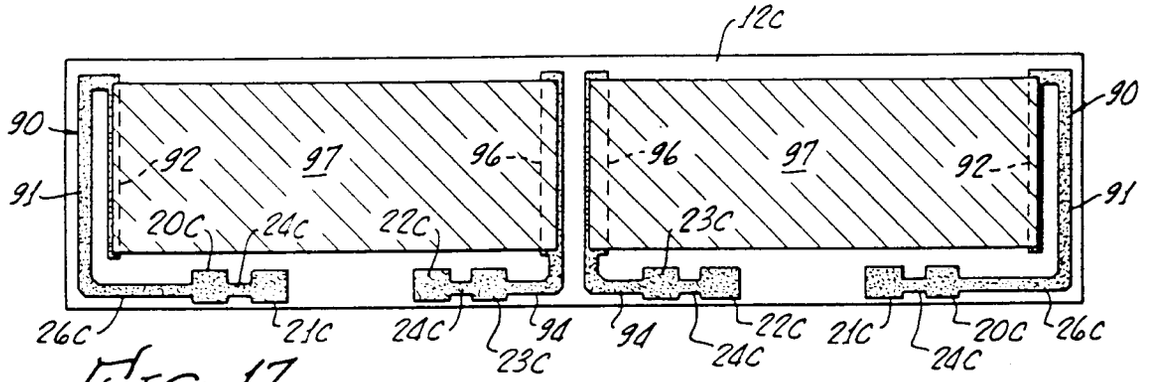


FIG. 17

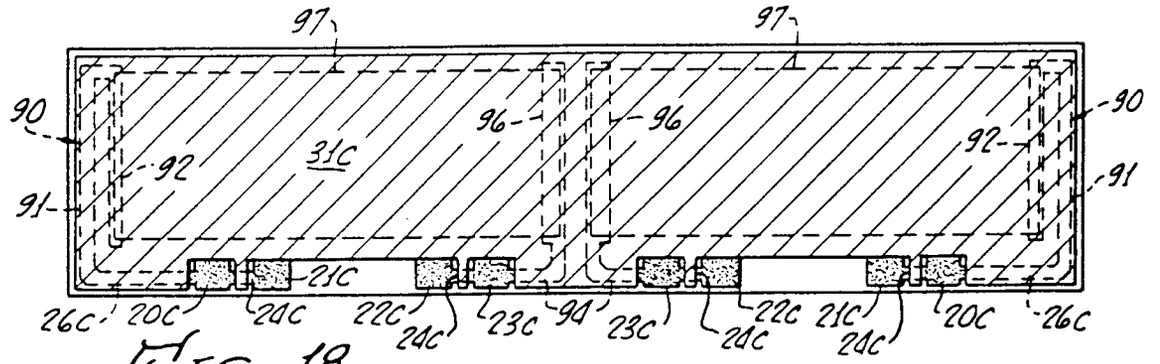


FIG. 18

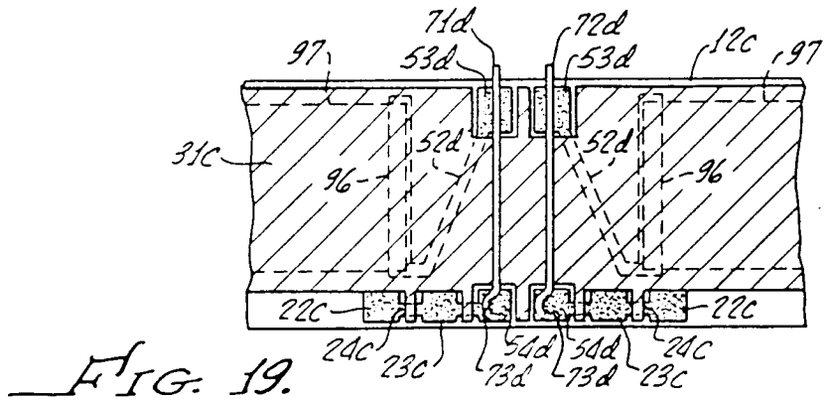


FIG. 19

European Patent Office

EUROPEAN SEARCH REPORT

Application Number EP 97104766.7

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A,D	EP - A - 0 395 231 (GEC PLESSEY TELECOMMUNICATIONS) * Totality * --	1,6	H 01 H 85/046 H 01 C 7/12
A,D	GB - A - 2 163 307 (CRYSTALATE ELECTRONICS) * Totality * --	1,6	
A	DE - A - 2 109 760 (TELEFONAKTIEBOLAGET LM ERICSSON) * Description * --	1,11	
A	DE - A - 3 245 629 (TELEFUNKEN ELECTRONIC) * Description * ----	1,2,11	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

H 01 H 85/00
H 01 C 7/00

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
VIENNA	26-05-1997	ZUGAREK

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

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