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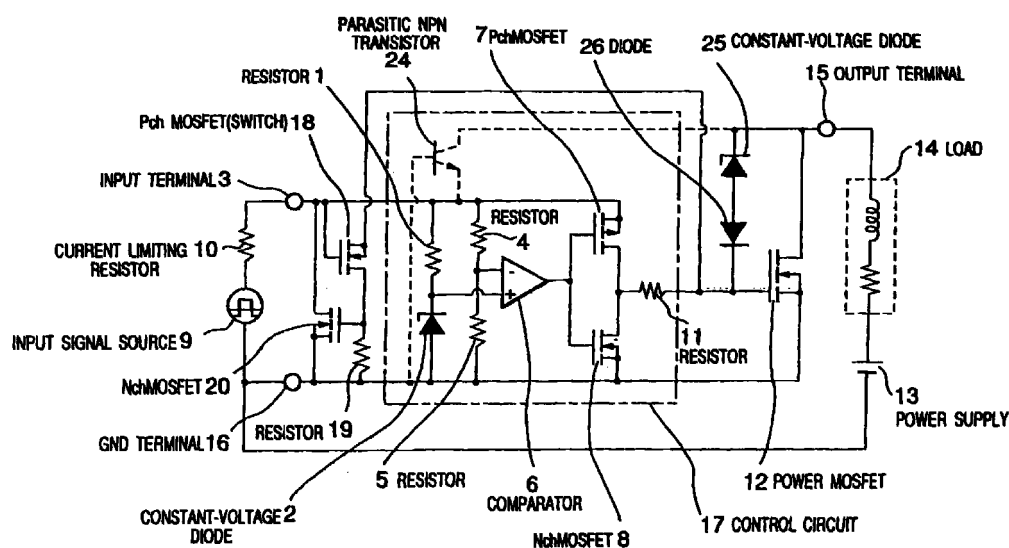
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(54) **Semiconductor device having power MOS transistor including parasitic transistor**

(57) A semiconductor device has a power MOSFET (12) connected between a semiconductor substrate (21) of N-type as an output terminal (15) and a GND terminal (16) connected to a first semiconductor layer (22) formed on the semiconductor substrate (21) and having a gate connected to a first node for controlling the supply of electric current to a load connected between the GND terminal and the output terminal, a control circuit receiving an input signal and controlling an operation of

the power MOSFET in response to the input signal, an input terminal provided in a second semiconductor layer (23) of N-type formed on the first semiconductor layer (22), a parasitic transistor (24) connected between the semiconductor substrate and the second semiconductor layer, and having a base connected to the first semiconductor layer, and switching circuit for keeping the parasitic transistor at a non-conductive state.

**FIG. 1**





European Patent  
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# EUROPEAN SEARCH REPORT

Application Number  
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Place of search THE HAGUE		Date of completion of the search 22 December 1999	Examiner Wirner, C
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