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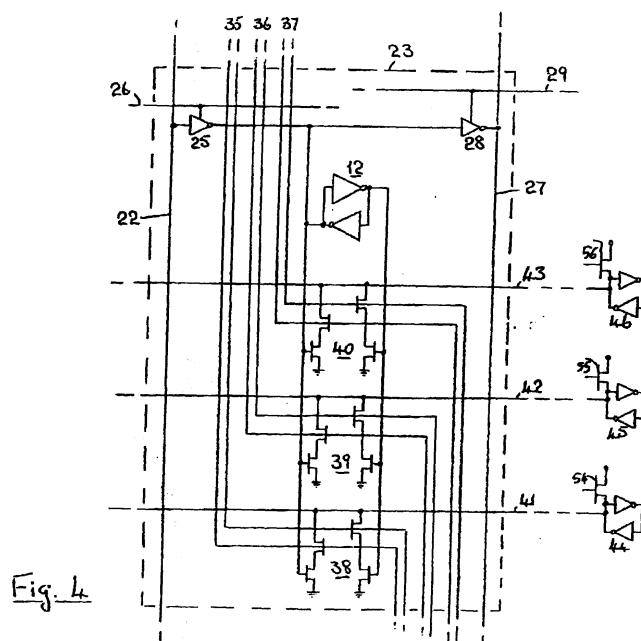
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(54) **Contents addressable memories**

(57) Each cell 23 of a contents addressable memory (CAM) comprises three comparator circuits 38, 39, 40 and respective latches 44, 45, 46. This arrangement allows three simultaneous comparison operations to be carried out against a bit value stored in memory element 12. Also, read access path 27 and write access path 22

are separate from the access paths 35, 36, 37 used for comparison purposes. In this way, read, write and comparison operations can be carried out contemporaneously, though not to the same row, allowing updating of cells 23 with minimum disruption to the CAM's operation.





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Office

EUROPEAN SEARCH REPORT

Application Number  
EP 97 30 2537

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
D,A	GB 2 277 617 A (PLESSEY SEMICONDUCTORS LTD) 2 November 1994 * figures 3,4 * -----	1	G11C15/04
			TECHNICAL FIELDS SEARCHED (Int.Cl.6)
			G11C
The present search report has been drawn up for all claims			
Place of search	Date of completion of the search	Examiner	
THE HAGUE	27 January 1999	Wolff, N	
CATEGORY OF CITED DOCUMENTS		T : theory or principle underlying the invention	
X : particularly relevant if taken alone		E : earlier patent document, but published on, or after the filing date	
Y : particularly relevant if combined with another document of the same category		D : document cited in the application	
A : technological background		L : document cited for other reasons	
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P : intermediate document		& : member of the same patent family, corresponding document	

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