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(54) Strobe select circuit

(57) The present invention is an apparatus and method for implementing a timer using a strobe selection circuit (7) which in turn is implemented using digital components. The strobe selection circuit (7) includes RS latches (90, 92, 94 and 96) which are set to select between input signals (10, 12, 14 and 16) to generate a clock output (62) when a reset signal (18) is de-asserted.

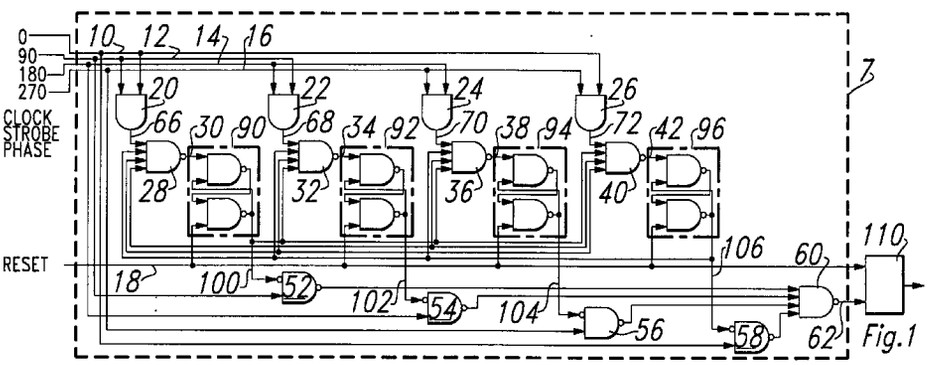

Fig.1

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Description

TECHNICAL FIELD OF THE INVENTION

The present invention relates generally to digital devices and more particularly to the implementation of timing circuitry using digital devices.

BACKGROUND OF THE INVENTION

IC fabrication processes tend to be targeted at one of two applications. Some allow chips to be made with precision passive components (resistors, capacitors, etc.) while others allow very dense areas of transistors to be placed. The former are required for chips with a mostly analogue function and will use Bipolar (and maybe MOSFET) transistors. The latter are targeted at large digital chips and will use MOSFET transistors exclusively.

When producing mixed signal chips with both analogue and digital functional blocks a decision must be taken as to which process is best suited. This is most likely to be governed by the relative quantity of each type of circuit.

When a large digital device is to incorporate a small analogue section, ways must be found around the inadequacy of the process' passive components, either by careful analogue circuit design or by mimicing analogue functions using digital techniques.

SUMMARY OF THE INVENTION

The present invention provides an implementation of timing circuits, which are specified by a minimum and maximum value and intended for analogue implementation, using a digital counter and a clock signal of varying phase thus eliminating the need for passive components.

BRIEF DESCRIPTION OF THE DRAWINGS

Other aspects of the invention and their advantages will be discerned when one refers to the following detailed description as taken in conjunction with the drawings, in which like numbers identify like parts and in which:

Fig. 1 is a circuit diagram of one embodiment of a strobe selection circuit in accordance with the present invention;
Fig.2 is a circuit diagram of a second embodiment of a strobe selection circuit in accordance with the present invention;
Figs.3A-D illustrate several exemplary input clock strobe waveforms;
Figs.4A-D show several exemplary waveforms which illustrate the results of performing AND operations on pairs of the waveforms shown in Figs. 3A-D; and
Figs.5A-G depict waveforms illustrating selection of the strobe.

DETAILED DESCRIPTION OF THE INVENTION

One embodiment of the present invention as shown in Fig.1 includes a strobe select circuit 7 which uses several input clock signals 10, 12, 14 and 16 having the same frequency, but differing phases to implement a timing circuit. These input clock signals 10, 12, 14 and 16 are produced by various techniques including a Delay Locked Loop with multiple variable-delay stages, or by creating increasing delay paths for a single input clock signal. The former technique provides for evenly separated phases, while the latter, although much simpler to design, is subject to process, temperature, and voltage level variations. Other methods for producing the input clock signals 10, 12, 14 and 16 will be readily apparent to those skilled in the art.

The number of input clock signals used is determined by the accuracy requirements of the application and by the frequency of a base clock, not shown, from which the input clock signals 10, 12, 14 and 16 are derived. The frequency must be a multiple of the shortest timer needed, i.e., if a timer of 50ns (+/-5ns) is needed, then a 10ns or 25ns period is appropriate but a 33ns period is not. Continuing with this example, the range of the exemplary timer is 45-55ns, i.e. 10ns. Thus, for a 25ns period clock, 2 phases give a resolution of 12.5ns, but 4 phases, which give a resolution of 6.25ns, are chosen to allow for subsequent gate delays. The strobe selection circuits 7 and 9 illustrating the present invention, as shown in Figs. 1 and 2, respectively and as described in more detail hereinbelow, use the four input clock phases 0°, 90°, 180° and 270°.

The Strobe Select Circuits 7 and 9 in accordance with the present invention and as shown in Figs. 1 and 2, respectively, have 5 inputs and 1 output. An asserted reset signal 18 holds the circuit 7 or 9 in a reset state, with the output signal at 62 in Fig. 1 and at 64 in Fig. 2 held low. Four RS latches 90, 92, 94 and 96 are held reset (where their outputs are HIGH) using this reset signal 18. The reset circuits 7 and 9 may be arranged for the signal 18 to be active HIGH or

active LOW.

Four clock strobes (input signals 10, 12, 14 and 16) are used in the circuits 7 and 9 shown in Figures 1 and 2, respectively, and are called stb0, stb90, stb180 and stb270, respectively, (the numbers referring to their relative phase to the base clock, not shown, from which they are derived). The waveforms associated with each of these strobes are shown in Figs. 3A-D, respectively.

Each pair of adjacent strobes (i.e. a pair of strobes separated by 90 degrees) are AND-ed together to give four signals 66, 68, 70 and 72, the respective waveforms of which are shown in Figs. 4A-D, respectively, only one of which is HIGH at any one time. Each of these signals 66, 68, 70 and 72 are associated with one of the RS latches 90, 92, 94 and 96.

The number of adjacent strobes AND-ed together so that only one of the combinations is HIGH at any one time depends on the number of input clock strobes used. As an example, if eight clock strobes are used instead of four, four adjacent clock strobes are AND-ed together to give eight signals, only one of which is HIGH at any one time.

The set input 30 for the RS latch 90 is the NAND 28 of the signal 66 and the output signals 102, 104 and 106 of the other three RS latches 92, 94 and 96. NAND gates 32, 36 and 40 are similarly used to generate the set inputs 34, 38 and 42 for the RS latches 92, 94 and 96, respectively.

Functionally, when the reset signal 18 is deasserted, the waveform of which is shown in Fig.5A, the RS latches 90, 92, 94 and 96 are able to be set. However, due to the NAND gates 28, 32, 36 and 40 on the set inputs 30, 34, 38 and 42 of the RS latches 90, 92, 94 and 96, only one gets set, as shown by the exemplary waveform in Fig.5C, namely the one associated with the two strobe inputs 10 and 12, 12 and 14, 14 and 16, or 16 and 10 which are both HIGH. In the exemplary waveform shown in Fig.5B, the strobe inputs which are 90 and 180 out of phase from the base clock are selected. When this RS latch 90, 92, 94 or 96 sets, its output signal 100, 102, 104 or 106 goes LOW which feeds into the NAND gates 28, 32, 36 and 40, respectively, on the other three RS latches and prevents them from being able to be set. So only one RS latch 90, 92, 94 or 96 will ever have its output signal 100, 102, 104 or 106 LOW.

The output signals 100, 102, 104 and 106 of the four RS latches 90, 92, 94 and 96, respectively, are inverted and fed into NAND gates 52, 54, 56 and 58 respectively, along with one of the input strobes 10, 12, 14 or 16. The RS latch 90, 92, 94 or 96 which is set enables its associated strobe signal 10, 12, 14 or 16 to traverse the NAND gate 52, 54, 56 or 58. The outputs of all four NAND gates 52, 54, 56 and 58 pass through another NAND gate 62 (which, by DeMorgan's Theorem implements an OR function) to give the output clock signal 62 in the first embodiment shown in Fig.1 and to give the output clock signal 64 in the second embodiment shown in Fig. 2.

Two embodiments of the strobe selection circuit 7 and 9 are shown in Figs. 1 and 2, respectively, the difference being in which strobe signal 10, 12, 14 or 16 gets selected by which RS latch 90, 92, 94 or 96. In order to avoid glitches, the strobe signal 10, 12, 14 or 16 selected to the output 62 or 64 must either be (upto) halfway through its LOW period, as illustrated by the waveform in Fig.5D, or (upto) halfway HIGH as illustrated by the waveform shown in Fig.5E (the other two could be transitioning LOW to HIGH or HIGH to LOW at this time which gives a very short glitch on the output clock signal 62 or 64), the waveforms of which are shown in Figs.5F and 5G, respectively.

Thus, in the second embodiment of the present invention as shown in Fig.2, the order of the clock strobes 10, 12, 14 and 16 into the NAND gates 52, 54, 56 and 58 is changed.

The final component of a timer in accordance with the present invention is a synchronous count-down counter 110. The counter 110 is held reset by the same reset signal 18 as the strobe select circuits 7 and 9 shown in Figs.1 and 2, respectively. When the reset signal 18 is removed, the counter 110 counts down with each clock edge output 62 or 64 from the strobe select circuits 7 or 9 shown in Figs.1 and 2, respectively.

Assuming rising edge logic, the delay to the first rising edge is either upto half a cycle minus delay through two NAND gates, and fanout into the counter in the circuit shown in Fig.1, or just these gate delays in the circuit shown in Fig.2.

DESIGN EXAMPLE: Timer in the range 70-90ns.

Use a 25ns period clock, with four strobes 6.25ns apart.

Using the circuit 9 shown in Fig.2, with a 3 down to 0 counter 110:

When the reset signal 18 is removed, the edge appears instantly. The output signal 64 is high for 6.25-12.5ns. It is then low for 12.5ns, and edges appear at 25ns intervals after that.

$$\text{Minimum} = 6.25\text{ns} + 12.5\text{ns} + 3 \times 25\text{ns} = 93.75\text{ns}$$

$$\text{Maximum} = 12.5\text{ns} + 12.5\text{ns} + 3 \times 25\text{ns} = 100\text{ns}$$

This is no good as it is out of range. Alternatively, try the circuit 7 shown in Fig.1.

In the circuit 7 shown in Fig.1, with a 3 down to 0 counter 110:

When the reset signal 18 is removed, the edge appears instantly. The output clock signal 62 is low for 6.25-12.5ns. Edges then appear at 25ns intervals.

Minimum = 6.25ns + 3 x 25ns = 81.25ns

Maximum = 12.5ns + 3 x 25ns = 87.5ns

This lies easily within the 70-90ns range, and is thus suitable for this exemplary application.

Claims

1. Apparatus implementing a timer comprising:

   selection circuitry for selecting from a plurality of input strobe signals to generate an output clock signal; and
   a counter coupled to said selection circuitry and operable to count down a predetermined amount of time in response to each said output clock signal.

2. The apparatus of Claim 1 wherein each of said input strobe signals has an associated frequency and phase and wherein said associated frequency of each of said input strobe signals is equal to a base frequency and wherein said associated phase of each of said input strobe signals is an offset from a base phase.

3. The apparatus of Claim 2 wherein said selection circuitry includes a plurality of latch circuits, each of said latch circuits having a set input and a reset input, said set input responsive to one of a plurality of combinations of said input strobe signals and output signals from all other of said latch circuits, said reset input responsive to a reset signal.

4. The apparatus of Claim 3 wherein only one of said plurality of combinations of said input strobe signals is asserted at any one time.

5. The apparatus of Claim 4 wherein said reset signal is asserted and wherein said each of said latch circuits is operable to generate a latch output signal and to inhibit said other of said latch circuits from being set in response to said one of said combinations of said input strobe signals being asserted and said reset signal being de-asserted.

6. The apparatus of Claim 5 wherein said selection circuitry further includes circuitry for combining said latch output signal with one of said input strobe signals to generate said output clock signal.

7. The method of Claim 6 wherein said combining circuitry is further operable to combine said latch output signal with said one of said input strobe signals which is not near one of its transition times.

8. A method of implementing a timer, using a base clock, the base clock having an associated frequency and phase, using a plurality of input strobe signals, a reset signal, and a plurality of latch circuits, each of said input strobe signals having an associated frequency equal to the base clock frequency and an associated phase equal to the base clock phase plus an associated offset, each of said latch circuits having an associated set input and reset input and operable to generate a latch output signal, the method comprising the steps of:

   combining selected ones of the input strobe signals to generate a plurality of latch input signals;
   associating each of said latch input signals with the set input of one of the latch circuits;
   associating the latch output signals from said one of the latch circuits to the set input of all other of the latch circuits;
   de-asserting the reset signal at the reset input of the latch circuits to enable the latch circuits to be set;
   combining the latch output associated with said one of the latch circuits with one of the input strobe signals to generate an output clock signal; and
   associating said output clock signal with an input of a counter, said counter held reset by the reset signal and operable to count down with each said output clock signal in response to said de-asserting step.

9. The method of Claim 8 wherein said step of combining selected ones of the input strobe signals includes the step of combining selected ones of the input strobe signals so that only said one of said latch input signals is high at any one time.

10. The method of Claim 9 wherein said step of combining the latch output includes the step of combining the latch output associated with said one of the latch circuits with said one of the input strobe signals which is not near one of its transition times.

11. The method of Claim 10 wherein said step of combining the latch output includes the step of combining the latch output associated with said one of the latch circuits with said one of the input strobe signals which is halfway through its high period.

12. The method of Claim 10 wherein said step of combining the latch output includes the step of combining the latch output associated with said one of the latch circuits with said one of the input strobe signals which is halfway through its low period.

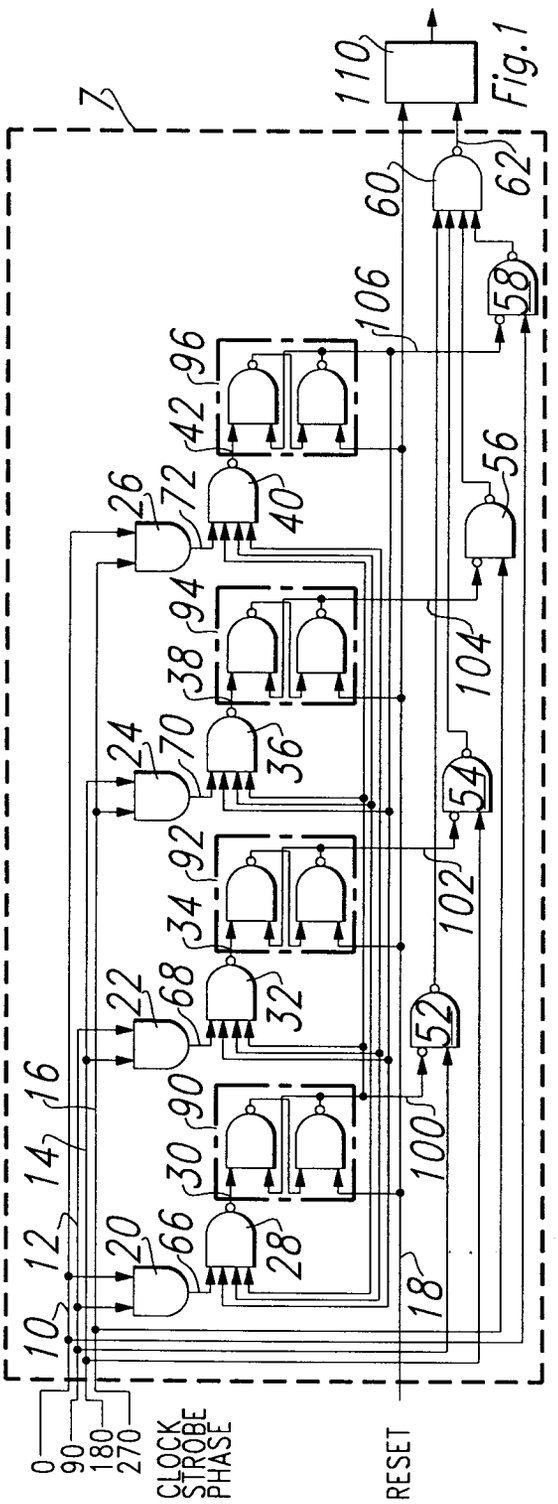
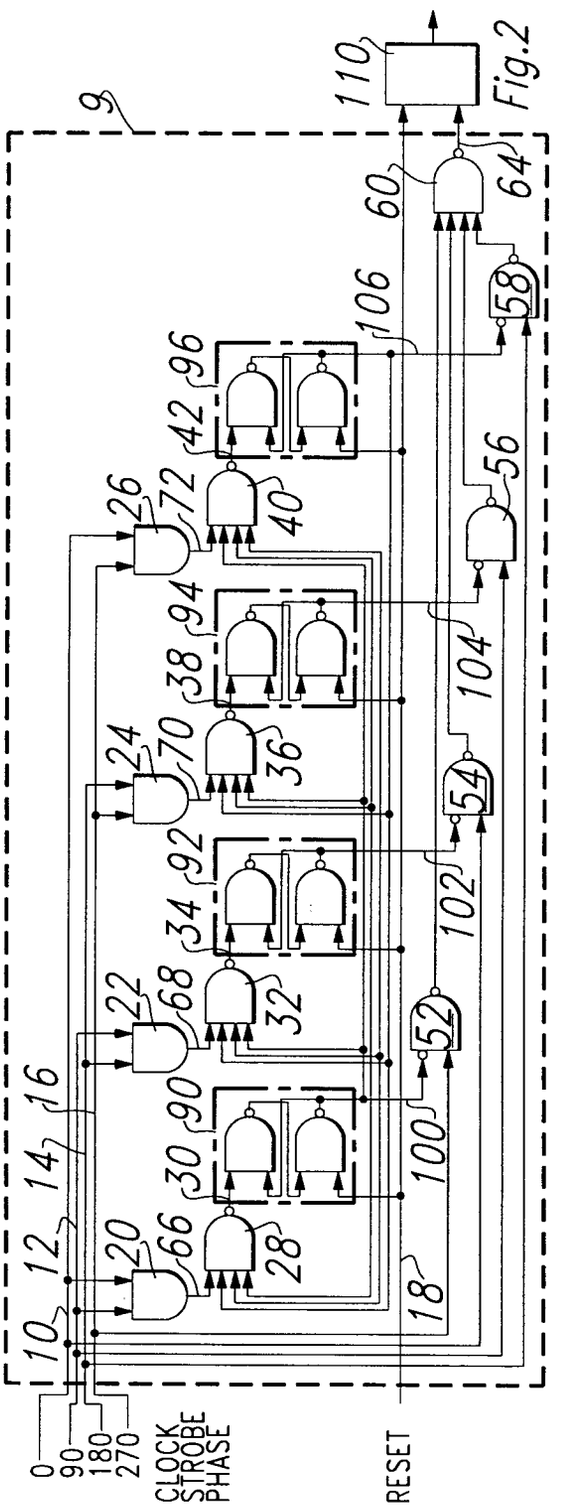

7
110
60
62
58
106
96
42
56
26
72
40
94
38
104
24
70
36
54
92
34
102
22
68
32
52
90
30
100
16
14
12
20
66
28
18
10
0
90
180
270
CLOCK
STROBE
PHASE
RESET

Fig.1


9
110
60
64
58
106
96
42
56
26
72
40
94
38
104
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70
36
54
92
34
102
22
68
32
52
90
30
100
16
14
12
20
66
28
18
10
0
90
180
270
CLOCK
STROBE
PHASE
RESET

Fig.2

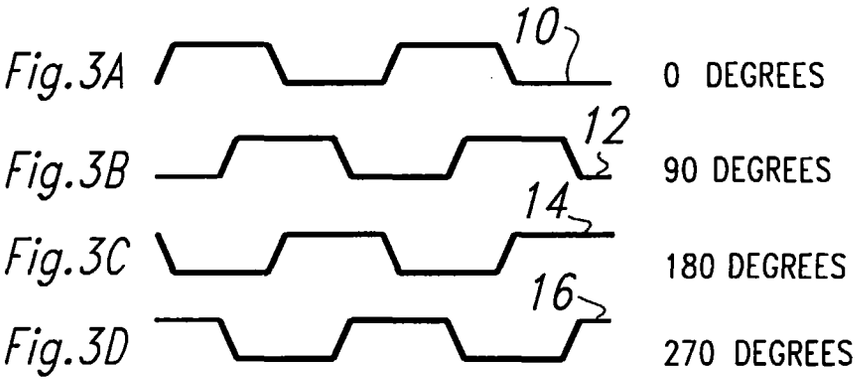
Fig.3A
10
0 DEGREES
Fig.3B
12
90 DEGREES
Fig.3C
14
180 DEGREES
Fig.3D
16
270 DEGREES

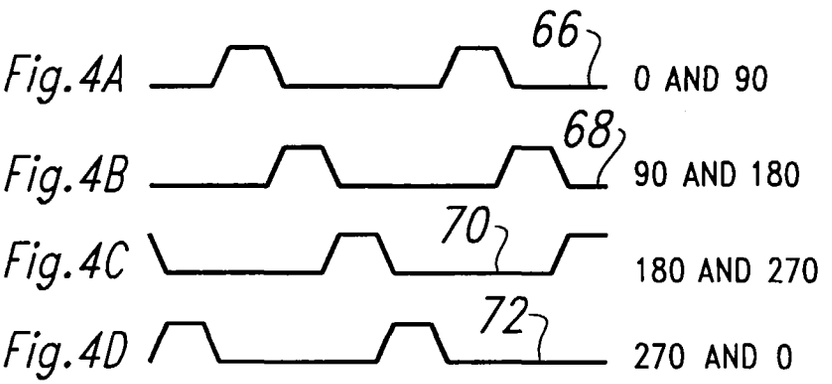
Fig.4A
66
0 AND 90
Fig.4B
68
90 AND 180
Fig.4C
70
180 AND 270
Fig.4D
72
270 AND 0

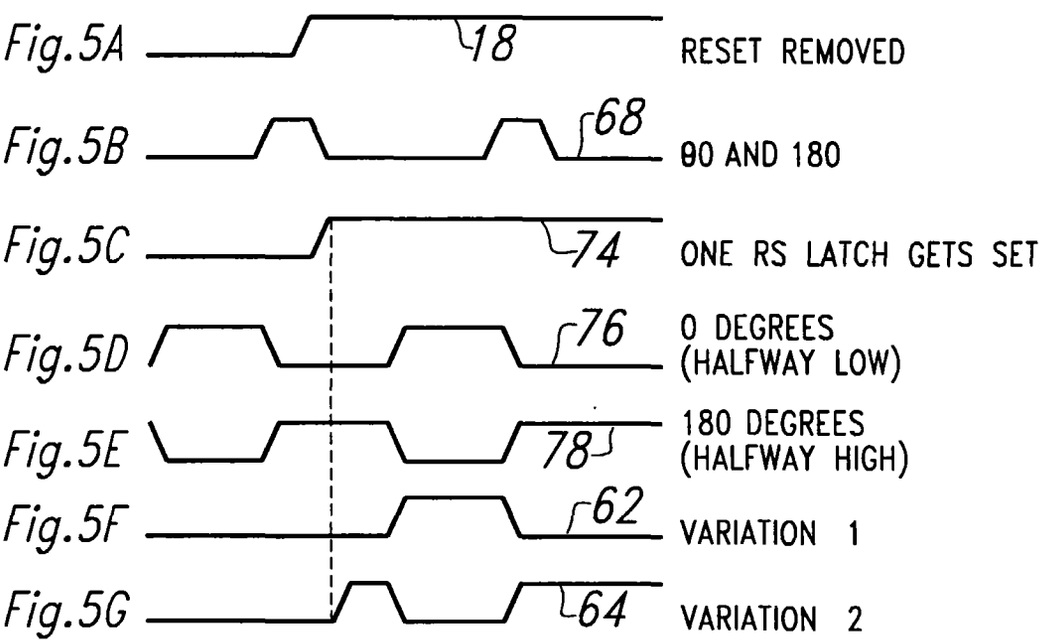
Fig.5A
18
RESET REMOVED
Fig.5B
68
90 AND 180
Fig.5C
74
ONE RS LATCH GETS SET
Fig.5D
76
0 DEGREES
(HALFWAY LOW)
Fig.5E
78
180 DEGREES
(HALFWAY HIGH)
Fig.5F
62
VARIATION 1
Fig.5G
64
VARIATION 2

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EUROPEAN SEARCH REPORT

Application Number
EP 96 10 7337

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
Y	US-A-3 502 991 (SAMPSON SIDNEY F) 24 March 1970 * column 2, line 59 - column 5, line 39 *	1-12	G04F1/00
Y	WESCON TECHNICAL PAPERS, vol. 18, no. 27/4, 1974, NORTH HOLLYWOOD, pages 1-7, XP002016552 Z. TARZY-HORNOCH: "Some nanosecond and subnanosecond resoltution timing techniques." * page 5, left-hand column, last paragraph - page 6, right-hand column, paragraph 1; figure 6 *	1-12	
Y	IBM TECHNICAL DISCLOSURE BULLETIN, vol. 16, no. 7, December 1973, NEW YORK, pages 2087-2089, XP002016553 S. BOÏNODIRIS: "Clock synchronisation for counting time intervals." * page 2087, last paragraph - page 2088, line 4; figures 1,2 *	1-12	
A	PATENT ABSTRACTS OF JAPAN vol. 008, no. 021 (E-224), 28 January 1984 & JP-A-58 184886 (NIPPON HOSO KYOKAI), 28 October 1983, * abstract *	1-12	TECHNICAL FIELDS SEARCHED (Int.Cl.6) G04F
A	US-A-2 928 045 (R.C. RENICK ET AL.) 8 March 1960 * figures 1-5 *	1-12	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	22 October 1996	Exelmans, U

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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