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(54) **Strobe select circuit**

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Circuit de sélection de cadence

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(56) References cited:
US-A- 2 928 045 **US-A- 3 502 991**

- **WESCON TECHNICAL PAPERS, vol. 18, no. 27/4, 1974, NORTH HOLLYWOOD, pages 1-7, XP002016552 Z. TARZY-HORNOCH: "Some nanosecond and subnanosecond resolution timing techniques."**
- **IBM TECHNICAL DISCLOSURE BULLETIN, vol. 16, no. 7, December 1973, NEW YORK, pages 2087-2089, XP002016553 S. BO NODIRIS: "Clock synchronisation for counting time intervals."**
- **PATENT ABSTRACTS OF JAPAN vol. 008, no. 021 (E-224), 28 January 1984 & JP-A-58 184886 (NIPPON HOSO KYOKAI), 28 October 1983,**

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Description

TECHNICAL FIELD OF THE INVENTION

[0001] The present invention relates generally to digital devices and more particularly to the implementation of timing circuitry using digital devices.

BACKGROUND OF THE INVENTION

[0002] IC fabrication processes tend to be targeted at one of two applications. Some allow chips to be made with precision passive components (resistors, capacitors, etc.) while others allow very dense areas of transistors to be placed. The former are required for chips with a mostly analogue function and will use Bipolar (and maybe MOSFET) transistors. The latter are targeted at large digital chips and will use MOSFET transistors exclusively.

[0003] When producing mixed signal chips with both analogue and digital functional blocks a decision must be taken as to which process is best suited. This is most likely to be governed by the relative quantity of each type of circuit.

[0004] When a large digital device is to incorporate a small analogue section, ways must be found around the inadequacy of the process' passive components, either by careful analogue circuit design or by mimicking analogue functions using digital techniques.

SUMMARY OF THE INVENTION

[0005] The present invention provides an implementation of timing circuits, which are specified by a minimum and maximum value and intended for analogue implementation, using a digital counter and a clock signal of varying phase thus eliminating the need for passive components.

[0006] US-A-3 502 991 discloses an apparatus implementing a timer comprising selection circuitry for selecting from a plurality of input strobe signals to generate an output clock signal, and a counter coupled to said selection circuitry and operable to count a predetermined amount of time in response to said output clock signal.

[0007] WESCON TECHNICAL PAPERS, vol. 18, no. 27/4, 1974, NORTH HOLLYWOOD, pages 1-7 XP002016552 Z. TARZY-HORNOCH: "Some nanosecond and sub-nanosecond resolution timing techniques" discloses a slice-free rate limiter to not more than one pulse per time T with a phase-locked clock for delay generation whose start time pulse T clocks and through delays reclocks the flip-flops so that they store a pattern representative of the nearest phase to the start time.

[0008] IBM TECHNICAL DISCLOSURE BULLETIN, vol. 16, no. 7, December 1973, NEW YORK, pages 2087-2089, XP 002016553 S. BOINDIRIS: 'Clock synchronisation for counting timer intervals discloses im-

provements in the accuracy of the asynchronous time interval measurement by phase splitting of the clock pulses counted for this measurement, and to compensate for circuit delay, clock pulse outputs are correlated to slightly delayed pulses by an additional increment.

[0009] The present invention alleviates the inadequacy of the passive components of the IC chips produced, by careful analogue circuit design and by mimicking analogue functions using digital techniques when a large digital device is to incorporate a small analogue selection during the production of mixed signal IC chips with both analogue and digital functional blocks. This is achieved by an apparatus implementing a timer comprising selection circuitry for electing from a plurality of input strobe signals to generate an output clock signal, and a counter coupled to said selection circuitry and operable to count a predetermined amount of time in response to said output clock signal which is built according to the characterising part of claim 1.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] Other aspects of the invention and their advantages will be discerned when one refers to the following detailed description as taken in conjunction with the drawings, in which like numbers identify like parts and in which:

Fig. 1 is a circuit diagram of one embodiment of a strobe selection circuit in accordance with the present invention;

Fig.2 is a circuit diagram of a second embodiment of a strobe selection circuit in accordance with the present invention;

Figs.3A-D illustrate several exemplary input clock strobe waveforms;

Figs.4A-D show several exemplary waveforms which illustrate the results of performing AND operations on pairs of the waveforms shown in Figs. 3A-D; and

Figs.5A-G depict waveforms illustrating selection of the strobe.

DETAILED DESCRIPTION OF THE INVENTION

[0011] One embodiment of the present invention as shown in Fig.1 includes a strobe select circuit 7 which uses several input clock signals 10, 12, 14 and 16 having the same frequency, but differing phases to implement a timing circuit. These input clock signals 10, 12, 14 and 16 are produced by various techniques including a Delay Locked Loop with multiple variable-delay stages, or by creating increasing delay paths for a single input clock signal. The former technique provides for evenly separated phases, while the latter, although much simpler to design, is subject to process, temperature, and voltage level variations. Other methods for producing the input clock signals 10, 12, 14 and 16 will

be readily apparent to those skilled in the art.

[0012] The number of input clock signals used is determined by the accuracy requirements of the application and by the frequency of a base clock, not shown, from which the input clock signals 10, 12, 14 and 16 are derived. The frequency must be a multiple of the shortest timer needed, i.e., if a timer of 50ns (+/-5ns) is needed, then a 10ns or 25ns period is appropriate but a 33ns period is not. Continuing with this example, the range of the exemplary timer is 45-55ns, i.e. 10ns. Thus, for a 25ns period clock, 2 phases give a resolution of 12.5ns, but 4 phases, which give a resolution of 6.25ns, are chosen to allow for subsequent gate delays. The strobe selection circuits 7 and 9 illustrating the present invention, as shown in Figs. 1 and 2, respectively and as described in more detail hereinbelow, use the four input clock phases 0°, 90°, 180° and 270°.

[0013] The Strobe Select Circuits 7 and 9 in accordance with the present invention and as shown in Figs. 1 and 2, respectively, have 5 inputs and 1 output. An asserted reset signal 18 holds the circuit 7 or 9 in a reset state, with the output signal at 62 in Fig. 1 and at 64 in Fig. 2 held low. Four RS latches 90, 92, 94 and 96 are held reset (where their outputs are HIGH) using this reset signal 18. The reset circuits 7 and 9 may be arranged for the signal 18 to be active HIGH or active LOW.

[0014] Four clock strobes (input signals 10, 12, 14 and 16) are used in the circuits 7 and 9 shown in Figures 1 and 2, respectively, and are called stb0, stb90, stb180 and stb270, respectively, (the numbers referring to their relative phase to the base clock, not shown, from which they are derived). The waveforms associated with each of these strobes are shown in Figs. 3A-D, respectively.

[0015] Each pair of adjacent strobes (i.e. a pair of strobes separated by 90 degrees) are AND-ed together to give four signals 66, 68, 70 and 72, the respective waveforms of which are shown in Figs. 4A-D, respectively, only one of which is HIGH at any one time. Each of these signals 66, 68, 70 and 72 are associated with one of the RS latches 90, 92, 94 and 96.

[0016] The number of adjacent strobes AND-ed together so that only one of the combinations is HIGH at any one time depends on the number of input clock strobes used. As an example, if eight clock strobes are used instead of four, four adjacent clock strobes are AND-ed together to give eight signals, only one of which is HIGH at any one time.

[0017] The set input 30 for the RS latch 90 is the NAND 28 of the signal 66 and the output signals 102, 104 and 106 of the other three RS latches 92, 94 and 96. NAND gates 32, 36 and 40 are similarly used to generate the set inputs 34, 38 and 42 for the RS latches 92, 94 and 96, respectively.

[0018] Functionally, when the reset signal 18 is deasserted, the waveform of which is shown in Fig.5A, the RS latches 90, 92, 94 and 96 are able to be set. However, due to the NAND gates 28, 32, 36 and 40 on the set inputs 30, 34, 38 and 42 of the RS latches 90, 92,

94 and 96, only one gets set, as shown by the exemplary waveform in Fig.5C, namely the one associated with the two strobe inputs 10 and 12, 12 and 14, 14 and 16, or 16 and 10 which are both HIGH. In the exemplary waveform shown in Fig.5B, the strobe inputs which are 90 and 180 out of phase from the base clock are selected. When this RS latch 90, 92, 94 or 96 sets, its output signal 100, 102, 104 or 106 goes LOW which feeds into the NAND gates 28, 32, 36 and 40, respectively, on the other three RS latches and prevents them from being able to be set. So only one RS latch 90, 92, 94 or 96 will ever have its output signal 100, 102, 104 or 106 LOW.

[0019] The output signals 100, 102, 104 and 106 of the four RS latches 90, 92, 94 and 96, respectively, are inverted and fed into NAND gates 52, 54, 56 and 58 respectively, along with one of the input strobes 10, 12, 14 or 16. The RS latch 90, 92, 94 or 96 which is set enables its associated strobe signal 10, 12, 14 or 16 to traverse the NAND gate 52, 54, 56 or 58. The outputs of all four NAND gates 52, 54, 56 and 58 pass through another NAND gate 62 (which, by DeMorgan's Theorem implements an OR function) to give the output clock signal 62 in the first embodiment shown in Fig.1 and to give the output clock signal 64 in the second embodiment shown in Fig.2.

[0020] Two embodiments of the strobe selection circuit 7 and 9 are shown in Figs. 1 and 2, respectively, the difference being in which strobe signal 10, 12, 14 or 16 gets selected by which RS latch 90, 92, 94 or 96. In order to avoid glitches, the strobe signal 10, 12, 14 or 16 selected to the output 62 or 64 must either be (upto) half-way through its LOW period, as illustrated by the waveform in Fig.5D, or (upto) halfway HIGH as illustrated by the waveform shown in Fig.5E (the other two could be transitioning LOW to HIGH or HIGH to LOW at this time which gives a very short glitch on the output clock signal 62 or 64), the waveforms of which are shown in Figs.5F and 5G, respectively.

[0021] Thus, in the second embodiment of the present invention as shown in Fig.2, the order of the clock strobes 10, 12, 14 and 16 into the NAND gates 52, 54, 56 and 58 is changed.

[0022] The final component of a timer in accordance with the present invention is a synchronous count-down counter 110. The counter 110 is held reset by the same reset signal 18 as the strobe select circuits 7 and 9 shown in Figs.1 and 2, respectively. When the reset signal 18 is removed, the counter 110 counts down with each clock edge output 62 or 64 from the strobe select circuits 7 or 9 shown in Figs.1 and 2, respectively.

[0023] Assuming rising edge logic, the delay to the first rising edge is either upto half a cycle minus delay through two NAND gates, and fanout into the counter in the circuit shown in Fig.1, or just these gate delays in the circuit shown in Fig.2.

[0024] DESIGN EXAMPLE: Timer in the range 70-90ns.

[0025] Use a 25ns period clock, with four strobes

6.25ns apart.

[0026] Using the circuit 9 shown in Fig.2, with a 3 down to 0 counter 110:

[0027] When the reset signal 18 is removed, the edge appears instantly. The output signal 64 is high for 6.25-12.5ns. It is then low for 12.5ns, and edges appear at 25ns intervals after that.

$$\text{Minimum} = 6.25\text{ns} + 12.5\text{ns} + 3 \times 25\text{ns} = 93.75\text{ns}$$

$$\text{Maximum} = 12.5\text{ns} + 12.5\text{ns} + 3 \times 25\text{ns} = 100\text{ns}$$

[0028] This is no good as it is out of range. Alternatively, try the circuit 7 shown in Fig.1.

[0029] In the circuit 7 shown in Fig.1, with a 3 down to 0 counter 110:

When the reset signal 18 is removed, the edge appears instantly. The output clock signal 62 is low for 6.25-12.5ns. Edges then appear at 25ns intervals.

$$\text{Minimum} = 6.25\text{ns} + 3 \times 25\text{ns} = 81.25\text{ns}$$

$$\text{Maximum} = 12.5\text{ns} + 3 \times 25\text{ns} = 87.5\text{ns}$$

[0030] This lies easily within the 70-90ns range, and is thus suitable for this exemplary application.

Claims

1. Apparatus for implementing a timer comprising:

selection circuitry (7,9) for selecting from a plurality of input strobe signals (10, 12, 14, 16) to generate an output clock signal (62, 64);
a counter (110) coupled to said selection circuitry and operable to count a predetermined time period in response to said output clock signal; and

characterised in that said selection circuitry includes a plurality of latch circuits each having a set input (30, 34, 38, 42) and a reset input, each set input being responsive to one of a plurality of combinations of said input strobe signals and each reset input being responsive to a reset signal (18).

2. The apparatus of Claim 1, wherein each of said input strobe signals has an associated frequency and phase and wherein said associated frequency of each of said input strobe signals is equal to a base frequency and wherein said associated phase of each of said input strobe signals is an offset from a base phase.

3. The apparatus of Claim 1 or Claim 2, wherein only one of said plurality of combinations of said input strobe signals is asserted at any one time.

4. The apparatus of any preceding claim, wherein said reset signal is asserted and wherein each of said latch circuits is operable to generate a latch output signal and to inhibit said other of said latch circuits from being set in response to said one of said combinations of said input strobe signals being asserted and said reset signal being de-asserted.

5. The apparatus of any preceding claim wherein said selection circuitry further includes circuitry (52, 54, 56, 58) for combining said latch output signal with one of said input strobe signals to generate said output clock signal.

6. The apparatus of Claim 5, wherein said combining circuitry is further operable to combine said latch output signal with one of said input strobe signals which is not near one of its transition times.

7. A method of implementing a timer in an apparatus as claimed in Claim 1, which method comprising:

generating a plurality of input strobe signals each having an associated frequency equal to a base clock frequency and an associated phase equal to a base clock phase plus an associated offset;

combining selected ones of a plurality of input strobe signals (10;12;14;16) to generate a plurality of latch input signals;

associating each of said latch input signals with a set input of one of the latch circuits;

de-asserting a reset signal (118) at the reset input of said latch circuits to enable the latch circuits to be set;

combining a latch output signal associated with said one of said latch circuits with one of said input strobe signals to generate an output clock signal (62;64), said latch output signal being generated by each of a plurality of latch circuits (90;92;94;96) having an associated set input (30;34;38;42) and a reset input; and associating said output clock signal with an input of a counter (110), said counter being held reset by the reset signal and operable to count with said output clock signal in response to said de-asserting step.

8. The method of Claim 7, wherein said step of combining selected ones of the input strobe signals includes combining selected ones of the input strobe signals so that only said one of said latch input signals is high at any one time.

9. The method of Claim 8, wherein said step of combining the latch output includes combining the latch output associated with said one of the latch circuits with said one of the input strobe signals which is not near one of its transition times.

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10. The method of Claim 9, wherein said step of combining the latch output includes combining the latch output associated with said one of the latch circuits with said one of the input strobe signals (78) which is halfway through its high period.

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11. The method of Claim 9, wherein said step of combining the latch output includes combining the latch output associated with said one of the latch circuits with said one of the input strobe signals (76) which is halfway through its low period.

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Patentansprüche

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1. Vorrichtung für die Implementierung eines Taktgebers, die umfaßt:

eine Auswahlhaltungsanordnung (7, 9), die eine Auswahl aus mehreren Eingangs-Strobe-Signalen (10, 12, 14, 16) trifft, um ein Ausgangstaktsignal (62, 64) zu erzeugen;

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einen Zähler (110), der mit der Auswahlhaltungsanordnung verbunden und so betreibbar ist, daß er als Antwort auf das Ausgangstaktsignal eine vorgegebene Zeitperiode zählt; und

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dadurch gekennzeichnet, daß die Auswahlhaltungsanordnung mehrere Zwischenspeicherschaltungen enthält, die jeweils einen Setzeingang (30, 34, 38, 42) und einen Rücksetzeingang besitzen, wobei jeder Setzeingang auf eine von mehreren Kombinationen aus Eingangs-Strobe-Signalen anspricht und jeder Rücksetzeingang auf ein Rücksetzsignal (18) anspricht.

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2. Vorrichtung nach Anspruch 1, bei der jedem der Eingangs-Strobe-Signale eine Frequenz und eine Phase zugeordnet ist, die zugeordnete Frequenz jedes der Eingangs-Strobe-Signale gleich einer Grundfrequenz ist und die zugeordnete Phase jedes der Eingangs-Strobe-Signale eine Verschiebung gegenüber einer Grundphase ist.

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3. Vorrichtung nach Anspruch 1 oder Anspruch 2, bei der nur eine der mehreren Kombinationen aus Eingangs-Strobe-Signalen zu irgendeinem Zeitpunkt positiv ist.

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4. Vorrichtung nach einem vorhergehenden Anspruch, bei der das Rücksetzsignal positiv ist und

jede der Zwischenspeicherschaltungen so betreibbar ist, daß sie ein Zwischenspeicherausgangssignal erzeugt und als Antwort auf die Tatsache, daß die eine der Kombinationen der Eingangs-Strobe-Signale positiv ist und das Rücksetzsignal nicht positiv ist, verhindert, daß die andere der Zwischenspeicherschaltungen gesetzt wird.

5. Vorrichtung nach einem vorhergehenden Anspruch, bei der die Auswahlhaltungsanordnung ferner eine Schaltungsanordnung (52, 54, 56, 58) enthält, die das Zwischenspeicherausgangssignal mit einem der Eingangs-Strobe-Signale kombiniert, um das Ausgangstaktsignal zu erzeugen.

6. Vorrichtung nach Anspruch 5, bei der die Kombinationsschaltungsanordnung ferner so betreibbar ist, daß sie das Zwischenspeicherausgangssignal mit einem der Eingangs-Strobe-Signale, das sich nicht in der Nähe einer seiner Übergangszeiten befindet, kombiniert.

7. Verfahren für die Implementierung eines Zeitgebers in einer Vorrichtung nach Anspruch 1, bei dem

mehrere Eingangs-Strobe-Signale erzeugt werden, wovon jedem eine Frequenz, die gleich einer Grundtaktfrequenz ist, und eine Phase, die gleich einer Grundtaktphase zuzüglich einer zugeordneten Verschiebung ist, zugeordnet sind;

ausgewählte der mehreren Eingangs-Strobe-Signale (10; 12; 14; 16) kombiniert werden, um mehrere Zwischenspeichereingangssignale zu erzeugen;

jedes der Zwischenspeichereingangssignale einem Setzeingang einer der Zwischenspeicherschaltungen zugeordnet wird;

ein Rücksetzsignal (118) am Rücksetzeingang der Zwischenspeicherschaltungen nicht positiv angenommen wird, um ein Setzen der Zwischenspeicherschaltungen zu ermöglichen;

ein Zwischenspeicherausgangssignal, das einer der Zwischenspeicherschaltungen zugeordnet ist, mit einem der Eingangs-Strobe-Signale kombiniert wird, um ein Ausgangstaktsignal (62; 64) zu erzeugen, das durch jede von mehreren Zwischenspeicherschaltungen (90; 92; 94; 96), die einen zugeordneten Setzeingang (30; 34; 38; 42) und einen Rücksetzeingang besitzen, erzeugt wird; und

das Ausgangstaktsignal einem Eingang eines Zählers (110) zugeordnet wird, wobei der Zäh-

ler durch das Rücksetzsignal zurückgesetzt gehalten wird und so betreibbar ist, daß er als Antwort auf den Schritt der Annahme der Nichtpositivität mit dem Ausgangstaktsignal zählt.

8. Verfahren nach Anspruch 7, bei dem bei dem Schritt, bei dem ausgewählte der Eingangs-Strobe-Signale ausgewählt werden, ausgewählte der Eingangs-Strobe-Signale in der Weise kombiniert werden, daß nur eines der Zwischenspeichereingangssignale zu einem beliebigen Zeitpunkt einen H-Zustand aufweist.
9. Verfahren nach Anspruch 8, bei dem bei dem Schritt, bei dem die Zwischenspeicherausgangssignale kombiniert werden, das Zwischenspeicherausgangssignal, das der einen der Zwischenspeicherschaltungen zugeordnet ist, mit dem einen der Eingangs-Strobe-Signale, das sich nicht in der Nähe einer seiner Übergangszeiten befindet, kombiniert wird.
10. Verfahren nach Anspruch 9, bei dem bei dem Schritt, bei dem das Zwischenspeicherausgangssignal kombiniert wird, das Zwischenspeicherausgangssignal, das der einen der Zwischenspeicherschaltungen zugeordnet ist, mit dem einen der Eingangs-Strobe-Signale (78), das sich in der Mitte seines H-Zustands befindet, kombiniert wird.
11. Verfahren nach Anspruch 9, bei dem bei dem Schritt, bei dem das Zwischenspeicherausgangssignal kombiniert wird, das Zwischenspeicherausgangssignal, das der einen der Zwischenspeicherschaltungen zugeordnet ist, mit dem einen der Eingangs-Strobe-Signale (76), das sich in der Mitte seines L-Zustands befindet, kombiniert wird.

Revendications

1. Appareil pour implémenter un temporisateur comprenant

des circuits de sélection (7, 9) pour sélectionner dans une pluralité de signaux d'activation d'entrée (10, 12, 14, 16) pour générer un signal d'horloge de sortie (62, 64);
un compteur (110) couplé auxdits circuits de sélection et prévu pour compter une période de temps prédéterminée en réponse audit signal d'horloge de sortie ; et

caractérisé en ce que lesdits circuits de sélection incluent une pluralité de circuits à verrouillage chacun ayant une entrée de mise à un (30, 34, 38, 42) et une entrée de mise à zéro, chaque entrée de mise à un étant apte à répondre à une d'une plu-

ralité de combinaisons desdits signaux d'activation d'entrée et chaque entrée de mise à zéro étant apte à répondre à un signal de mise à zéro (18).

2. Appareil de la revendication 1, dans lequel chacun desdits signaux d'activation d'entrée a une fréquence et une phase associées et dans lequel ladite fréquence associée de chacun desdits signaux d'activation d'entrée est égale à une fréquence de base et dans lequel ladite phase associée de chacun desdits signaux d'activation d'entrée est un décalage par rapport à une phase de base.
3. Appareil de la revendication 1 ou de la revendication 2, dans lequel seule une de ladite pluralité de combinaisons desdits signaux d'activation d'entrée est activée à un moment quelconque.
4. Appareil de l'une quelconque des revendications précédentes, dans lequel ledit signal de mise à zéro est activé et dans lequel chacun desdits circuits à verrouillage est prévu pour générer un signal de sortie à verrouillage et pour empêcher lesdits autres desdits circuits à verrouillage d'être mis à un en réponse à ladite une desdites combinaisons, desdits signaux d'activation d'entrée d'être activés et desdits signaux de mise à zéro d'être désactivés.
5. Appareil de l'une quelconque des revendications précédentes, dans lequel lesdits circuits de sélection incluent en outre des circuits (52, 54, 56, 58) pour combiner ledit signal de sortie à verrouillage avec un desdits signaux d'activation d'entrée pour générer ledit signal d'horloge de sortie.
6. Appareil de la revendication 5, dans lequel lesdits circuits de combinaison sont en outre prévus pour combiner ledit signal de sortie à verrouillage avec un desdits signaux d'activation d'entrée qui n'est pas proche d'un de ses temps de transition.
7. Procédé d'implémentation d'un temporisateur dans un appareil selon la revendication 1, lequel procédé comprenant

la génération d'une pluralité de signaux d'activation d'entrée ayant chacun une fréquence associée égale à une fréquence d'horloge de base et une phase associée égale à une phase d'horloge de base plus un décalage associé ;
la combinaison de signaux sélectionnés d'une pluralité de signaux d'activation d'entrée (10 ; 12 ; 14 ; 16) pour générer une pluralité de signaux d'entrée à verrouillage ;
d'association de chacun desdits signaux d'entrée à verrouillage avec une entrée mise à un d'un des circuits à verrouillage ;
la désactivation d'un signal de mise à zéro

(118) à l'entrée de mise à zéro desdits circuits à verrouillage pour permettre aux circuits à verrouillage d'être mis à un ;

la combinaison d'un signal de sortie de verrouillage associé avec un desdits circuits à verrouillage avec un desdits signaux d'activation d'entrée pour générer un signal d'horloge de sortie (62 ; 64), ledit signal de sortie à verrouillage étant généré par chacun d'une pluralité de circuits à verrouillage (90 ; 92 ; 94 ; 96) ayant une entrée de mise à un associée (30 ; 34 ; 38 ; 42) et une entrée de mise à zéro ; et l'association dudit signal d'horloge de sortie avec une entrée d'un compteur (110), ledit compteur étant maintenu mis à zéro par le signal de mise à zéro et prévu pour compter avec ledit signal d'horloge de sortie en réponse à ladite étape de désactivation.

8. Procédé de la revendication 7, dans lequel ladite étape de combinaison de signaux sélectionnés des signaux d'activation d'entrée inclut la combinaison de signaux sélectionnés des signaux d'activation d'entrée, de sorte que seulement ledit un desdits signaux d'entrée à verrouillage est haut à un moment quelconque.
9. Procédé de la revendication 8, dans lequel ladite étape de combinaison de la sortie à verrouillage inclut la combinaison de la sortie à verrouillage associée avec ledit un des circuits à verrouillage avec ledit un des signaux d'activation d'entrée qui n'est pas proche d'un de ses temps de transition.
10. Procédé de la revendication 9, dans lequel ladite étape de combinaison de la sortie à verrouillage inclut la combinaison de la sortie à verrouillage associée avec ledit un des circuits à verrouillage avec ledit un des signaux d'activation d'entrée (78) qui est à mi-distance à travers sa période haute.
11. Procédé de la revendication 9, dans lequel ladite étape de combinaison de la sortie à verrouillage inclut la combinaison de la sortie à verrouillage associée avec ledit un des circuits à verrouillage avec ledit un des signaux d'activation d'entrée (76) qui est à mi-distance à travers sa période basse.

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