(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 806 780 B1

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention of the grant of the patent:
02.08.2000 Bulletin 2000/31

(51) Int Cl.[7]: **H01C 1/034**, H01C 7/10

(21) Application number: **96400993.0**

(22) Date of filing: **09.05.1996**

(54) **Zinc phosphate coating for varistor and method**

Zink-Phosphatbeschichtung für Varistor und Verfahren zur Herstellung

Revêtement en phosphate de zinc pour varistor et méthode de fabrication

(84) Designated Contracting States:
AT BE NL

(43) Date of publication of application:
12.11.1997 Bulletin 1997/46

(73) Proprietor: **Littlefuse, Inc.**
Des Plaines, IL 60016 (US)

(72) Inventor: **Ravindranathan, Palaniappan**
75116 Paris (FR)

(74) Representative: **Ballot, Paul Denis Jacques et al**
Cabinet Ballot-Schmit,
7, rue Le Sueur
75116 Paris (FR)

(56) References cited:
EP-A- 0 716 429
GB-A- 2 044 531
GB-A- 2 100 246
US-A- 5 115 221

- **PATENT ABSTRACTS OF JAPAN vol. 016, no. 303 (E-1228), 3 July 1992 & JP 04 083302 A (TOSHIBA CORP), 17 March 1992,**
- **PATENT ABSTRACTS OF JAPAN vol. 015, no. 343 (E-1106), 30 August 1991 & JP 03 131004 A (TOSHIBA CORP), 4 June 1991,**
- **PATENT ABSTRACTS OF JAPAN vol. 014, no. 016 (E-872), 12 January 1989 & JP 01 259506 A (ROHM CO LTD), 17 October 1989,**
- **PATENT ABSTRACTS OF JAPAN vol. 017, no. 514 (E-1433), 16 September 1993 & JP 05 136012 A (ROHM CO LTD), 1 June 1993,**

Note: Within nine months from the publication of the mention of the grant of the European patent, any person may give notice to the European Patent Office of opposition to the European patent granted. Notice of opposition shall be filed in a written reasoned statement. It shall not be deemed to have been filed until the opposition fee has been paid. (Art. 99(1) European Patent Convention).

EP 0 806 780 B1

Description

[0001] The present invention relates to nonlinear resistive devices, such as varistors, and more particularly to methods of making such devices using barrel plating techniques in which only the electrically contactable end terminals of the device are plated.

[0002] Nonlinear resistive devices are disclosed in the specifications of U.S. Patent No. 5,115,221.

[0003] Figure 1 is a typical device 10 that includes plural layers 12 of semiconductor material with electrically conductive electrodes 14 between adjacent layers. A portion of each electrode 14 is exposed in a terminal region 16 so that electrical contact may be made therewith. The electrodes 14 may be exposed at one or both of opposing terminal regions, and typically the electrodes are exposed at alternating terminal regions 16 as illustrated. The exposed portions of the electrodes 14 are contacted by electrically conductive end terminals 18 that cover the terminal regions 16.

[0004] The apparently simple structure of such devices belies their manufacturing complexity. For example, the attachment of the end terminals 18 has proved to be a problem in search of a solution. The terminal regions may be plated with nickel and tin-lead metals to increase solderability and decrease solder leaching. One method of affixing the end terminals 18 is to use a conventional barrel plating method in which the entire device is immersed in a plating solution. However, the stacked layers are semiconductor material, such as zinc oxide, that may be conductive during the plating process so that the plating adheres to the entire surface of the device. Thus, in order to provide separate end terminals as shown in Figure 1, a portion of the plating must be removed after immersion, or covered before immersion with a temporary plating resist comprised of an organic substance insoluble to the plating solution. However, the removal of the plating or organic plating resist is an extra step in the manufacturing process, and may involve the use of toxic materials that further complicate the manufacturing process.

[0005] It has also been suggested that the metal forming the end terminals 18 be flame sprayed onto the device, with the other portions of the surface of the device being masked. Flame spraying is not suitable for many manufacturing processes because it is slow and includes the creation of a special mask, with the additional steps attendant therewith, as disclosed in the specification of U.S. Patent No. 4,316,171.

[0006] An object of the present invention is to provide a method and device that obviates the problems of the prior art, and in which an electrically insulating, inorganic layer is formed on portions of the device before the device is barrel plated.

[0007] Another object is to provide a method and device in which a phosphoric acid is reacted with the exposed surface of stacked zinc oxide semiconductor layers to form a zinc phosphate coating, and in which a zinc phosphate coating protects portions of the device that are not to be plated when the end terminals are formed.

[0008] A further object is to provide a method and nonlinear resistive device having a body of layers of semiconductor material with an electrode between adjacent layers, in which the body of the nonlinear resistive device is coated with an inorganic layer that is electrically insulating, except at a terminal region of the body where an electrode is exposed for connection to an end terminal, and in which the coated body is plated with an electrically conductive metal to form the end terminal in a process in which the body becomes electrically conductive and in which the electrically conductive metal does not plate the coated portions of the body because the inorganic layer is not electrically conductive.

[0009] The invention is defined in claims 1 and 6.

[0010] The invention will now be described, by way of example, with reference to the accompanying drawings in which:

[0011] Figure 1 is a pictorial depiction of a varistor typical of the prior art.

[0012] Figure 2 is vertical cross section of an embodiment of the device of the present invention.

[0013] Figure 3 is a pictorial depiction of a high energy disc varistor with an insulating layer of the present invention thereon.

[0014] Figure 4 is a pictorial depiction of a surface mount device with an insulating layer of the present invention.

[0015] Figure 2 illustrates an embodiment of a nonlinear resistive element 20 that includes a body 22 having stacked zinc oxide semiconductor layers 24 with planar electrodes 26 between adjacent pairs of layers 24. Each electrode 26 has a contactable portion 28 that is exposed for electrical connection to electrically conductive metal (preferably silver, silver-platinum, or silver-palladium) end terminations 30 that cover terminal regions 32 of the body 22 and contact the electrodes 26. The portions of body 22 not covered with the end terminations 30 are coated with an electrically insulative zinc phosphate layer 34. The end terminations 30 may be plated with layers 36 of electrically conductive metal that form electrically contactable end portions for the resistive element 20. By way of example, in one embodiment the zinc oxide layers 24 may have the following composition in mole percent: 94-98% zinc oxide and 2-6% of one or more of the following additives; bismuth oxide, cobalt oxide, manganese oxide, nickel oxide, antimony oxide, boric oxide, chromium oxide, silicon oxide, aluminum nitrate, and other equivalents.

[0016] The body 22 and end terminations 30 are provided conventionally. The zinc phosphate layer 34 may be formed by reacting phosphoric acid with the zinc oxide semiconductor layers exposed at the exterior of the body 22. The reaction may take place for 25-35 minutes at 70° to 80°C. By way of example, one part orthophosphoric acid (85 wt%) may be added to fifty parts deionized water. The solution may be heated to 75°C and

stirred. The body 22 with end terminations 30 affixed may be washed with acetone and dried at 100°C for ten minutes. The washed device may be submerged in the phosphoric acid solution at 75°C for thirty minutes to provide the layer 34. After the layer 34 is applied, the body may be cleaned with hot, deionized water and dried at about 100°C for about fifteen minutes. The layer 34 does not adhere to the end terminations 30 because the silver or silver-platinum in the end terminations 30 is not affected by the phosphoric acid. The phosphoric acid solution may also be applied by spraying, instead of submerging, the washed device.

[0017] After the zinc phosphate layer 34 has been applied, the device may be barrel plated with an electrically conductive metal, such as nickel and tin-lead, to provide the layers 36. A conventional barrel plating process may be used, although the pH of the plating solution is desirably kept between about 4.0 and 6.0. In the barrel plating process the device is made electrically conductive and the plating material adheres to the electrically charged portions of the device. The metal plating of layers 36 does not plate the zinc phosphate layer 34 during the barrel plating because the zinc phosphate is not electrically conductive.

[0018] The zinc phosphate layer 34 is electrically insulating and may be retained in the final product to provide additional protection. The layer 34 does not effect the I-V characteristics of the device.

[0019] In an alternative embodiment, instead of zinc oxide, the semiconductor may be iron oxide, a ferrite.

[0020] In another alternative embodiment, the method described above may be used in the manufacture of other types of electronic devices. For example, a high energy disc varistor has a glass or polymer insulating layer on its sides. With reference to Figure 3, instead of glass or polymer, the disc varistor 40 may have an insulating layer 42 of phosphate formed in the manner discussed above. The present invention is applicable to other varistor products such as a surface mount device depicted in Figure 4, radial parts, arrays, connector pins, discoidal construction, etc.

Claims

1. A method of making a nonlinear resistive device (20) comprising the steps of :

(a) providing a body (22) for the nonlinear resistive device (20), the exterior of the body being a zinc oxide semiconductor (24) except at a terminal region (32) where an end termination (30) is provided ;
(b) reacting a phosphoric acid with the body (20) to form an electrically insulative zinc phosphate coating (34) on the exposed zinc oxide semiconductor, the end termination (32) not being coated with the zinc phosphate ; and
(c) barrel plating the body (22) to plate the end termination (30) with an electrically conductive metal (36),

wherein the electrically conductive metal (36) does not form on the zinc phosphate coated portions of the body during the barrel plating because the zinc phosphate is not electrically conductive.

2. A method as claimed in claim 1 wherein the end termination (30) comprises a layer of a metal selected from the group consisting of silver, silver-platinum, and silver-palladium.

3. A method as claimed in claim 1 or 2 wherein the body (22) comprises in mole percent, 94-98 % zinc oxide and 2-6 % of one or more of the additives selected from the group of additives consisting of bismuth oxide, cobalt oxide, manganese oxide, nickel oxide, antimony oxide, boric oxide, chromium oxide, silicon oxide, and aluminum nitrate.

4. A method as claimed in any one of claims 1 to 3 wherein the step of reacting phosphoric acid comprises the step of submerging the body (22) in the phosphoric acid, with the step of submerging the body comprising the step of submerging the body in a orthophosphoric acid solution for 25 to 35 minutes at 70° to 80°C.

5. A method as claimed in any one of claims 1 to 4 wherein the electrically conductive metal (36) comprises at least one of nickel and tin-lead, and the body (22) is a varistor.

6. A method of providing a semiconductor device including an inorganic electrically insulative layer, the semiconductor device having an exposed semiconductor surface (24) and electrically conductive metal end terminations (28), the method comprising the steps of :

(a) exposing the semiconductor device to a phosphoric acid solution to form a phosphate coating on the exposed semiconductor surfaces, and not on the end terminations (30) ; and
(b) barrel plating the semiconductor device with an electrically conductive metal plating in a process in which the device is electrically charged and submerged in a plating solution, the plating being formed on the end terminations (30) and not on the phosphate coating because the phosphate coating is not electrically conductive.

7. A method as claimed in claim 6 wherein the exposed semiconductor surfaces comprise one of zinc oxide and iron oxide.

8. A method as claimed in claims 6 or 7 wherein the phosphoric acid solution comprises orthophosphoric acid and deionized water.

9. A method as claimed in any claims 6 to 8 wherein the uncoated semiconductor device is submerged in a phosphoric acid solution for 25 to 35 minutes at 70°C to 80°C to form an electrically insulative zinc phosphate coating on the exposed surface of the zinc oxide layers (24), the end terminations (30) not being coated with the zinc phosphate coating.

Patentansprüche

1. Verfahren zum Herstellen eines nichtlinearen Widerstandsbauteils (20), das folgende Schritte aufweist:

   a) Vorsehen eines Körpers (22) für das nichtlineare Widerstandsbauteil (20), wobei das Äußere des Körpers ein Zinkoxid-Halbleiter (24) ausgenommen an einer Anschlußregion (32) ist, an der ein Kontaktanschluß (30) vorgesehen ist;
   b) Durchführen einer Reaktion von Phosphorsäure mit dem Körper (20), um einen elektrisch isolierenden Zinkphosphat-Überzug (34) auf dem freigelegten Zinkoxid-Halbleiter zu bilden, wobei der Kontaktanschluß (30) nicht mit dem Zinkphosphat beschichtet wird; und
   c) Durchführen eines Trommelplattierens des Körpers (22), um auf den Anschluß (30) ein elektrisch leitfähiges Metall (36) abzuscheiden, wobei das elektrisch leitfähige Metall (36) während des Trommelplattierens nicht die mit Zinkphosphat beschichteten Abschnitte des Körpers beschichtet, weil das Zinkphosphat nicht elektrisch leitfähig ist.

2. Verfahren nach Anspruch 1, bei dem der Kontaktanschluß (30) eine Schicht eines Metalls aufweist, das aus der Gruppe Silber, Silber-Platin und Silber-Palladium ausgewählt ist.

3. Verfahren nach Anspruch 1 oder 2, bei dem der Körper (22) 94 bis 98 Mol% Zinkoxid und 2 bis 6 Mol% von einem oder mehreren Zusätzen aufweist, die aus der Gruppe der Zusätze Wismutoxid, Kobaltoxid, Manganoxid, Nickeloxid, Antimonoxid, Boroxid, Chromoxid, Siliziumoxid und Aluminiumnitrat ausgewählt sind

4. Verfahren nach einem der Ansprüche 1 bis 3, bei dem der Schritt des Durchführens einer Reaktion von Phosphorsäure den Schritt des Tauchens des Körpers (22) in die Phosphorsäure aufweist, wobei der Schritt des Tauchens des Körpers das Tauchen in eine Ortho-Phosphorsäurelösung für 25 bis 35 Minuten bei 70 bis 80° C umfaßt.

5. Verfahren nach einem der Ansprüche 1 bis 4, bei dem das elektrisch leitfähige Metall (36) mindestens einen der Stoffe Nickel und Zinn-Blei umfaßt und der Körper (22) ein Varistor ist.

6. Verfahren zum Vorsehen eines Halbleiterbauteils mit einer anorganischen elektrisch isolierenden Schicht, wobei das Halbleiterbauteil eine freigelegte Halbleiteroberfläche (24) und elektrisch leitfähige Metallkontaktanschlüsse (28) aufweist, wobei das Verfahren die Schritte umfaßt:

   a) Exponieren des Halbleiterbauteils einer Phosphorsäurelösung, um eine Phosphatbeschichtung auf den ausgesetzten Halbleiteroberflächen, aber nicht auf den Kontaktanschlüssen (30) zu bilden; und
   b) Trommelplattieren des Halbleiterbauteils mit einem elektrisch leitfähigen Metall, das'in einem Prozeß abgeschieden wird, mittels dem das Bauteil elektrisch geladen und in eine Galvanisierlösung getaucht ist, wobei die Plattierung auf den Kontaktanschlüssen (30) und nicht auf der Phosphatbeschichtung gebildet wird, weil die Phosphatbeschichtung nicht elektrisch leitfähig ist.

7. Verfahren nach Anspruch 6, bei dem die exponierten Halbleiteroberflächen entweder Zinkoxid oder Eisenoxid aufweisen.

8. Verfahren nach Anspruch 6 oder 7, bei dem die Phosphorsäurelösung Ortho-Phosphorsäure und deionisiertes Wasser umfaßt.

9. Verfahren nach einem der Ansprüche 6 bis 8, bei dem das nicht beschichtete Halbleiterbauteil in eine Phosphorsäurelösung für 25 bis 35 Minuten bei 70 bis 80° C getaucht wird, um eine elektrisch isolierende Zinkphosphatschicht auf der exponierten Oberfläche der Zinkoxidschichten (24) zu bilden, wobei die Kontaktanschlüsse (30) nicht mit der Zinkphosphatschicht überzogen werden.

Revendications

1. Procédé de fabrication d'un dispositif à résistance non linéaire (20) comprenant les étapes consistant à :

   (a) fournir un corps (22) destiné au dispositif a résistance non linéaire (20), l'extérieur du corps étant un semi-conducteur d'oxyde de zinc (24), sauf au niveau d'une zone d'extrémité (32) où

une terminaison d'extrémité (30) est prévue ;
(b) faire réagir un acide phosphorique avec le corps (20) pour former un dépôt de phosphate de zinc, électriquement isolant (34), sur le semi-conducteur d'oxyde de zinc exposé, la terminaison d'extrémité (32) n'étant pas revêtue du phosphate de zinc ; et
(c) métalliser au tambour le corps (22) pour métalliser la terminaison d'extrémité (30) avec un métal conducteur électriquement (36),

dans lequel le métal électriquement conducteur (36) ne se forme pas sur les parties du corps recouvertes de phosphate de zinc pendant la métallisation au tambour parce que le phosphate de zinc n'est pas électriquement conducteur.

2. Procédé selon la revendication 1 dans lequel la terminaison d'extrémité (30) comprend une couche d'un métal sélectionné dans le groupe constitué d'argent, d'argent-platine, et d'argent-palladium.

3. Procédé selon la revendication 1 ou 2, dans lequel le corps (22) comprend en pourcentage molaire, 94 à 98 % d'oxyde de zinc et 2 à 6 % de l'un ou de plusieurs des additifs sélectionnés dans le groupe d'additifs constitué d'oxyde de bismuth, d'oxyde de cobalt, d'oxyde de manganèse, d'oxyde de nickel, d'oxyde d'antimoine, d'oxyde borique, d'oxyde de chrome, d'oxyde de silicium et de nitrate d'aluminium.

4. Procédé selon l'une quelconque des revendications 1 à 3 dans lequel l'étape consistant à faire réagir de l'acide phosphorique comprend l'étape consistant à immerger le corps (22) dans l'acide phosphorique, l'étape d'immersion du corps comprenant l'étape consistant à immerger le corps dans une solution d'acide orthophosphorique pendant 25 à 35 minutes à une température de 70° à 80° C.

5. Procédé selon l'une quelconque des revendications 1 à 4 dans lequel le métal électriquement conducteur (36) comprend au moins l'un des métaux nickel et étain-plomb et dans lequel le corps (22) est un varistor.

6. Procédé consistant à fournir un dispositif à semi-conducteur comprenant une couche inorganique isolante électriquement, le dispositif à semi-conducteur comportant une surface semi-conductrice exposée (24) et des terminaisons d'extrémité métalliques conductrices électriquement (28), le procédé comprenant les étapes consistant à :

(a) exposer le dispositif à semi-conducteur à une solution d'acide phosphorique pour former un dépôt de phosphate sur les surfaces semi-conductrices exposées et non sur les terminaisons d'extrémité (30) ; et
(b) métalliser au tambour le dispositif à semi-conducteur avec un placage métallique électriquement conducteur selon un processus dans lequel le dispositif est chargé électriquement et immergé dans une solution de métallisation, le placage étant formé sur les terminaisons d'extrémité (30) et non sur le dépôt de phosphate parce que le dépôt de phosphate n'est pas conducteur électriquement.

7. Procédé selon la revendication 6 dans lequel les surfaces semi-conductrices exposées comprennent, soit de l'oxyde de zinc, soit de l'oxyde de fer.

8. Procédé selon les revendications 6 ou 7 dans lequel la solution d'acide phosphorique comprend de l'acide orthophosphorique et de l'eau désionisée.

9. Procédé selon l'une quelconque des revendications 6 à 8 dans lequel le dispositif à semi-conducteur non recouvert est immergé dans une solution d'acide phosphorique pendant 25 à 35 minutes, à une température comprise entre 70° C et 80° C pour former un dépôt de phosphate de zinc, électriquement isolant, sur la surface exposée des couches d'oxyde de zinc (24), les terminaisons d'extrémité (30) n'étant pas recouvertes du dépôt de phosphate de zinc.

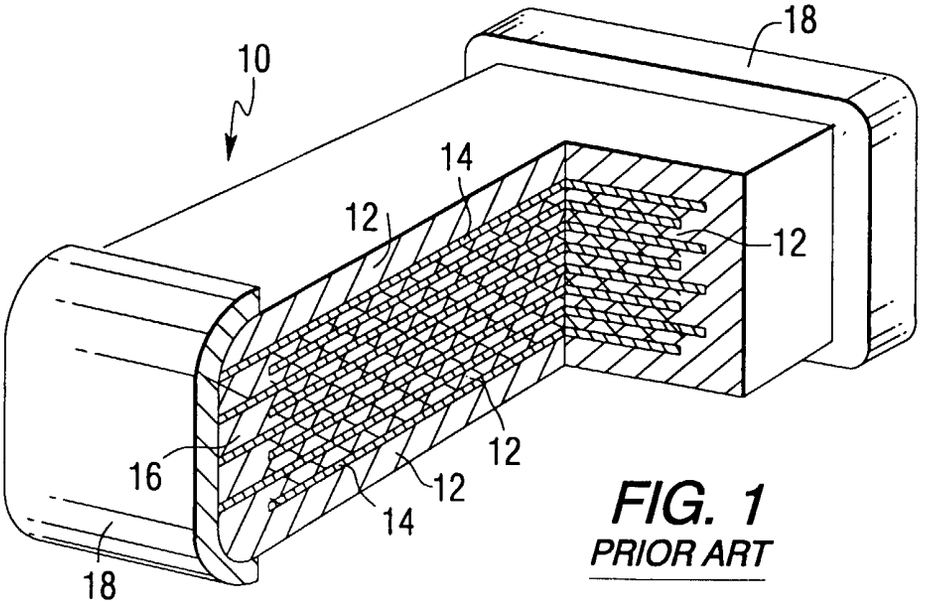

FIG. 1
PRIOR ART

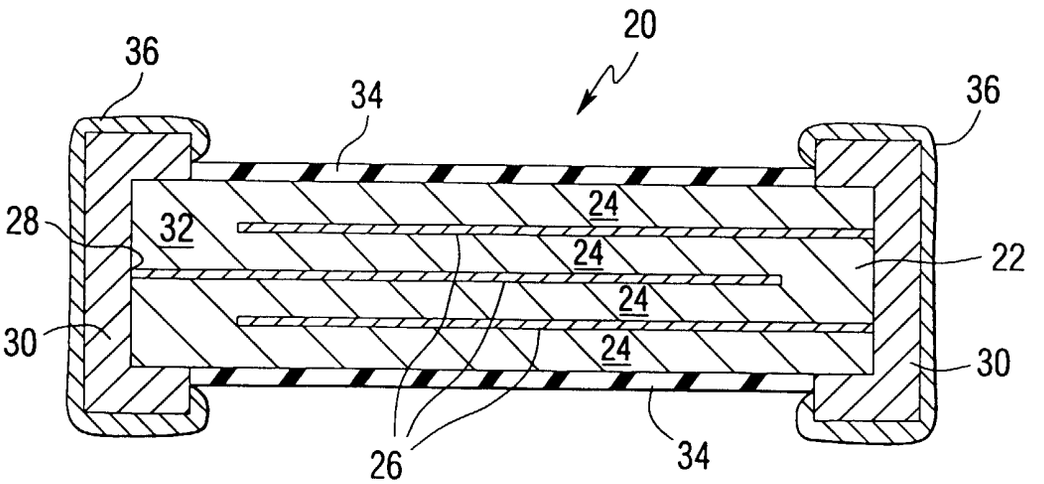

FIG. 2

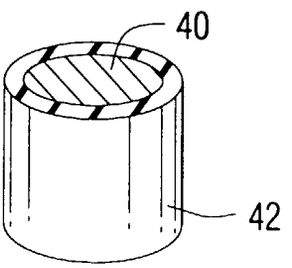

FIG. 3

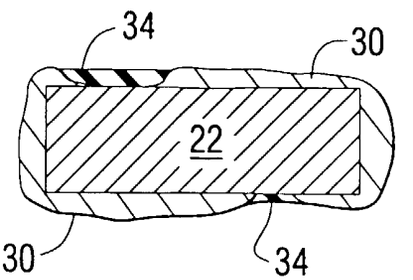

FIG. 4