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(54) **GATED FILAMENT STRUCTURES FOR A FIELD EMISSION DISPLAY**

GATE-FASERSTRUKTUREN FÜR EINE FELDEMISSIONSANZEIGEVORRICHTUNG

STRUCTURES A FILAMENTS COMPORTANT DES GRILLES POUR DISPOSITIF D'AFFICHAGE PAR EMISSION DE CHAMP

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## Description

### BACKGROUND OF THE INVENTION

Field of Use

**[0001]** This invention relates to a method of creating a gated filament structures for a field emission display with filaments positioned in apertures. The relative position of the majority of each filament tip to its associated aperture is substantially the same for a majority of the filament tips of the display. This relationship is maintained even for large displays where there are nonuniformities in the thickness of the insulating layer or in the plating of the filaments.

Description of the Related Art:

**[0002]** Field emission displays include a faceplate, a backplate and connecting walls around the periphery of the faceplate and backplate, forming a sealed vacuum envelope. In some field emission displays, the envelope is held at vacuum pressure, which can be about $1 \times 10^{-7}$ torr or less. The interior surface of the faceplate is coated with light emissive elements, such as phosphor or phosphor patterns, which define an active region of the display. Field emission cathodes, such as cones and filaments, are located adjacent to the backplate. Application of an appropriate voltage at the extraction electrode releases electrons which are accelerated toward the phosphors on the faceplate. The accelerated electrons strike their targeted phosphors, causing the phosphors to emit light seen by the viewer at the exterior of the faceplate. Emitted electrons for each of the sets of emitters are intended to strike only certain targeted phosphors.

**[0003]** A variety of methods for forming field emitters are known.

**[0004]** U.S. Patent No. 3,655,241 discloses fabricating field emitters using a screen with arrays of circular or square openings that is placed above a substrate electrode. A deposition is performed simultaneously from two sources. One of the sources consists of an emitter-forming metal, such as molybdenum, and atoms are deposited in a direction perpendicular to the substrate electrode. The other source consists of a closure material, such as a molybdenum-alumina composite. Atoms of the closure material are caused to impinge on the screen at a small angle to the substrate. The closure material progressively closes the openings in the screen. Thus the emitter-forming metal is deposited in the shape of cones or pyramids, depending on whether the screen openings are circular or square.

**[0005]** Another method of creating field emitters is disclosed in U.S. Patent No. 5,164,632. Part of an aluminum plate is anodically oxidized to create a thin alumina layer having pores that extend nearly all the way through the alumina. An electrolytic technique is used to fill the pores with gold for the field emitters. An address line is formed over the filled pores along the alumina side of the structure, after which the remaining aluminum and part of the adjoining alumina are removed along the opposite side of the structure to re-expose the gold in the pores. Part of the re-exposed gold is removed during an ion-milling process utilized to sharpen the field emitters. Gold is then evaporatively deposited onto the alumina and partly into the pores to form the gate electrode.

**[0006]** Field emitters are fabricated in U.S. Patent No. 5,150,192 by creating openings partway through a substrate by etching through a mask formed on the bottom of the substrate. Metal is deposited along the walls of the openings and along the lower substrate surface. A portion of the thickness of the substrate is removed along the upper surface. A gate electrode is then formed by a deposition/planarization procedure. Cavities are provided along the upper substrate surface after which the hollow metal portions in the openings are sharpened to complete the field emitter structures.

**[0007]** However, large area field emission displays require a relatively strong substrate for supporting the field emitters extending across the large emitter area. The requisite substrate thickness is typically several hundred microns to 10 mm or more.

**[0008]** The fabrication methods in U.S. Patents 5,164,632 and 5,150,192 make it very difficult to attach the field emitters to the substrates of thickness required for large area displays.

**[0009]** In U.S. Patent No. 4,940,916, a gated area field emitter consists of cones formed on a highly resistive layer that overlies a highly conductive layer situated on an electrically insulating supporting structure. For a thickness of 0.1 to 1 microns, the highly resistive layer has a resistivity of $10^4$ to $10^5$ ohm-cm. The resistive layer limits the currents through the electron-emissive cones so as to protect the field emitter from breakdown and short circuits.

**[0010]** It is desirable to have uniformity of emission from the cathodes. A field emission cathode relies on there being a very strong electric field at the surface of a filament or generally on the surface of the cathode. Creation of the strong field is dependent on, (i) the sharpness of the cathode tip and (ii) the proximity of the extraction electrode (gate) and the cathode. Application of the voltage between these two electrodes produces the strong electric field. Emission nonuniformity is related to the nonuniformity in the relative positions of the emitter tip and the gate. Emission nonuniformity can also result from differences in the sharpness of the emitting tips.

**[0011]** Busta, "Vacuum Microelectronics-1992," J. Micromech. Microeng., Vol. 2, 1992 pp. 43- 74 provides a general review of field-emission devices. Among other things, Busta discusses Utsumi, "Keynote Address, Vacuum Microelectronics: What's New and Exciting," IEEE Trans. Elect. Dev., Oct. 1990, pp. 2276-2283, who suggests that a filament with a rounded end is the best

shape for a field emitter. Also of interest is Fischer et al., "Production and Use of Nuclear Tracks: Imprinting Structure on Solids," Rev. Mod. Phys., Oct. 1983, pp. 907- 948, which deals with the use of charged-particle tracks in manufacturing field emitters according to a replica technique.

**[0012]** A well collimated source of evaporant, as taught in U.S. Patent No. 3,655,241, is necessary in order to obtain uniformity of cone or filament formation across the entire field emission display. In order to maintain a collimated source, the majority of evaporant is deposited on interior surfaces of the evaporation equipment. The combination of the expensive of the evaporation equipment, and the wastage of evaporant, is undesirable for commercial manufacturing and is compounded as the size of the display increases. With large displays, there are nonuniformities in the thickness of the insulating layer and the plating of the filaments.

**[0013]** It would be desirable to provide a gated filament structure for a field emission display where each filament and filament tip is positioned in a gate aperture. It would further be desirable to provide a large field emission display in which the relative positions of the filament tips to their associated apertures are substantially the same for a majority of the filament tips of the display. There is a need to maintain this relationship for large displays which have more nonuniformities in the thickness of the insulating layer and in the plating of the filaments.

**[0014]** Reference is made to WO94/28569, which describes a microtip display device and method of manufacture using heavy ion lithography. A microtip electron source and a cathodoluminescent anode are produced and then assembled. The source is manufactured by forming a stack of layers, forming holes therein and then forming microtips in said holes. In order to form the holes, latent traces randomly distributed in a superficial layer of the stack are formed by irradiating the layer with heavy ions. The traces are then exposed by etching until holes appear in said layer.

**[0015]** Reference is also made to DE-A-4209301 and DE-A-3340777.

## SUMMARY

**[0016]** In a first aspect, the invention provides a method of creating gated filament structures for a field emission display, comprising the consecutive or non-consecutive steps of:

providing a multi-layer structure including a substrate, an insulating layer positioned on the substrate and a metal gate layer positioned on at least a portion of a top surface of the insulating layer;

providing a plurality of apertures in the gate layer, each aperture extending through the gate layer from the top surface of the gate layer, characterised by:

forming a plurality of spacers adjacent to the edges of the apertures and extending into the apertures,

using the spacers as masks for etching the insulating layer so as to form a plurality of pores in the insulating layer; and

plating the plurality of pores in the insulating layer to form filaments.

**[0017]** In a second aspect, the invention provides a field emission display device comprising a gated filament structure formed using a method as aforesaid.

**[0018]** An advantage of the invention is that it can provide gated filament structures for large field emission displays.

**[0019]** A further advantage of the invention is that it can provide gated filament structures that are electroplated.

**[0020]** Another advantage of the invention is that it can provide a commercial manufacturing process for forming filaments in a large field emission display.

**[0021]** Yet another advantage of the invention is that it can provide a commercial manufacturing process for forming filaments in a large field emission display using electroplating.

**[0022]** Still a further advantage of the invention is that it can provide a method for forming filaments in a field emission display which uses spacers as an etch mask and as part of the mold for plating the filament structures.

**[0023]** In one preferred embodiment for creating gated filament structures in a field emission display, a multilayer structure is provided that includes a substrate, an insulating layer and a metal gate layer positioned on at least a portion of a top surface of the insulating layer. For purposes of definition, an insulating substrate is, (i) a conductive or semi-conductive substrate with an insulating layer on a top surface of the substrate, (ii) a conductive or semi-conductive substrate with patterned insulating regions on a top surface of the substrate or (iii) an insulating substrate. A plurality of patterned gates are provided and define a plurality of gate apertures on the top surface of the insulating layer. A plurality of spacers are formed in the gate apertures at edges of the patterned gates on the top surface of the insulating layer. The patterned gates can be part of the initial multi-layer structure, or formed thereafter. A plurality of spacers are formed in the gate apertures at edges of the patterned gates on the top surface of the insulating layer. The spacers are used as masks for etching the insulating layer and forming a plurality of pores in the insulating layer. The pores are plated with a filament material that extends form the pores, into the gate apertures, and creates a plurality of filaments. The spacers are then removed. Further, the multi-layer structure can include a conductivity layer on at least a portion of a top surface of the substrate.

**[0024]** In another preferred embodiment for creating

gated filament structures in a field emission display, a multi-layer structure is provided that includes a substrate, an insulating layer, a metal gate layer positioned on a top surface of the insulating layer and a gate encapsulation layer positioned on a top surface of the metal gate layer. A plurality of patterned gate are provided and define a plurality of gate apertures on the top of the insulating layer. A plurality of spacers are formed in the gate apertures at edges of the patterned gates on the top surface of the insulating layer. The spacers are used as masks for etching the insulating layer and forming a plurality of pores in the insulating layer. The pores are plated with a filament material to create a plurality of filaments.

**[0025]** The majority of filament tips can, (i) extend between the top and bottom metal gate layer surfaces, (ii) extend below the bottom metal gate layer surface, or (iii) extend above the top metal gate layer surface.

**[0026]** Each filament of the display can be electroplated.

**[0027]** In another embodiment, the gated filament structure for a field emission device includes a substrate.

**[0028]** Additionally, the majority of the filament tips can extend beyond the top metal gate layer planar surface, or below the bottom metal gate layer planar surface.

**[0029]** Further, each filament can be electroplated. Each filament is vertically self aligned in its associated aperture.

**[0030]** In one preferred form, the resulting gated filament structure for a field emission display includes a plurality of filaments. Included is a substrate, an insulating layer positioned adjacent to the substrate, and a metal gate layer including a plurality of gates positioned adjacent to the insulating layer. The metal gate layer has an average thickness "s" and a top metal layer planar surface that is substantially parallel to a bottom metal gate layer planar surface. A plurality of apertures extending through each gate formed in the metal gate layer. Each aperture has an average width "r" along a bottom planar surface of the aperture. Each aperture defines a midpoint plane positioned parallel to and equally distant from the top metal gate layer planar surface and the bottom metal gate layer planar surface. A plurality of gated filaments are individually positioned in an aperture. Each filament has a filament axis. The intersection of the filament axis and the midpoint plane defines a point "O". Each filament includes a filament tip terminating at a point "A". A majority of all filament tips of the display have a length "L" between each filament tip at point A and point O along the filament axis where,

$$L \leq (s + r)/2$$

**[0031]** It is preferred that at least 75% of all filament tips of the display have this relationship for points A and O, more preferably at least 90% of the filament tips have this relationship.

## DESCRIPTION OF THE DRAWINGS

**[0032]**

Figure 1 is a cross-sectional view of a multi layer structure with a gated filament in an insulating pore.

Figure 2 is a cross-sectional view of an initial multilayer structure used to create the gated filaments.

Figure 3 is a cross-sectional view of the structure of Figure 2, after the tracking resist layer has been etched to open up an aperture at the gate.

Figure 4 is a cross-sectional view of the structure of Figure 3 following reactive ion etching of the metal gate layer, and the creation of gates and apertures.

Figure 5(a) is a cross-sectional view of the structure of Figure 4 with a conformal layer applied over the gates and into the apertures.

Figure 5(b) is a cross-sectional view of the structure of Figure 5(a) when conforming layer 32 is anisotropicaly etched and material is removed. The anisotropic etching step removes the material, thus forming a spacer at a step.

Figure 6 is a cross-sectional view of the structure of Figure 5 following anisotropic etching of the conformal layer, leaving spacers in the apertures at their edges on the top surface of the insulating layer.

Figure 7 is a cross-sectional view of the structure of Figure 6 illustrating the use of the spacers as masks for reactive ion etching the insulating layer through the spacing over the insulating layer, to the resistive layer, and the formation of an insulating layer pore. The schematic of an electrochemical cell is also shown with an anode positioned over the gates, and the cathode connected to the metal row electrode and its associated resistive layer. The schematic also includes a voltage supply.

Figure 8 is a cross-sectional view of the structure of Figure 7 after the insulating layer pore has been filled with a filament material that extends through the insulating layer pore to a height generally not greater than the height of the spacers, creating the filament.

Figure 9 is a cross-sectional view of a gated filament structure with a sharpened tip that can extend into the gate.

Figure 10 is a second embodiment of the invention illustrating an initial multi-layer structure that includes a gate encapsulation layer positioned on a top surface of the metal gate layer and a tracking resist layer positioned on a top surface of the gate encapsulation layer.

Figure 11 is a cross-section view of the structure of Figure 10 after the tracking resist layer has been etched to open up an aperture at the gate encapsulation layer.

Figure 12 is a cross-sectional view of the structure of Figure 11 following reactive ion etching of the gate encapsulation layer and the metal gate layer, to create gates and apertures.

Figure 13 is a cross-sectional view of the structure of Figure 12 with a conformal layer applied on top of the gate and into the aperture.

Figure 14 is a cross-sectional view of Figure 13 following anisotropic etching of the conforming member, leaving spacer material in the apertures at their edges on the top surface of the insulating layer to form a plurality of spacers.

Figure 15 is a cross-sectional view of the structure of Figure 14 using the spacers as masks for etching the insulating layer through the spacing over the insulating layer to the resistive layer, and form an insulating layer pore. The schematic of an electrochemical cell is also shown with an anode positioned over the gates, and the cathode connected to the metal row electrode and its associated resistive layer. The schematic also includes a voltage supply.

Figure 16 is a cross-sectional view of the structure of Figure 15 after the insulating layer pore has been filled with a filament material which extends through the insulating layer pore to a height above the gate.

Figure 17 is a cross-sectional view of a structure, similar to that of Figure 16 except the thickness of the insulating layer is non-uniform. The relationship between the filament tip and the gate is still maintained even with the nonuniformity.

Figure 18 is a cross-sectional view of the structure of Figure 16. The relationship between the filament tip and the gate is still maintained even with nonuniformity of plating of the filaments.

Figure 19 is a cross-sectional view of a gated filament following removal of the gate encapsulation layer and the spacers. Also illustrated is a schematic of an electrochemical cell with the gate as the cathode, and the overgrown filament as the anode.

Figure 20 is a cross-sectional view of the structure of Figure 19 illustrating the creation of a gated sharpened filament.

Figure 21 is a cross-sectional view of the filament positioned in its aperture.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

**[0033]** For purposes of this disclosure, a large area field emission display is defined as having at least a 6 inch diagonal screen, more preferably at least an 8 inch diagonal screen, yet more preferably at least a 10 inch diagonal screen, and still more preferably at least a 12 inch diagonal screen.

**[0034]** The ratio of length to maximum diameter of a filament is at least 2, and normally at least 3. The length-to-maximum-diameter ratio is preferably 5 or more.

**[0035]** A gated filament structure 10 is created, as illustrated in Figure 1, from a multi-layer structure which includes a substrate 12, a metal row electrode 14, a resistive layer 16 on top of row electrode 14, an insulating layer 18 on a top surface of resistive layer 16, a metal gate layer 20, and a filament 22 in an insulating pore. Insulating layer 18 is positioned between substrate 12 and metal gate layer 20. It will be appreciated that insulating layer 18 is positioned adjacent to substrate 12 and there can be additional layers between insulating layer 18 and substrate 12 in this adjacent relationship. Thus, adjacent is used herein to mean one layer on top of another layer as well as the possibly of adjacent layers can have intervening layers between them. A portion of insulating layer 18 adjacent to filament 22 has been removed. Filaments are typically cylinders of circular transverse cross section. However, the transverse cross section can be somewhat non-circular. The insulating pore is formed with spacers and reactive ion etching. For definitional purposes, substrate means, (i) a conductive or semi-conductive substrate with an insulating layer on a top surface of the substrate, (ii) a conductive or semi-conductive substrate with patterned insulating regions or (iii) an insulating substrate.

**[0036]** Referring now to Figure 2, the initial multi-layer structure also includes a tracking resist layer 24 positioned on a top surface of metal gate 20.

**[0037]** Suitable materials for the multi-layer structure include the following:

substrate 12 - glass or ceramic
metal row electrode 14 - Ni
resistive layer 16 - cermet, $CrO_x$ or SiC
insulating layer 18 - $SiO_2$
metal gate layer 20 - Cr and/or Mo
tracking resist layer 24 - polycarbonate
filament 22 - Ni or Pt

**[0038]** Multi-layer structure of Figure 2 can be irradiated with energetic charged particles, such as ions, to produce charged particle tracks in tracking resist layer 24.

**[0039]** The other methods include but are not limited to conventional lithography, such as photolithography, x-ray lithography and electron beam lithography.

**[0040]** When charged particles are used, they impinge on tracking resist layer 24 in a direction that is substantially perpendicular to a flat lower surface of substrate 12, and therefore are generally perpendicular to tracking resist layer 24. The charged particles pass through tracking resist layer 24 in a straight path creating a continuous damage zone along the path. Particle tracks are randomly distributed across the multi-layer structure with a well defined average spacing. The track density can be as much as $10^{11}$ tracks/cm$^2$. A typical value is $10^8$ tracks/cm$^2$, which yields an average track spacing of 1 micron.

**[0041]** In one embodiment, a charged particle accel-

erator forms a well collimated beam of ions which are used to form tracks. The ion beam is scanned uniformly across tracking resist layer 24. A preferred charged particle species is ionized Xe with an energy typically in the range of about 4 MeV to 16 MeV. Alternatively, charged particle tracks can be created from a collimated source of nuclear fission particles produced, for example, by the radioactive element Californium 252.

**[0042]** Once the particle tracks have been formed, a chemical etch, including but not limited to KOH or NaOH, etches and can over-etch the track formed in tracking resist layer 24 (Figure 3). Instead of forming a cylindrical pore etched along the track, it is widened to open up an aperture 28 in tracking resist layer 24 that is conical with a generally trapezoidal cross-section. Aperture 28 has a diameter of about 50 to 1000 nm, such as by way of example 200 nm, at gate layer 20. Tracking resist layer 24 is used as a mask to etch gate layer 20 to produce, in one embodiment a 200 nm diameter gate hole 28 (Figure 4). The etching can be reactive ion etching such as $Cl_2$ for Cr and $SF_6$ for Mo. The depth of reactive ion etching into insulating layer 18 is minimized. A variety of mechanisms are available to ensure that the reactive ion etching stops at insulating layer 18 including but not limited to, monitoring the process and stopping it at the appropriate time, the use of feedback devices, such as sensors, and use of a selective etch. Excess tracking resist 24 material is stripped away, leaving a gate 30 on the top of insulating layer 18.

**[0043]** Referring now to Figure 5(a), a conformal layer 32 is applied on top of gates 30 and into apertures 28. Suitable materials for conformal layer 32 include but are not limited to silicon nitride, amorphous or small grained polycrystalline Si, and $SiO_2$. Methods for applying conformal layer include but are not limited to CVD.

**[0044]** As shown in Figure 5(b) when conforming layer 32 is anisotropicaly etched material is removed. Material is removed from conformal layer 32 at surfaces which are parallel to a plane 33 defined by insulating substrate 12, e g., surface 35 is not etched. The anisotropic etching step removes the material, thus forming a spacer 36 at a step 34.

**[0045]** It is seen in Figure 6 that spacer 36 leaves an aperture 38 at the top of insulating layer 18. The size of spacers 36 is controlled to define the size of aperture 38, which can be, in one instance about 100 nm in width.

**[0046]** As shown in Figure 7, spacers 36 are used as a mask for etching, e.g., a highly anisotropic selective etch in order to etch substantially only insulating layer 18 and form an insulating pore 40. Other structures are minimally etched. During the etch process, polymer is formed on the walls of insulating pores due to the use of $CH_4$ in the plasma. This forms a polymer on side and bottom walls of insulating pores 40. The polymer protects the walls from chemical attack but does not protect the walls from the energetic particles. Because the energetic particles come straight down and hit only the bottom of insulating pore 40, the polymer is removed only from the bottom of insulating pore 40 and not along the sidewalls. The walls are protected from chemical attack, and etching is only in a direction towards resistive layer 16 because of the anisotropic nature of the reactive ion etching. There is substantially no undercutting of insulating layer 18 because of polymer formation along the vertical walls of insulating pore 40 perpendicular to the plane of insulating substrate 12. Insulating pore 40 does not extend substantially into resistive layer 16. The control of limiting the etching of resistive layer 16 is accomplished with a variety of mechanisms, including but not limited to, (i) employing a selective etch that etches resistive layer 16 very slowly, (ii) determination of an end point when the etching will be completed by timing and the like, and (iii) monitoring to determine the point when resistive layer 16 begins to be etched.

**[0047]** Following reactive ion etching, it may be desirable to apply a chemical treatment on insulating pore 40 to remove the polymer. Suitable chemical treatments include but are not limited to, a plasma of $CF_4$ with $O_2$, or commercially available polymer strippers used in the semiconductor industry well known to those skilled in the art. Thereafter, an electrochemical cell is used, such as shown in Figure 7.

**[0048]** Referring now to Figure 8, insulating pore 40 is then filled with a filament material. The plating extends into patterned gate 30. Suitable plating materials include but are not limited to Ni, Pt and the like. Plating can be achieved by pulse plating, with resistance layer 16 as the cathode, and an external anode. The voltage of resistive layer 16 and patterned gate 30 is controlled so that plating does not occur on metal gate layer 20.

**[0049]** Spacers 36 are subsequently removed with a removal process, including but not limited to selective plasma etching and wet etching. Thereafter, insulating layer 18 adjacent to filament 22 can be removed with an isotropic plasma or wet chemical (dilute HF) etch. The amount of insulating layer 18 removed is almost down to resistive layer 16.

**[0050]** Alternatively, insulating layer 18 is not removed (Figure 9).

**[0051]** The use of spacers 36 along with reactive ion etching defines insulating pores 40 which are used to create filaments 22. An alternative process is to use tracking of the insulating layer 18 and chemical etching along the particle tracks.

**[0052]** With reference once again to Figure 1, filament 22 is created and its tip preferably is between a top planar surface 41 of gate layer 20, and a bottom planar surface 43 of gate layer 20. In another embodiment, the filament tip is formed above planer surface 41. Less preferably, filament tip is formed below planar surface 43. The tip of filament 22 can be polished/etched to form a desired tip geometry.

**[0053]** Filaments 22 can have a variety of geometries such as flat topped cylinders, rounded top cylinders, sharp cones and the like, which can be created by polishing/etching.

**[0054]** If there are nonuniformities in the thickness of insulating layer 18, or nonuniformities in plating, another embodiment of the invention, illustrated in Figures 10 through 21, may be more suitable for producing filaments 22 with the same position relative to each respective gate 30, as more fully described hereafter. With reference now to Figures 10 and 20, filament 22 is formed above patterned gate 30 by the inclusion of a gate encapsulation layer 42. As shown in Figure 20 patterned gate 30 is then used to define the point of filament 22, e.g., the tip geometry of filament 22, which allows for accommodation of non-uniformity in plating and nonuniformity in thickness of the dielectric. This defines the self-alignment of filament 22. Suitable gate encapsulation layer 42 materials include but are not limited to Si, $SiO_2$ and $Si_3N_4$.

**[0055]** The initial multi-layer structure is illustrated in Figure 10 and includes a substrate 12, a metal row electrode 14 positioned on a top surface of substrate 12, a resistive layer 16 on a top surface of metal row electrode 14, an insulating layer 18 on a top surface of resistive layer 16, a metal gate layer 20 positioned on a top surface of insulating layer 18, a gate encapsulation layer 42 positioned on a top surface of metal gate layer 20 and optionally a tracking resist layer 24 positioned on a top surface of gate encapsulation layer 42. It will be appreciated that tracking resist layer 24 need not be included in this embodiment. The appropriate choice of material for gate encapsulation layer 42 may permit gate encapsulation layer 42 to be used also as the tracking resist layer. The only differences between the multi-layer structure in the two embodiments is the inclusion of gate encapsulation layer 42, with or without tracking resist layer 24. Gate encapsulation layer 42 provides two functions, (i) it encapsulates patterned gate 30 and (ii) allows for the formation of taller spacers 36, permitting plating filament 22 above patterned gate 30.

**[0056]** Particle tracking is utilized, as practiced in the first embodiment, and tracking resist layer 24 is etched (Figure 11). A reactive ion etch through gate encapsulation layer 42 and gate layer 20 is performed (Figure 12), creating gate hole 28 and patterned gate 30. Tracking resist layer 24 need not be included if gate encapsulation layer 42 can be tracked, etched and used as a resist for patterning gate 30. It will be appreciated that the same methods employed in the embodiment illustrated in Figures 1 through 9 are employed in this second embodiment, illustrated in Figures 10 through 21. The detailed descriptions of the multiplicity of steps utilized will not be repeated here.

**[0057]** Tracking resist layer 24, if included, is removed and a spacer conformal layer 32 is formed over gate layer 20 and into gate hole 28 (Figure 13). With the proper selection of materials for gate encapsulation layer 42 and spacer conformal layer 32, gate layer 20 is completely insulated; therefore eliminating concerns regarding controlling voltage on patterned gate 30 to ensure that plating will not occur on patterned gate 30.

**[0058]** With the anisotropic etching of spacer conformal layer 32, the resulting spacers 36 have a height equal to the height of gate layer 20 plus encapsulation layer 42 (Figure 14).

**[0059]** Insulating pore 40 is formed (Figure 15) and can have a width in the range of 50 to 1000 nm. A suitable width is about 100 nm. Insulating pore 40 is then filled (Figure 16).

**[0060]** Referring now to Figures 17 and 18, the effects of nonuniformity of the thickness of insulating layer 18 of gated filament structure 10, and nonuniformity of plating are illustrated. Assuming that all insulating pores 40 fill at the same rate, then where insulating layer 18 is thin, insulating pores will be filled more quickly and there will be overplating (Figure 16). Due to plating nonuniformity some insulating pores 40 will fill faster than others (Figure 17). It is difficult to achieve uniformity of plating, particularly in large field emission displays because it is arduous to build suitable equipment to achieve uniform plating. The requirements of such equipment are that it provides, (i) uniform current density and (ii) efficiently stirs the electrolyte to avoid concentration gradients and depletion of the electrolyte. In any event, even with these nonuniformities, the relationship between filament 22 and its respective gate aperture 28 is maintained, as more fully described hereafter.

**[0061]** Conformal layer 32 and spacers 36 are removed, leaving a filament 22 that extends beyond patterned gate 30. (Figure 19). Patterned gate 30 can be used to electro-polish filament 22. Thus, patterned gate 30 is used to define the point where a tip 44 of filament 22 will be (Figure 20). Patterned gate 30 serves as the cathode for the electro-polishing. A suitable electrolyte is well known to those skilled in the art. This essentially pinches off filament 22 so that excess material becomes free and can be washed away. The remaining filament 22 has a tip 44 geometry that is sharp.

**[0062]** Tip 44 of filament 22 is now located at the position of patterned gate 30.

**[0063]** Filament 22 and filament tip 44 are positioned in gate aperture 28 to establish a relative position for filament tip 44 with its associated gate aperture 28. Referring now to Figure 21, the relative position of filament tip 44 to its associated gate aperture 28 is defined as the position of tip 44 relative to a top planar surface 41 of gate layer 20 and a bottom planar surface 43 of gate layer 20.

**[0064]** Metal gate layer 20 has an average thickness "s" and a top metal gate planar surface 20(a) that is substantially parallel to a bottom metal gate planar surface 20(b). Metal gate layer 20 includes a plurality of pores 40 extending through metal gate 30. Each pore 40 has an average width "r" along a bottom planar surface of the aperture. Each pore defines a midpoint plane 46 positioned parallel to and equally distant from top metal gate planar surface 20(a) and bottom metal gate planar surface 20(b). A plurality of filaments 22 each have a filament tip 44 which terminates at a point "A" and a fil-

ament axis 48 that extends along a length of the filament through filament tip 44. At the intersection of filament axis 48 and midpoint plane 46, a point "O" is defined. A majority of all filament tips 44 of the display have a length "L" between each filament tip 44 at point A and point O along filament axis 48, where,

$$L \leq (s+r)/2.$$

**[0065]** Preferably, at least 75% of all filament tips 44 have this relationship between point A and point O, more particularly, it is at least 90%.

**[0066]** The majority of filament tips 44 of the display can have, (i) point A above top metal gate layer planar surface 20(a), (ii) point A between top metal gate layer planar surface 20(a) and bottom metal gate layer planar surface 20(b), or (iii) point A below bottom metal gate layer planar surface 20(b).

**[0067]** With the method of the present invention every insulating pore 40 is overplated and vertical self-alignment is utilized. Patterned gate 30 is used to do the polishing/etching. With the inclusion of gate encapsulation layer 42 filament 22 is plated above patterned gate 30. Additionally, there may be more plating at the edges of the field emission display than in the middle. This can occur because of (i) current crowding effects and (ii) electrolytic depletion effects. As long as the plating is above patterned gate 30 in all places two advantages are achieved, (i) a tolerance on thickness uniformity of deposited insulating layer 18 is provided, and (ii) a high tolerance for the uniformity of plating is possible.

**[0068]** The result is the creation of filaments 22 for the field emission display and the position of each filament 22 is the same within each pore 40 (vertical alignment). Polished filament tips 44 can be created. Further, cones can be formed, as well as filaments using electroless deposition and selective deposition processes well known to those skilled in the art.

**[0069]** In another embodiment, the gate can be patterned and used as a mask to completely etch the insulating layer. The conformal layer is then deposited into the created pore. This can lead to complete encapsulation of the gate, making plating easier. Excess material formed on a bottom of the pore is removed with a suitable method including but not limited to plasma or wet etch. The pore is then overplated.

**[0070]** Conformal layer is subsequently substantially removed chemically, and the desired filament tip is then electrochemically etched to created the desired geometry.

**[0071]** The foregoing description of preferred embodiments of the present invention has been provided for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise forms disclosed. Obviously, many modifications and variations will be apparent to practitioners skilled in this art. The embodiments were chosen and described in order to best explain the principles of the invention and its practical application, thereby enabling others skilled in the art to understand the invention for various embodiments and with various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the following claims.

## Claims

1. A method of creating gated filament structures for a field emission display, comprising the consecutive or non-consecutive steps of:

   providing a multi-layer structure including a substrate (12), an insulating layer (18) positioned on the substrate (12) and a metal gate layer (20) positioned on at least a portion of a top surface of the insulating layer (18);
   providing a plurality of apertures (28) in the gate layer, each aperture extending through the gate layer from the top surface of the gate layer,

   **characterised by**:

   forming a plurality of spacers (36) adjacent to the edges of the apertures and extending into the apertures;
   using the spacers as masks for etching the insulating layer (18) so as to form a plurality of pores (40) in the insulating layer; and
   plating the plurality of pores (40) in the insulating layer to form filaments (22).

2. The method of claim 1, wherein the multi-layer structure further comprises:

   a conductive layer (14) on at least a portion of a top surface of the substrate.

3. The method of claim 1, further comprising:

   removing the spacers (36).

4. The method of claim 1, wherein the multi-layer structure further comprises:

   a metal row electrode (14) positioned on a top surface of the substrate; and
   a resistive layer (16) at least partially positioned on a top surface of the metal row electrode, with the insulating layer (18) positioned on a top surface of the resistive layer.

5. The method of claim 4, wherein the multi-layer structure further comprises:

a tracking resist layer (24) positioned on a top surface of the metal gate layer.

**6.** The method of claim 5, further comprising:

irradiating the multi-layer structure with charged energy particles to produce a plurality of tracks in the tracking resist layer.

**7.** The method of claim 1, further comprising:

removing a portion of the insulating layer (18) adjacent to the filaments.

**8.** The method of claim 5, further comprising:

irradiating the multi-layer structure with charged energetic particles to produce a plurality of tracks in the tracking resist layer;
etching the plurality of tracks to form a plurality of apertures (26) in the tracking resist layer; and
etching the metal gate layer to form the plurality of apertures (28).

**9.** The method of claim 3, wherein forming the plurality of spacers comprises:

applying a conformal layer into the apertures (28); and
removing the conformal layer (32) while leaving spacer material in the apertures.

**10.** The method of claim 5, wherein the tracking resist layer (24) is made of polycarbonate.

**11.** The method of claim 5, further comprising:

irradiating the multi-layer structure with energetic charged Xe.

**12.** The method of claim 6, wherein the plurality of tracks are etched to form the plurality of apertures (26) in the tracking resist layer with an aperture size at the metal gate layer of about 0.05 to 2.0 microns.

**13.** The method of claim 1, wherein the metal gate layer (20) is etched with a reactive ion etching which does not extend substantially into the insulating layer (18).

**14.** The method of claim 1, wherein the metal gate layer (20) is etched with a reactive ion etching which etches the insulating layer (18) at a slower rate than an etching rate of the metal gate layer.

**15.** The method of claim 9, wherein the conformal layer (32) is made of a material selected from silicon nitride, amorphous and small grained polycrystalline Si, or $SiO_2$.

**16.** The method of claim 1, wherein the metal gate layer (20) has a thickness of about 500 to 2000A.

**17.** The method of claim 9, wherein the thickness of the conformal layer (32) is about 50 nm.

**18.** The method of claim 1, wherein an anisotropic reactive ion etch is used to create the plurality of pores (40) in the insulating layer.

**19.** The method of claim 1, wherein undercutting of the insulating layer (18) is minimised.

**20.** The method of claim 4, wherein etching the insulating layer (18) to form the plurality of insulating pores does not extend substantially into the resistive layer (16).

**21.** The method of claim 4, wherein voltages on the resistive layer (16) and on the metal gate layer (20) are controlled to minimise plating filament material on the metal gate layer.

**22.** The method of claim 1, further comprising:

treating the filaments (22) to form a desired filament tip geometry.

**23.** The method of claim 1, wherein forming the filaments includes electroplating.

**24.** The method of claim 23, wherein the multi-layer structure includes a row electrode (14) positioned beneath the insulating layer and electroplating includes applying a potential to the row electrode.

**25.** The method of claim 1, further comprising:

electropolishing one or more of the plurality of filaments.

**26.** The method of claim 25, wherein electropolishing includes applying a potential to the gate layer.

**27.** The method of claim 1, further comprising:

pinching off the filament tip to provide the filament tip with a sharp geometry.

**28.** The method of claim 1, wherein the filaments are formed in the pores such that the filaments extend into the apertures and the spacers mask the edges of the apertures from formation of filament.

**29.** A field emission display device comprising a gated filament structure formed using a method as de-

fined in any preceding claim.

**Patentansprüche**

1. Verfahren zum Erzeugen von Gate-Faserstrukturen für eine Feldemissionsanzeigevorrichtung, wobei das Verfahren die aufeinander folgenden oder nicht aufeinander folgenden Schritte umfasst:

   Vorsehen einer mehrschichtigen Struktur, die ein Substrat (12), eine an dem Substrat (12) positionierte Isolierschicht (18) und eine metallische Gate-Schicht (20) aufweist, die an mindestens einem Teilstück einer oberen Oberfläche der Isolierschicht (18) positioniert ist;
   Vorsehen einer Mehrzahl von Öffnungen (28) in der Gate-Schicht, wobei sich jede Öffnung von der oberen Oberfläche der Gate-Schicht durch die Gate-Schicht erstreckt; **gekennzeichnet durch**:

      Bilden einer Mehrzahl von Abstandseinrichtungen (36) angrenzend an die Ränder der Öffnungen und sich in die Öffnungen erstreckend;
      Verwenden der Abstandseinrichtungen als Masken zum Ätzen der Isolierschicht (18), so dass eine Mehrzahl von Poren (40) in der Isolierschicht gebildet wird; und
      Plattieren der Mehrzahl von Poren (40) in der Isolierschicht, so dass Fasern (22) gebildet werden.

2. Verfahren nach Anspruch 1, wobei die mehrschichtige Struktur ferner folgendes umfasst:

   eine leitfähige Schicht (14) auf mindestens einem Teilstück einer oberen Oberfläche des Substrats.

3. Verfahren nach Anspruch 1, wobei das Verfahren ferner folgendes umfasst:

   Entfernen der Abstandseinrichtungen (36).

4. Verfahren nach Anspruch 1, wobei die mehrschichtige Struktur ferner folgendes umfasst:

   eine metallische Reihenelektrode (14), die an einer oberen Oberfläche des Substrats positioniert ist; und
   eine Sperrschicht (16), die mindestens teilweise an einer oberen Oberfläche der metallischen Reihenelektrode positioniert ist, wobei die Isolierschicht (18) an einer oberen Oberfläche der Sperrschicht positioniert ist.

5. Verfahren nach Anspruch 4, wobei die mehrschichtige Struktur ferner folgendes umfasst:

   eine Spurverfolgungs-Sperrschicht (24), die an einer oberen Oberfläche der metallischen Gate-Schicht positioniert ist.

6. Verfahren nach Anspruch 5, wobei das Verfahren ferner folgendes umfasst:

   Bestrahlen der mehrschichtigen Struktur mit geladenen Energieteilchen, um in der Spurverfolgungs-Sperrschicht eine Mehrzahl von Spuren zu erzeugen.

7. Verfahren nach Anspruch 1, wobei das Verfahren ferner folgendes umfasst:

   Entfernen eines Teilstücks der Isolierschicht (18) angrenzend an die Fäden.

8. Verfahren nach Anspruch 5, wobei das Verfahren ferner folgendes umfasst:

   Bestrahlen der mehrschichtigen Struktur mit geladenen Energieteilchen, um in der Spurverfolgungs-Sperrschicht eine Mehrzahl von Spuren zu erzeugen;
   Ätzen der Mehrzahl von Spuren, so dass eine Mehrzahl von Öffnungen (26) in der Spurverfolgungs-Sperrschicht gebildet wird; und
   Ätzen der metallischen Gate-Schicht, so dass die Mehrzahl von Öffnungen (28) gebildet wird.

9. Verfahren nach Anspruch 3, wobei das Bilden der Mehrzahl von Abstandseinrichtungen folgendes umfasst:

   Vorsehen einer konformen Schicht in den Öffnungen (28); und
   Entfernen der konformen Schicht (32), wobei Abstandseinrichtungsmaterial in den Öffnungen verbleibt.

10. Verfahren nach Anspruch 5, wobei die Spurverfolgungs-Sperrschicht (24) aus Polycarbonat hergestellt wird.

11. Verfahren nach Anspruch 5, wobei das Verfahren ferner folgendes umfasst:

    Bestrahlen der mehrschichtigen Struktur mit energetisch geladenem Xe.

12. Verfahren nach Anspruch 6, wobei die Mehrzahl von Spuren so geätzt wird, dass die Mehrzahl von Öffnungen (26) in der Spurverfolgungs-Sperrschicht mit einer Öffnungsgröße an der metalli-

schen Gate-Schicht von etwa 0,05 bis 2,0 Mikron gebildet wird.

**13.** Verfahren nach Anspruch 1, wobei die metallische Gate-Schicht (20) mittels reaktivem Ionenätzen geätzt wird, das sich im wesentlichen nicht in die Isolierschicht (18) erstreckt.

**14.** Verfahren nach Anspruch 1, wobei die metallische Gate-Schicht (20) mittels reaktivem Ionenätzen geätzt wird, wobei die Isolierschicht (18) mit einer niedrigeren Rate geätzt wird als der Ätzrate der metallischen Gate-Schicht.

**15.** Verfahren nach Anspruch 9, wobei die konforme Schicht (32) aus einem Werkstoff gebildet wird, der aus Siliziumnitrid, amorphem und kleinkörnigem polykristallinem Si oder $SiO_2$ ausgewählt wird.

**16.** Verfahren nach Anspruch 1, wobei die metallische Gate-Schicht (20) eine Dicke von etwa 500 bis 2000 A aufweist.

**17.** Verfahren nach Anspruch 9, wobei die Dicke der konformen Schicht (32) etwa 50 nm beträgt.

**18.** Verfahren nach Anspruch 1, wobei anisotropes reaktives Ionenätzen verwendet wird, um die Mehrzahl von Poren (40) in der Isolierschicht zu erzeugen.

**19.** Verfahren nach Anspruch 1, wobei das Unterätzen der Isolierschicht (18) so gering wie möglich gehalten wird.

**20.** Verfahren nach Anspruch 4, wobei das Ätzen der Isolierschicht (18) zum Bilden der Mehrzahl von isolierenden Poren sich im wesentlichen nicht in die Sperrschicht (16) erstreckt.

**21.** Verfahren nach Anspruch 4, wobei die Spannungen an der Sperrschicht (16) und an der metallischen Gate-Schicht (20) so geregelt werden, dass das Plattieren von Fasermaterial an der metallischen Gate-Schicht minimiert wird.

**22.** Verfahren nach Anspruch 1, wobei das Verfahren ferner folgendes umfasst:

Behandeln der Fasern (22), so dass eine gewünschte Faserspitzengeometrie gebildet wird.

**23.** Verfahren nach Anspruch 1, wobei das Bilden der Fasern das Elektroplattieren aufweist.

**24.** Verfahren nach Anspruch 23, wobei die mehrschichtige Struktur eine Reihenelektrode (14) aufweist, die unterhalb der Isolierschicht positioniert ist, und wobei das Elektroplattieren das Anlegen einer Spannung an die Reihenelektrode aufweist.

**25.** Verfahren nach Anspruch 1, wobei das Verfahren ferner folgendes umfasst:

Elektropolieren eines oder mehrerer der Mehrzahl von Fasern.

**26.** Verfahren nach Anspruch 25, wobei das Elektropolieren das Anlegen einer Spannung an die Gate-Schicht umfasst.

**27.** Verfahren nach Anspruch 1, wobei das Verfahren ferner folgendes umfasst:

Abklemmen der Faserspitze, um die Faserspitze mit einer spitzen Geometrie vorzusehen.

**28.** Verfahren nach Anspruch 1, wobei die Fasern in den Poren derart gebildet werden, dass sich die Fasern in die Öffnungen erstrecken und dass die Abstandseinrichtungen die Ränder der Öffnungen von der Faserbildung maskieren.

**29.** Feldemissionsanzeigevorrichtung, die eine Gate-Faserstruktur umfasst, die unter Verwendung eines Verfahrens gemäß der Definition in den vorstehenden Ansprüchen gebildet wird.

**Revendications**

**1.** Procédé de création de structures de filaments à grille pour un affichage à émission de champ, comprenant les étapes consécutives ou non consécutives consistant à :

fournir une structure multicouche comprenant un substrat (12), une couche isolante (18) positionnée sur le substrat (12) et une couche de grille métallique (20) positionnée sur au moins une partie d'une surface supérieure de la couche isolante (18) ;
fournir une pluralité d'ouvertures (28) dans la couche de grille, chaque ouverture s'étendant à travers la couche de grille à partir de la surface supérieure de la couche de grille,

**caractérisée par** :

la formation d'une pluralité d'espaceurs (36) adjacents aux bords des ouvertures et s'étendant dans les ouvertures ;
l'utilisation des espaceurs en tant que masques pour attaquer chimiquement la couche isolante (18) de manière à former une pluralité de pores

(40) dans la couche isolante ; et
la métallisation de la pluralité de pores (40) dans la couche isolante de manière à former des filaments (22).

**2.** Procédé selon la revendication 1, dans lequel la structure multicouche comprend en outre :

une couche conductrice (14) sur au moins une partie de la surface supérieure du substrat.

**3.** Procédé selon la revendication 1, comprenant en outre :

l'élimination des espaceurs (36).

**4.** Procédé selon la revendication 1, dans lequel la structure multicouche comprend en outre :

une électrode de ligne métallique (14) positionnée sur une surface supérieure du substrat ; et une couche résistive (16) au moins partiellement positionnée sur une surface supérieure de l'électrode de ligne métallique, la couche isolante (18) étant positionnée sur une surface supérieure de la couche résistive.

**5.** Procédé selon la revendication 4, dans lequel la structure multicouche comprend en outre :

une couche de résist de poursuite (24) positionnée sur une surface supérieure de la couche de grille métallique.

**6.** Procédé selon la revendication 5, comprenant en outre :

l'irradiation de la structure multicouche avec des particules d'énergie chargées pour produire une pluralité de pistes dans la couche de résist de poursuite.

**7.** Procédé selon la revendication 1, comprenant en outre :

l'élimination d'une partie de la couche isolante (18) adjacente aux filaments.

**8.** Procédé selon la revendication 5, comprenant en outre :

l'irradiation de la structure multicouche avec des particules d'énergie chargées pour produire une pluralité de pistes dans la couche de résist de poursuite ;
l'attaque chimique de la pluralité de pistes pour former une pluralité d'ouvertures (26) dans la couche de résist de poursuite ; et
l'attaque chimique de la couche de grille métallique pour former la pluralité d'ouvertures (28).

**9.** Procédé selon la revendication 3, dans lequel la formation de la pluralité d'espaceurs comprend :

l'application d'une couche conforme dans les ouvertures (28) ; et
l'élimination de la couche conforme (32) tout en laissant le matériau espaceur dans les ouvertures.

**10.** Procédé selon la revendication 5, dans lequel la couche de résist de poursuite (24) se compose de polycarbonate.

**11.** Procédé selon la revendication 5, comprenant en outre :

l'irradiation de la structure multicouche avec du Xe chargé en énergie.

**12.** Procédé selon la revendication 6, dans lequel la pluralité de pistes est attaquée chimiquement pour former la pluralité d'ouvertures (26) dans la couche de résist de poursuite avec une taille d'ouverture au niveau de la couche de grille métallique comprise entre environ 0,05 et 2,0 microns.

**13.** Procédé selon la revendication 1, dans lequel la couche de grille métallique (20) est attaquée chimiquement par attaque par ions réactifs qui ne s'étend sensiblement pas dans la couche isolante (18).

**14.** Procédé selon la revendication 1, dans lequel la couche de grille métallique (20) est attaquée chimiquement par attaque par ions réactifs qui attaque la couche isolante (18) à une vitesse moins rapide qu'une vitesse d'attaque de la couche de grille métallique.

**15.** Procédé selon la revendication 9, dans lequel la couche conforme (32) se compose d'un matériau sélectionné parmi le nitrure de silicium, le Si ou le $SiO_2$ amorphe polycristallin à petits grains.

**16.** Procédé selon la revendication 1, dans lequel la couche de grille métallique (20) présente une épaisseur comprise entre environ 500 et 2000 A.

**17.** Procédé selon la revendication 9, dans lequel l'épaisseur de la couche conforme (32) est d'environ 50 nm.

**18.** Procédé selon la revendication 1, dans lequel une attaque par ions réactifs anisotropes est utilisée pour créer la pluralité de pores (40) dans la couche isolante.

**19.** Procédé selon la revendication 1, dans lequel le dégagement de la couche isolante (18) est minimisé.

**20.** Procédé selon la revendication 4, dans lequel l'attaque chimique de la couche isolante (18) pour former la pluralité de pores isolants ne s'étend sensiblement pas dans la couche résistive (16).

**21.** Procédé selon la revendication 4, dans lequel les tensions sur la couché résistive (16) et sur la couche de grille métallique (20) sont contrôlées de manière à minimiser le matériau de filament de métallisation sur la couche de grille métallique.

**22.** Procédé selon la revendication 1, comprenant en outre :

le traitement des filaments (22) pour former une géométrie de bout de filament souhaitée.

**23.** Procédé selon la revendication 1, dans lequel la formation des filaments comprend la galvanoplastie.

**24.** Procédé selon la revendication 23, dans lequel la structure multicouche comprend une électrode de ligne (14) positionnée en dessous de la couche isolante, et la galvanoplastie comprend l'application d'un potentiel à l'électrode de ligne.

**25.** Procédé selon la revendication 1, comprenant en outre :

le polissage par anodisation d'un filament ou d'une pluralité de filaments.

**26.** Procédé selon la revendication 25, dans lequel le polissage par anodisation comprend l'application d'un potentiel à la couche de grille.

**27.** Procédé selon la revendication 1, comprenant en outre :

le pincement du bout de filament pour doter le bout de filament d'une géométrie pointue.

**28.** Procédé selon la revendication 1, dans lequel les filaments sont formés dans les pores de telle sorte que les filaments s'étendent dans les ouvertures et que les espaceurs masquent les bords des ouvertures de la formation des filaments.

**29.** Dispositif d'affichage à émission de champ comprenant une structure de filaments à grille formée en utilisant un procédé tel que défini dans l'une quelconque des revendications précédentes.

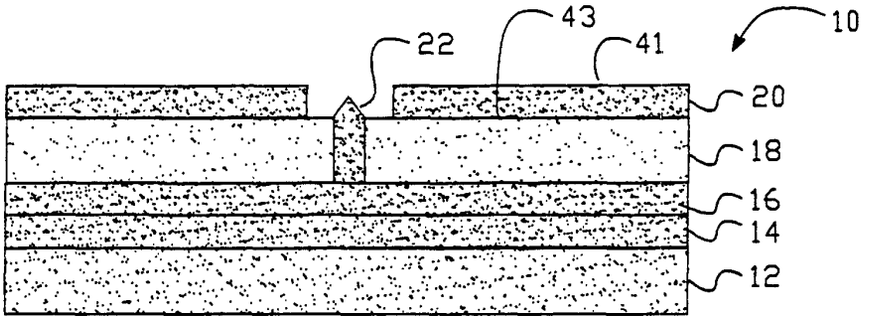


FIG.1

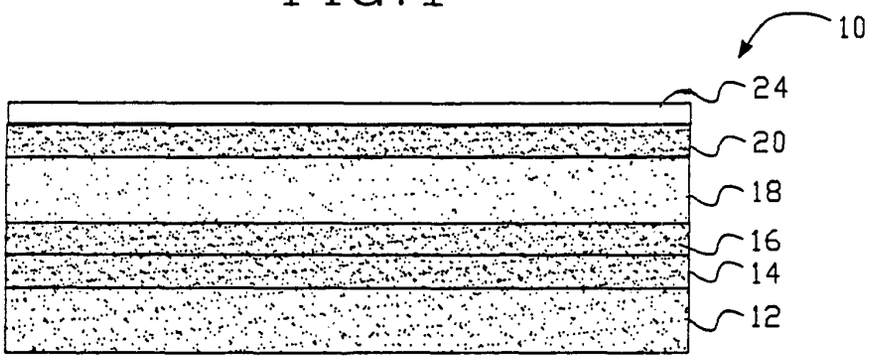


FIG.2

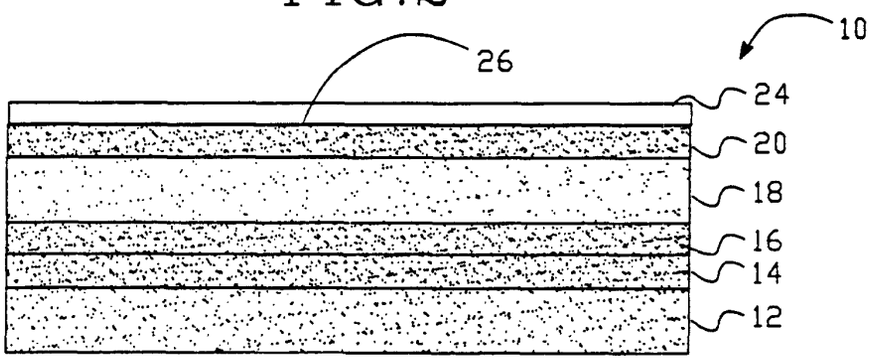


FIG.3

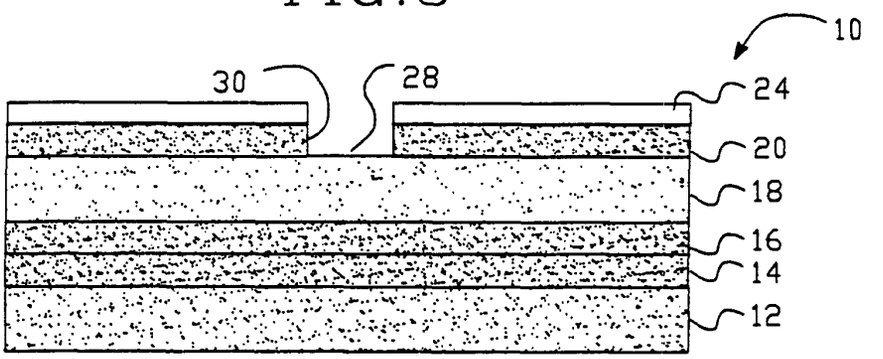


FIG.4

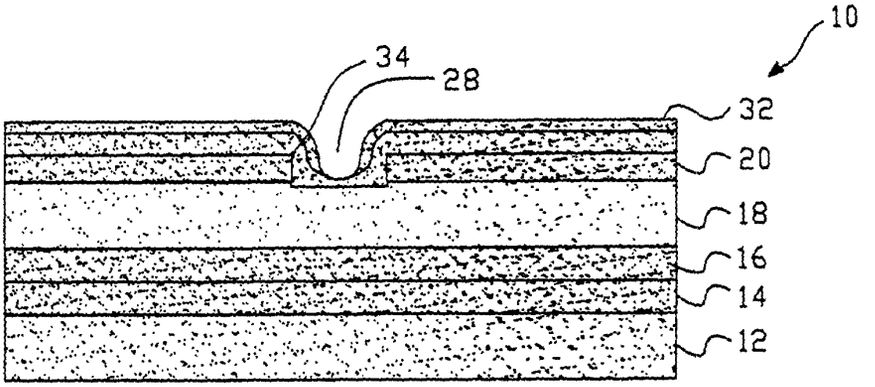


FIG.5a

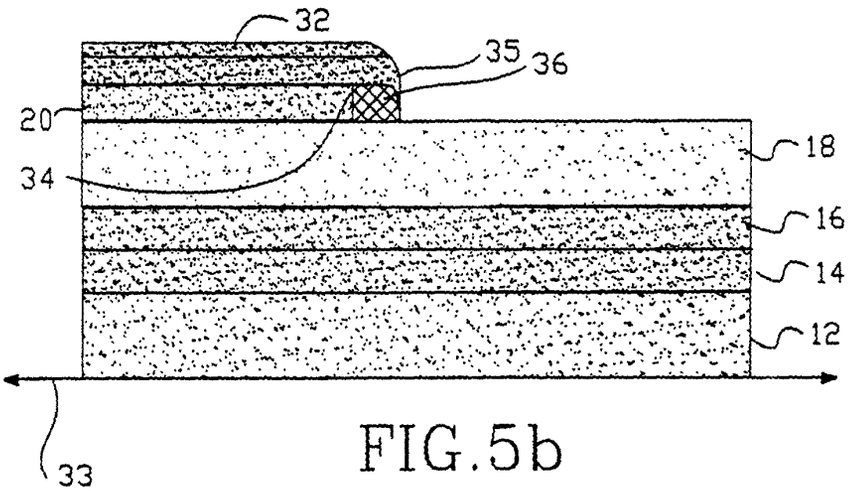


FIG.5b

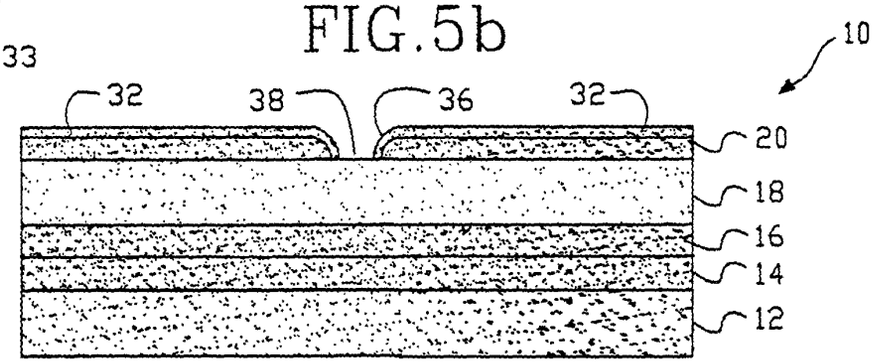


FIG.6

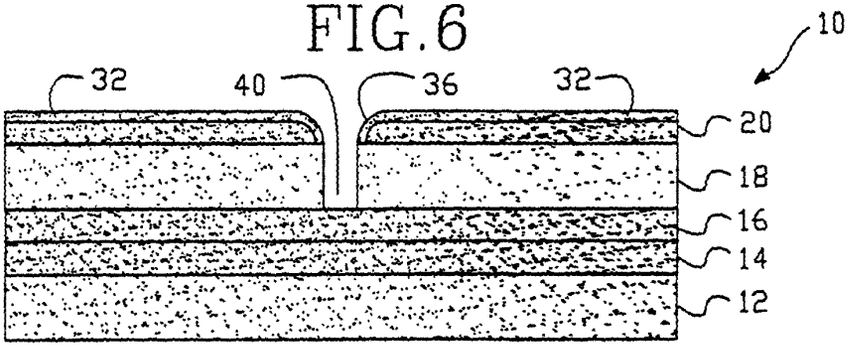


FIG.7

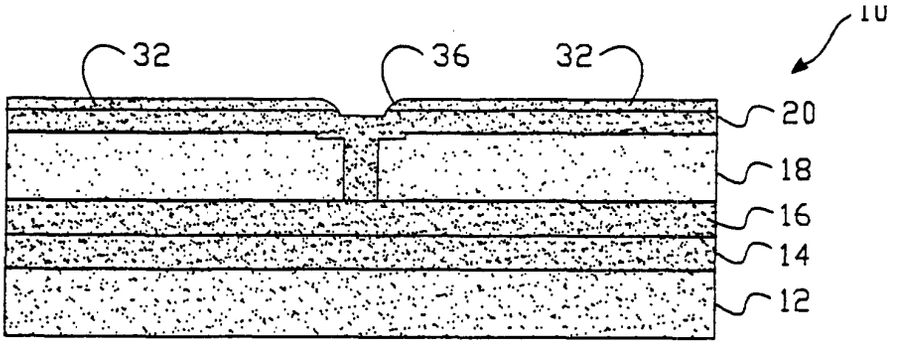


FIG.8

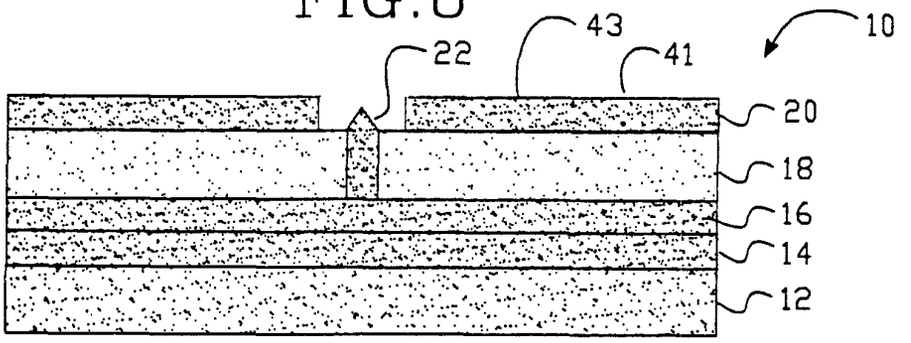


FIG.9

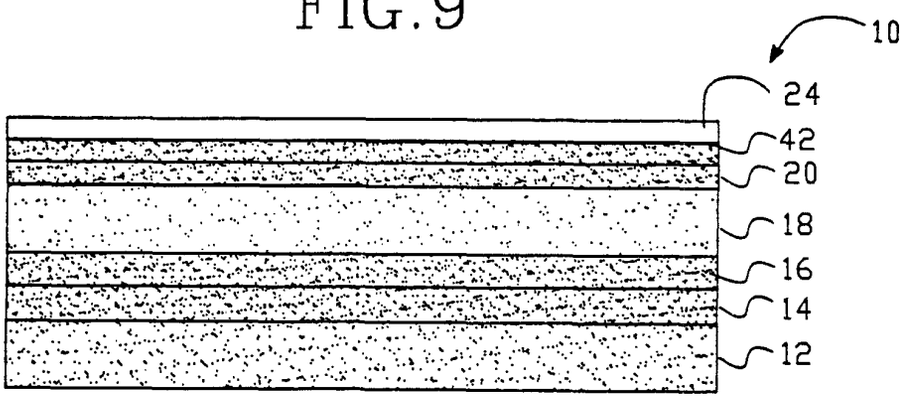


FIG.10

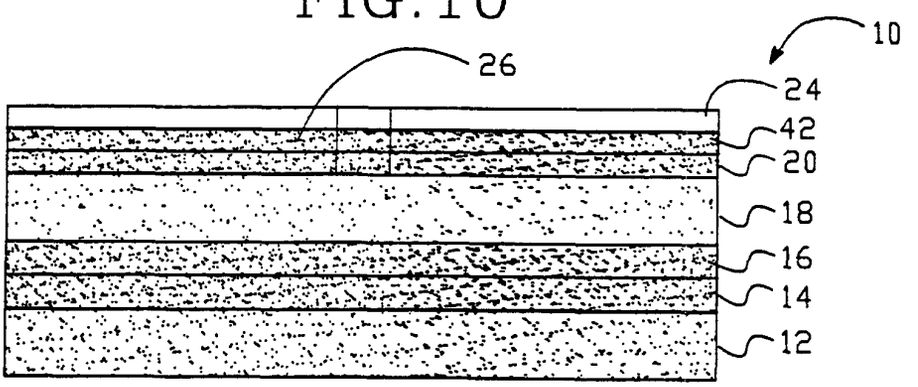


FIG.11

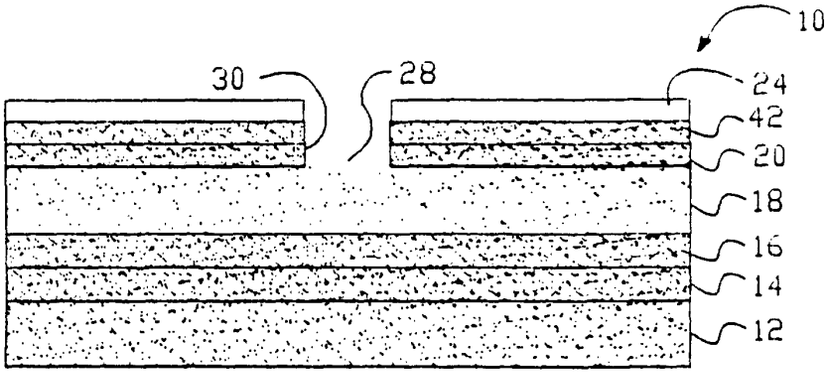


FIG.12

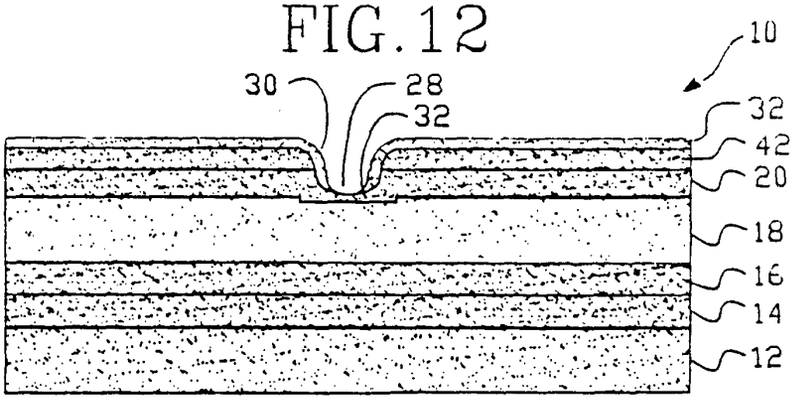


FIG.13

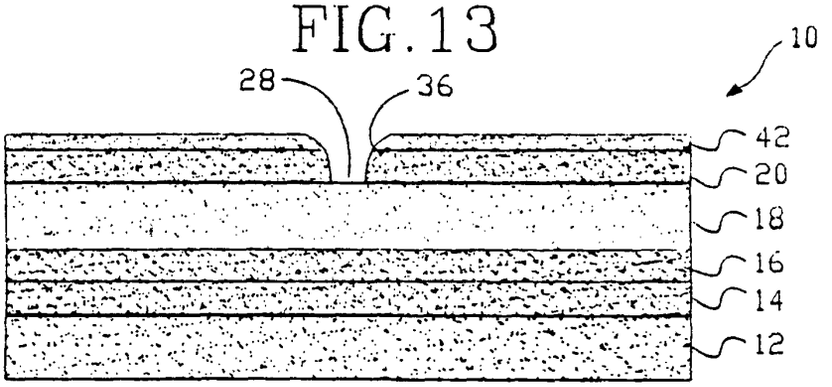


FIG.14

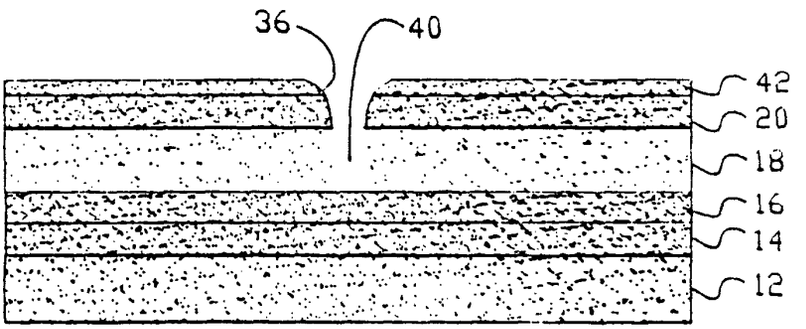


FIG.15

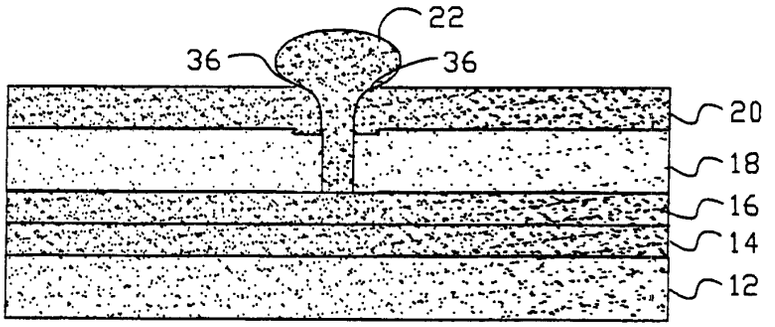


FIG.16

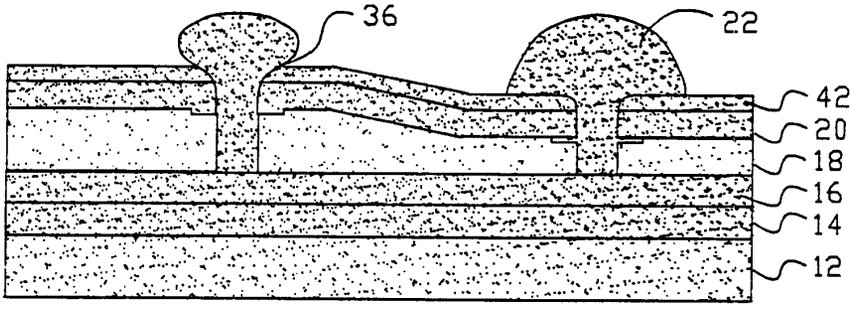


FIG.17

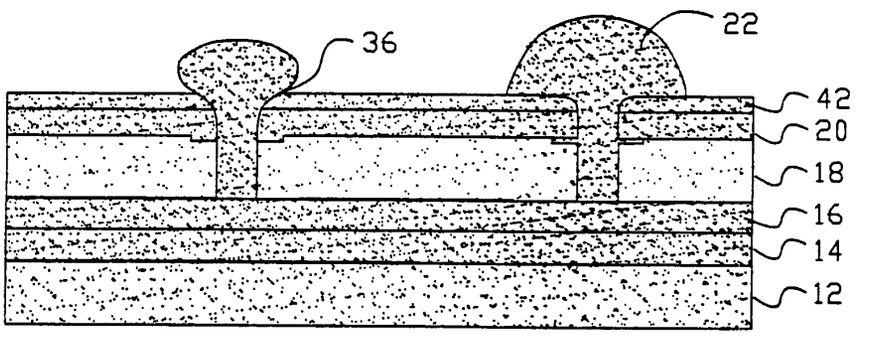


FIG.18

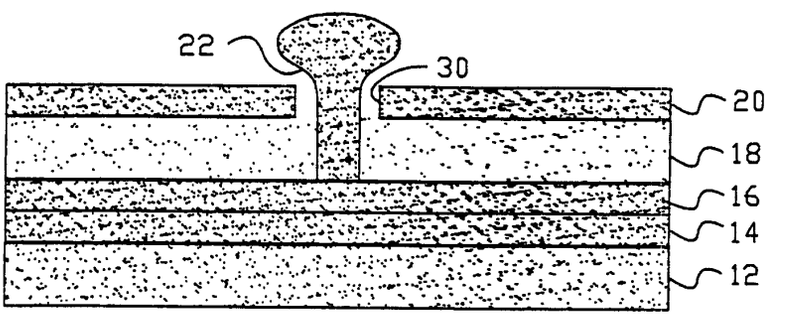


FIG.19

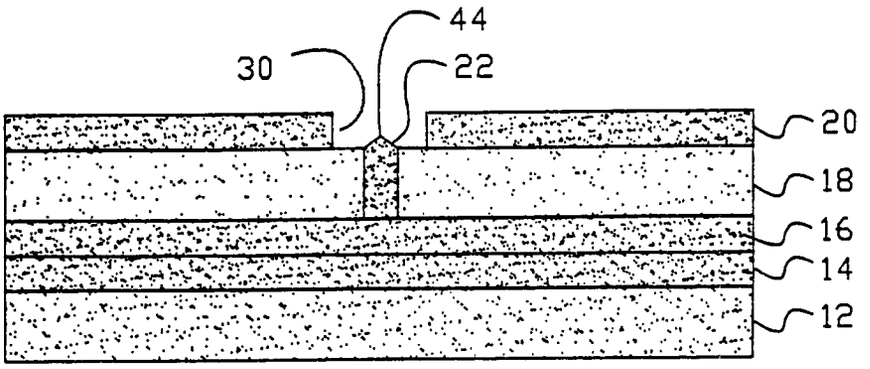


FIG.20

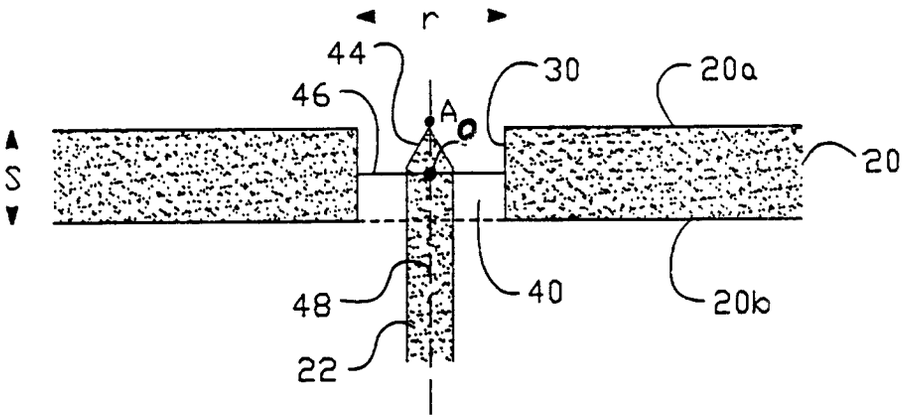


FIG.21