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(54) Drive device for scanning a monolithic integrated LED array

(57) A drive for a matrix of light emitting devices includes a plurality of column decoding switches (12) each including a plurality of column circuits, each circuit coupled to an individual column and a power source (50). An individual data line (C0 - C59) coupled to each decoding switch (12) for selecting and activating a specific decoding switch (12). A plurality of column address lines (A0 - A1) coupled to each of the decoding switches (12) for logically selecting a specific circuit. Similar row decoding switches (15) are optionally connected to the rows of the matrix and to a current sink (51) and similarly addressed. Whereby one contact of a selected LED is coupled to the current sink (51) by an addressed one of the row coupling circuits (15) and a second contact of the LED is coupled to the power source (50) by the addressed one of the column coupling circuits (12).

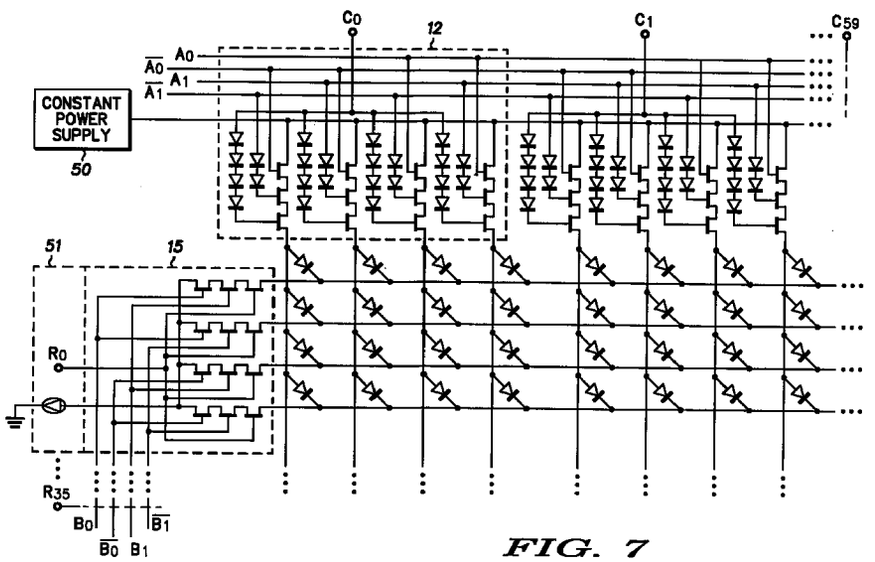


FIG. 7

EP 0 809 229 A2

Description

Field of the Invention

The present invention relates, in general, to display devices, and more particularly, to a novel drive device for operating a display.

More particularly, this invention relates to Light Emitting Device (LED) arrays, and more specifically to a monolithic drive device integrated with an LED array.

Background of the Invention

Matrix addressing techniques are well known in the art and have been utilized to control various types of displays such as light emitting diode displays, liquid crystal device (LCD) displays, and field emission device (FED) displays. Matrix addressing schemes typically organize the light emitting elements or pixels into a number of rows and columns with each pixel at an intersection of a particular row and a particular column. Illuminating the pixel requires activating an intersecting row and column thereby providing a closed current path that includes the pixel to be illuminated.

Circuitry for driving an LED matrix display having rows and columns with a plurality of pixels, includes a memory with a certain number of bits width, where the number of bits is equal to the number of pixels, a column output for supplying the number of bits in parallel to a matrix display connected to the column output, and row selection and driver circuitry connected to the memory and to the column output for selecting a complete row of bits of data stored in the memory and supplying the complete row of bits to the column output. Memory for the driver circuitry is for example any of the electronic memories available on the market including but not limited to ROMs, PROMs, EPROMs, EEPROMs, RAMs, etc.,.

Image information is generally supplied to the LED driver circuitry memory by way of a data input and is stored in a predetermined location by means of an address supplied to the address input. The stored data is supplied to the LED display a complete row at a time by way of a latch/column driver. Each bit of data for each column in the row is accessed in memory and transferred to a latch circuit. The current data is then supplied to the column drivers to drive each pixel in the row simultaneously. At the same time, a shift register is sequentially selecting a new row of data each time a pulse is received from a clock. The newly selected row of pixels is actuated by row drivers so that data supplied to the same pixels by a latch/column driver causes the pixel to emit the required amount of light.

There are two basic approaches for energizing the appropriate row and for transferring data to the appropriate columns. One approach uses decoders while the other approach uses shift registers. Referring to the decoder approach, each row or column is individually addressed. The circuitry required to sequence through the addresses is well understood by those skilled in the art and is not included herein for simplicity.

The shift register takes advantage of the fact that random access to the rows and columns is not generally required in matrix displays, they need only be addressed sequentially. The advantage to the shift register approach is that it only requires a clock pulse to initiate a new row sequence.

It should also be noted that an LED matrix display could be a simple monochrome configuration, a display utilizing monochrome grayscale, or color. For a simple monochrome display, only a one bit digital signal is needed for each pixel, as the pixel is either on or off. For a display utilizing monochrome grayscale, either an analog signal or a multi-bit digital signal is required. A sixteen level grayscale, for example, needs a four bit digital signal. Full color, generally requires at least three light emitting elements per pixel, one for each of the basic colors (red, green and blue), and a type of grayscale signal system to achieve the appropriate amount of each color.

Generally, in non-color type displays (black and white) each pixel contains a single light emitting device which must be driven in a range of values to achieve a range of gray (gray scale) between full on (white) and full off (black). In order to get good gray scale, the data drivers generally have to be able to deliver an accurate analog voltage to each pixel. However, analog driver circuits are very expensive and, since there must be hundreds of data drivers (one for each row of light emitting devices), are the major part of the display cost.

Further, in full color displays, each pixel contains at least three light emitting devices, each of which produces a different color (e.g. red, green, and blue) and each of which must be driven (generally a row at a time) in a range of values to achieve a range of that specific color between full on and full off. Thus, full color displays contain three times as many analog drivers, which at least triples the manufacturing cost of the display. Also, the additional analog drivers require additional space and power, which can be a problem in portable electronic devices, such as pagers, cellular and regular telephones, radios, data banks, etc.

As described above, the columns and rows of the LED matrix require drivers for each individual column or row with additional latching circuits for the column drivers. This configuration is heavily dependent on a large number of I/O terminal counts and the circuit becomes burdensome and not conducive to miniaturization.

Another major concern in adapting displays with large numbers of light emitting elements or pixels to portable applications is the issue of power dissipation. This is a concern for the light emitting elements within the display as well as for the drive electronics. In a typical matrix addressable display, the data is input serially and latched into the circuitry that drives the light emitting elements. Typically a row (or column) is illuminated only a small fraction of the time each time the display is scanned. Because of the high scan rate and the large

number of pixels involved, high clock rates are involved in the shifting of data into and out of the memory. The high scan rates and high clock rates required, results in excessive dynamic power dissipation.

Displays utilizing two dimensional arrays, or matrices, of pixels each containing one or more light emitting devices are very popular in the electronic field and especially in portable electronic and communication devices, because large amounts of data and pictures can be transmitted very rapidly and to virtually any location. One problem with these matrices is that each row (or column) of light emitting devices in the matrix must be separately addressed and driven with a video or data driver.

Accordingly, it would be advantageous to be able to manufacture displays, and especially color displays, with simpler and fewer data drivers and with fewer I/O terminals.

It is an object of the present invention to provide new and improved driven matrices of light emitting devices using digital data drivers.

It is another object of the present invention to provide new and improved driven matrices of light emitting devices using fewer data drivers.

It is a further object of the present invention to provide matrix display and driver circuitry which utilizes substantially less power than equivalent prior art displays.

It is still a further object of the present invention to provide improvements in decoding switches of monolithic matrices of LEDs.

It is still a further object of the present invention to provide LED displays which are less expensive, smaller, and easier to manufacture.

It is yet a further object of the present invention to provide LED displays which integrate decoding switches for column and row selection in a monolithic integrated array.

It is still another object of the present invention to provide LED displays with reduced I/O terminal count for column and row selection in LED matrices.

Summary of the Invention

Briefly, to achieve the desired objects of the instant invention in accordance with a preferred embodiment thereof, provided is a drive device and matrix of light emitting devices including a plurality of light emitting devices with each light emitting device having a first contact and a second contact, the first contacts being organized into a plurality of rows of first contacts and the second contacts being organized into a plurality of columns of second contacts. A plurality of row circuits is provided, coupling each row of first contacts to one of a current sink or a power source. A plurality of column decoding switches, is provided, each coupled to a plurality of individual columns of first contacts and to another of the current sink or the power source. A plurality of column data lines are coupled, one each column data line coupled to one each of the column decoding switches, for selecting and activating a selected column decoding switch when an activating signal is supplied to a column data line associated with the selected column decoding switch. A plurality of column address lines are coupled, each to each of the plurality of column decoding switches, for selecting an addressed one of the plurality of individual columns of first contacts coupled to the selected column decoding switch and coupling the addressed one of the plurality of individual columns to the another of the current sink or the power source. Whereby one contact of a selected light emitting device of the matrix is coupled to the current sink by a row circuit and another contact of the selected light emitting device is coupled to the power source by the addressed one of the plurality of individual columns.

Similar decoding switches may be used in either or both of the column and row circuits. All of the decoding switches used for either column or row scanning have common address lines. As a result, when the decoding switches are integrated onto the same chip as the LED matrix, the apparatus and the proposed scanning method provides a great reduction in the column and row related I/O terminal count.

Brief Description of the Drawings

The foregoing and further and more specific objects and advantages of the instant invention will become readily apparent to those skilled in the art from the following detailed description of a preferred embodiment thereof taken in conjunction with the drawings, in which:

FIG. 1 is a schematic simplified drawing which illustrates a light emitting diode array with monolithic driving circuit in accordance with the present invention;

FIG. 2 is a simplified block diagram which illustrating a plurality of LED array column decode switches;

FIG. 3 illustrates a truth table for the LED array column decode switches illustrated in FIG. 2;

FIG. 4 illustrates a truth table for the LED array row decode switches;

FIG. 5 is a schematic simplified drawing which illustrates a light emitting diode array column decode switch circuit;

FIG. 6 is a schematic simplified drawing which illustrates a light emitting diode array row decode switch circuit;

FIG. 7 is a schematic simplified drawing which illustrates a plurality of column decode switches and row decode switches of an array of light emitting diodes;

FIG. 8 is a simplified drawing which illustrates a plurality of epitaxial layers which comprise a current epi-structure of a switch with a light emitting diode array; and

FIG. 9 is a simplified drawing which illustrates a plurality of epitaxial layers which comprise a modified epi-structure of a switch with a light emitting diode array.

Description of the Preferred Embodiment

Turning now to the drawings in which like reference characters indicate corresponding elements throughout the several views, attention is first directed to FIG. 1 which illustrates a light emitting device (LED) array integrated circuit 10. Integrated circuit 10 includes an array 11 of 240 by 144 light emitting devices or elements designated pixels, each pixel with a unique column and row electrical connection. It will of course be understood that integrated circuit 10 is being utilized for purposes of this explanation and could in fact include any of a large variety of arrays and specifically, different numbers of columns and rows and/or different types of devices.

As illustrated in this embodiment of the instant invention, a plurality of column decoder switches 12 are attached to 60 column data lines, C0 through C59. Lines C0 through C59 are designated as data lines, with data signals interchangeably designated C0 through C59, and two pairs of complimentary input signals, A_0, $\overline{A_{\overline{0}}}$, A_1 and $\overline{A_{\overline{1}}}$, are applied as address signals to the four address lines, interchangeably designated A_0, $\overline{A_{\overline{0}}}$, A_1 and $\overline{A_{\overline{1}}}$. Each column decoder switch 12 is illustrated as having address signals A_0, $\overline{A_{\overline{0}}}$, A_1, and $\overline{A_{\overline{1}}}$, and one of C0 through C59 applied thereto. It will be understood that only two signals and their compliments are used herein because generally a single circuit can generate each signal and its compliment, resulting in further saving of circuitry and chip area. Four individual (i.e. separate and distinct) columns 13 of array 11 are coupled to each column decode switch 12, thereby the plurality of column decode switches 12 can address 60 by 4 for a total of 240 columns 13 of array 11. Column decoding switches 12 are proposed for use with an LED array monolithically integrated with the decoding switches to simultaneously reduce the chip I/O count. All of column decoding switches 12 used for column scanning have common address lines A_0, $\overline{A_{\overline{0}}}$, A_1, and $\overline{A_{\overline{1}}}$ coupled thereto. As a result, the proposed column decoding switch 12 provides a great reduction in the column related I/O count. The improvements provided by the reduced number of elements for driving the column circuits 13 includes, specifically, a reduction in the number of I/O terminals and in the array power dissipation.

The means of addressing columns 13 of array 11 is generally as follows:

Column Selection

Set C_0=1 and C_1 through C_{59} to zero, thereby selecting columns 0,2,4 or 6; and
select a specific column 0,2,4 or 6 by providing a high signal to different pairs of A_0, $\overline{A_{\overline{0}}}$, A_1, or $\overline{A_{\overline{1}}}$ (e.g. A_0, A_1; A_0, $\overline{A_{\overline{1}}}$; $\overline{A_{\overline{0}}}$,$A_1$; or $\overline{A_{\overline{0}}}$, $\overline{A_{\overline{1}}}$).

Set C_0=0, C_1=1 and C_2 through C_{59} to zero, thereby selecting columns 1,3,5, or 7; and
select a specific column 1, 3, 5, or 7 by providing a high signal to different pairs of A_0, $\overline{A_{\overline{0}}}$, A_1, or $\overline{A_{\overline{1}}}$.
Set C_0 and C_1 to 0, C_2=1 and C_3 through C_{59} to zero, thereby selecting columns 8, 10, 12, or 14, etc.

It is now evident that this sequence can be maintained for the selection of four discrete columns 13 by the activation of a data input, C_0 through C_{59}, and the activation of address lines A_0, $\overline{A_{\overline{0}}}$, A_1, and $\overline{A_{\overline{1}}}$ then selects a specific column from the four discrete columns. Column decoding switches 12 have characteristics which provide a sequential scanning means to also reduce the array power dissipation from the reduced number of chip I/O counts.

Also illustrated in FIG. 1 is a plurality of row decoder switches 15, each with an individual data line of a plurality of input data lines R_0 through R_{35} coupled thereto (for a total of 36 row decoder switches 15 in this embodiment). Four individual (i.e. separate and distinct) rows 14 of array 11 are coupled to each row decoder switch 15. Each row decoder switch 15 is activated by the individual signal on data lines R_0 through R_{35} coupled thereto and by signals on row address lines B_0, $\overline{B_{\overline{0}}}$, B_1, and $\overline{B_{\overline{1}}}$. The means of addressing rows 14 of array 11 is generally as follows:

Row Selection

Set R_0=1 and R_1 through R_{35} to zero, thereby rows 0,2,4, or 6 are selected; and
select a specific row 0,2,4, or 6 by providing a high signal to different pairs of B_0, $\overline{B_{\overline{0}}}$, B_1, or $\overline{B_{\overline{1}}}$ (e.g. B_0,B_1; B_0, $\overline{B_{\overline{1}}}$; $\overline{B_{\overline{0}}}$,$B_1$; or $\overline{B_{\overline{0}}}$, $\overline{B_{\overline{1}}}$).
Set R_0=0 and R_1=1 and R_2 through R_{35} to zero, thereby rows 1,3,5, or 7 are selected; and
select a specific row 1,3,5, or 7 by providing a high signal to different pairs of B_0, $\overline{B_{\overline{0}}}$, B_1, or $\overline{B_{\overline{1}}}$.
Set R_0 and R_1=0, R_2= 1, and R_3 through R_{35} to zero, thereby rows 8,10,12, or 14 are selected; etc.

Columns 13 and rows 14 can be selected one by one or one out of four columns/rows from each decoding switch at once with this logic. The number of I/O counts is thereby greatly reduced and the alternating of the data input and the address lines are the means of selecting the required columns 13 and rows 14. By the monolithic integration of the low power column decoding switches 12 and row decoding switches 15 with LED array 11 on the same substrate, there is a great reduction in power. For instance, in a conventional decoder, the power expended for the aforementioned 240 by 144 LED array is 11 watts compared to 79 milliwatts for the column decoder switch 12 and row decoder switch 15 assembly of the instant invention. The added reduction of I/O counts, from 384 to 140 is a great improvement over conventional decoder circuits.

A fixed power supply (see FIG 7) is include in a silicon driver integrated circuit and connected as a power source to column decoding circuits 12. Also, a constant current sink circuit (see FIG. 7) is included in the silicon driver integrated circuit and connected as a power return circuit from row drivers 15. All of column decoding switches 12 have common address lines. As a result, the columns can be scanned sequentially, with no greater than n/4 (where n is the total number of columns) column decoders 12 at once depending on the input signal from the column input select lines, C_n. All of row decoding switches 15 have common address lines. As a result, the rows can be scanned sequentially, with no greater than m/4 (where m is the total number of rows) row decoders 14 at once depending on the row input signal, R_n. Power dissipation is limited by the MESFET leakage current. As a result, the power dissipation is much lower than that obtained from LED array 11 with a conventional decoding switch. The instant invention thereby reduces the number of I/O terminals required to address LED each pixel of array 11 and greatly reduces the power consumption of LED integrated circuit 10.

By the monolithic integration of low power column decoding switches 12 and row decoding switches 15 with LED array 11 on the same substrate, there is a great reduction in power dissipation. For instance, in a conventional decoder, the power expended for the aforementioned 240 by 144 LED array 11 is 11 watts compared to 79 milliwatts for LED integrated circuit 10 of the instant invention. The added reduction of I/O terminals, from 384 to 140 (in this specific example) illustrates the great improvement over conventional decoder circuits.

Turning now to FIG. 2, a single column decoder switch 12_n (representative of all column decoder switches 12) is illustrated in block form. Decoder switch 12_n includes a plurality of column decoder circuits 16, 17, 18, and 19 connected to output a signal to one of column 0 through column 3 of LED array 11 in response to appropriate address signals. Associated with this illustration is a truth table 30 illustrated in FIG. 3 which will be referenced as the illustration of FIG. 2 is described. Truth table 30 illustrates the signal levels of each address line, A_0, $\overline{A_0}$, A_1, $\overline{A_1}$, which are designated as a '1' or a '0', with column decoder switch 12_n selected by a high data signal C_n.

Referring to truth table 30, it should again be noted that A_0 and $\overline{A_0}$ are complementary signals and A_1 and $\overline{A_1}$ are complementary signals so that when one of the pair is a logic high the other is a logic low level. A first row 31 illustrates the logic signals required for the selection of column circuit 16, note that the data line C_n is at a logic high level, A_0 and A_1 are at a logic low level and $\overline{A_0}$ and $\overline{A_1}$ are at a logic high level. Referring now to a second row 32 in truth table 30, which illustrates the logic signals required for the selection of column circuit 17, the data line C_n is still at a logic high level, with A_0 and $\overline{A_1}$ being a logic low level and $\overline{A_0}$ and A_1 being a logic high level. In a third row 33 in truth table 30, which illustrates the logic signals required for the selection of column circuit 18, the data line C_n is still at a logic high level, with A_0 and $\overline{A_1}$ being a logic high level and $\overline{A_0}$ and A_1 being a logic low level. Finally, in a fourth row 34 in truth table 30, which illustrates the logic signals required for the selection of column circuit 19, the data line C_n is still at a logic high level, with A_0 and A_1 being a logic high level and $\overline{A_0}$ and $\overline{A_1}$ being a logic low level. Thus, any column decoder switch 12_n is selected by applying a logic high level signal to the associated data line C_n and any of the columns attached to the selected decoder switch 12_n are selected by activating an appropriate combination of address line A_0, $\overline{A_0}$, A_1, and $\overline{A_1}$.

FIG. 4 illustrates a selection logic truth table 40 for row decoder switches 15_n, which is similar to the column selection of truth table 30. A specific row decoder switch 15_n (representative of all row decoder switches 15) is selected by supplying a logic high level signal to the associated data line R_n. Within the selected row decoder switch 15_n, selection of one of four rows is accomplished by means of address lines B_0, $\overline{B_0}$, B_1, and $\overline{B_1}$. Data line R_n is, when activated, designated a 1 in the circuit logic. With address lines at a high level, which is designated by a 1 in truth table 40, the variation of inputs from the address lines determines which of the rows attached to decoder switch 15_n will be activated. As described in conjunction with truth table 30 of FIG. 3, the four rows 41 through 44 of truth table 40 illustrate the logic required for the selection of the four rows of array 10 associated with the particular decoder switch 15_n.

Turning now to FIG. 5, a schematic diagram of a preferred embodiment of a single column decoder circuit 20 (four of which are included in each column decoder switch 12, as will be explained presently) is illustrated. Column decoder circuit 20 includes three field effect transistors (FETs) 21, 22, and 23 connected in series between a terminal 24, adapted to have a source of power connected thereto (5 volts in the embodiment), and a specific column 13_n (illustrated as terminal 13_n). As will be explained presently, terminal 24 is connected to similar terminals of the other four column decoder circuits in the column decoder switch and to a fixed power supply. Address line A_0 is illustrated as an electrical terminal coupled to the gate of FET 21. FET 21 will couple the potential from terminal 24 to second FET 22 when a high signal is delivered on address line A_0. FET 21 will not conduct when the address line A_0 has a low signal applied thereto.

Address line A_1 supplies an activating signal to the gate of FET 22 which signal path contains two level shifting diodes 25 and 26. Level shifting diodes 25 and 26 provide a voltage shift to the gate of FET 22 to prevent forward biasing the gate-drain diode of FET 22. As illustrated, FET 22 will conduct when address signal A_1 is at a high level and will couple the potential from FET 21 to FET 23. However, if FET 21 is not conducting then there is nothing to couple to FET 23. A low level logic

signal from address line A_1 will prevent FET 23 from conducting.

Four level shifting diodes, 27, 28, 29, and 30 are connected in series with the gate terminal of FET 23 and provide a circuit path for data line C_n, which will either turn on FET 23 and couple a potential from FET 22 on a high signal or will prevent any activation signal from reaching column 13_n, if the signal on data line C_n is a low signal. The four level shifting diodes, 27, 28, 29, and 30 provide increased level shiftin of data line C_n from the increased number of diodes.

Referring to FIG. 6, a row decoding switch 33 is illustrated including three series connected FETs 34, 35, and 36 having address lines B_0 and B_1, and row data signal R_n, respectively, attached to the gates thereof. The free terminal of FET 34 is connected to an associated row 14_n, illustrated as a terminal 14 in FIG. 6. FET 34 couples row 14 to FET 35 upon an activation signal (logic high) being applied to address line B_0. The signal on data line B_1 must be at a logic high level to activate FET 35 to further complete an electrical circuit to FET 36. Data line R_n must now be at a logic high level to complete the electrical circuit from row 14_n to a current sink, illustrated as a terminal 38. As will be explained presently, terminal 38 is connected to similar terminals of the other four row decoder circuits in the row decoder switch and to a constant current sink. Electrical conductivity from row 14_n to terminal 38 completes an electrical circuit which activates any light emitting device or devices coupled between the intersection of column 13_n and row 14_n to emit light.

FIG. 7 illustrates a plurality of LED's in array 11 comprised of column 0 through column 2^n-1 and row 0 through row 2^m-1. For purposes of this explanation, LED_0 is electrically connected to column decoder switch 12_0 and row decoder switch 15_0, as a singular illustration of a plurality of column decoder switches 12 and a plurality of row decoder switches 15 connected to a plurality of columns and rows of LEDs in array 11 for addressing and activating a specific LED. FIG. 7 illustrates schematically a column decoder switch 12 (described in FIGS. 1, 2, and 3), which couples a fixed power source 50 to four columns, and a row decoder switch 15, which completes a circuit to a current sink 51 by electrically connecting a selected row thereto. As illustrated, there are a plurality of LED circuits which are of identical operation to the circuit described.

Because of the novel column and row decoder switches 12 and 15, respectively, there is a great reduction in power dissipation in LED array 11, from 11 watts in a conventional decoder to 79 milliwatts in the decoding switches and array of the instant invention. There is also a great reduction in I/O terminals on LED array integrated circuit 10 as illustrated in FIG. 1, from 384 to 140 I/O terminals in an LED array integrated with the decoding switches of the present invention.

Illustrated in FIG. 8 is an epi-structure 80 with monolithic integration of a low power decoding switch 82 (illustrated as a single FET) and an LED array 83 (illustrated as a single LED) onto the same substrate. LED array 83 includes a plurality of doped and undoped epitaxial layers formed sequentially on a simi-insulating gallium arsenide substrate 84. As illustrated, the epitaxial layers are an n+-GaAs layer 85, a n-InGap layer 86, an n-AlInP layer 87, an undoped AlGaInP layer 88, an undoped AlInP layer 89, a p-AlInP layer 90, a p-InGaP layer 91 approximately 200Å thick , and an undoped GaAs layer 92 approximately 500Å thick to form LED array 83 integrated with corresponding switch 82. Also illustrated are implants 94. provided for pixel isolation, implant 95 provided electrical connection to the lower terminal of each pixel, and implant 96 provided for row isolation. Metalized connections to each LED in array 83 are provided by contacts 97 and 98. Switch 82 includes device isolation implants 100, source and drain connection implants 102 and 104, and metalized contacts 112, 113, and 114 for source, gate and drain terminals, respectively. Additional information on this type of array can be found in U.S. Patent No. 5,453,386, entitled "Method of Fabrication of Implanted LED Array", issued September 26, 1995, and assigned to the same assignee. Also, for integration techniques, see U.S. Patent No. 5,483,085, entitled "Electro-Optic Integrated Circuit With Diode Decoder" issued January 9, 1996 and assigned to the same assignee.

A modified epi-structure 120 is illustrated in FIG. 9 which includes a decoding switch 122 integrated with an LED array 130 as a monolithic integration onto the same substrate. LED array 130 is similar to LED array 83 of FIG. 8. Decoding switch 122 is similar to switch 82 of FIG. 8 except that is fabricated by adding additional epitaxial layers after LED array 130 is fabricated so that p-dopant outdiffusion from LED 130 to FET 122 during the device fabrication is less of a problem.

Accordingly, methods of manufacturing displays, and especially color displays, with simpler and fewer data drivers and with fewer I/O terminals have been disclosed. Also disclosed are new and improved driven matrices of light emitting devices using digital data drivers and, specifically, matrices of light emitting devices using fewer data drivers. Further, matrix display and driver circuitry is disclosed which utilizes substantially less power than equivalent prior art displays and which are less expensive, smaller, and easier to manufacture. The present invention provides LED displays which integrate decoding switches for column and row selection in a monolithic integrated array with substantially reduced I/O terminal count for column and row selection in LED matrices. It will of course be understood that an LED display can be provided with only one of the assembly of column or row decoding switches and the other of the assembly of row or column (these are of course interchangeable) decoding switches can be replaced with normal hardwired connections, some form of decoding, a shift register, or the like.

Power dissipation is limited by MESFET leakage current. As a result, the power dissipation is much lower than that obtained from an array with conventional

decoders.

All the column decoding switches have common address lines. As a result, the column can be scanned sequentially or as n/4 where n is the number of columns at once depending on the input power supply from a driver. All the row decoding switches have common address lines. As a result rows can be scanned sequentially or as m/4 where m is the number of rows at once depending on the status of input row control signal, R_n. Level shifting diodes used to prevent a MESFET gate from being driven into forward bias are integrated with MESFETs. As a result the output voltage of the decoding switch is compatible with the output voltage of commercial TTL circuits.

The instant invention reduces the number of I/O terminals to activate LED pixels and greatly reduces the power consumption of the LED integrated circuit. By monolithic integration of a low power decoding switch with an LED array on the same substrate, there is a great reduction in power. For instance, in a conventional decoder, the power expended for a 240 by 144 LED array is 11 watts compared to 79 milliwatts for a decoder switch LED array of the instant invention. The added reduction of I/O terminals, from 384 to 140 is a great improvement over the array without the integration of decoding switches.

Various modifications and changes to the embodiments herein chosen for purposes of illustration will readily occur to those skilled in the art. For example, the integrated circuit can be formed in any convenient semiconductor material system or in any convenient organic system. Also, the LED array and switches can be formed in a variety of ways while still performing the stated functions. Further, a variety of different light emitting devices may be utilized and fabricated in a variety of somewhat modified and/or interchanged steps.

The foregoing is given by way of example only. Other modifications and variations may be made by those skilled in the art without departing from the scope of the invention as defined by the following claims.

Having fully described and disclosed the present invention and preferred embodiments thereof in such clear and concise terms as to enable those skilled in the art to understand and practice same, the invention claimed is:

Claims

1. A drive device and matrix of light emitting devices characterized by:

   a matrix (11) including a plurality of light emitting devices with each light emitting device having a first contact and a second contact, the first contacts being organized into a plurality of rows (14) of first contacts and the second contacts being organized into a plurality of columns (13) of second contacts;
   a plurality of row circuits (15) coupling each row (14) of first contacts to one of a current sink or a power source (50, 51);
   a plurality of column decoding switches (12), each coupled to a plurality of individual columns (13) of first contacts and to another of the current sink or the power source (50, 51);
   a plurality of column data lines (A0 - A1), one each column data line (A0 - A1) coupled to one each of the column decoding switches (12) for selecting and activating a selected column decoding switch (12) when an activating signal is supplied to a column data line (A0 - A1) associated with the selected column decoding switch (12); and
   a plurality of column address lines (C0 - C59), each coupled to each of the plurality of column decoding switches (12) for selecting an addressed one of the plurality of individual columns (13) of first contacts coupled to the selected column decoding switch (12) and coupling the addressed one of the plurality of individual columns (13) to the another of the current sink (51) or the power source (50);
   whereby one contact of a selected light emitting device of the matrix (11) is coupled to the current sink (51) by a row circuit (15) and another contact of the selected light emitting device is coupled to the power source (50) by the addressed one of the plurality of individual columns (13).

2. A drive device and matrix of light emitting devices as claimed in claim 1 further characterized in that the light emitting devices include one of organic light emitting devices, semiconductor light emitting diodes, and liquid crystal devices.

3. A drive device and matrix of light emitting devices as claimed in claim 1 further characterized in that each of the plurality of column decode switches (12) includes a first transistor (21) with current carrying electrodes forming first and second current carrying terminals of the column decode switch, and a control electrode.

4. A drive device and matrix of light emitting devices as claimed in claim 3 further characterized in that each of the plurality of column decode switches (12) further includes a second transistor (22) with a first current carrying electrode connected to the second current carrying terminal of the first transistor (21), a second current carrying terminal, a plurality of diodes, and a control electrode.

5. A drive device and matrix of light emitting devices as claimed in claim 4 further characterized in that each of the plurality of column decode switches (12) includes a first of the plurality of column address lines (A0 - A1) coupled to the control elec-

trode of the first transistor (21) and a second of the plurality of column address lines (A0 - A1) coupled to the control electrode of the second transistor (22).

6. A drive device and matrix of light emitting devices as claimed in claim 5 further characterized in that each of the plurality of column coupling circuits (12) further includes a third transistor (23) with a first current carrying electrode connected to the second current carrying terminal of the second transistor (22), a second current carrying terminal, a plurality of diodes (27, 28, 29, 30), and a control electrode, and the plurality of column coupling circuits (12) further includes the column data line (CN) associated with the selected column decoding switch (12) coupled to the control electrode of the third transistor (23).

7. A drive device and matrix of light emitting devices as claimed in claim 1 further characterized in that each of the plurality of row circuits (15) includes a first transistor (34) with current carrying electrodes forming first and second current carrying terminals of the column decode switch, and a control electrode.

8. A drive device and matrix of light emitting devices as claimed in claim 7 further characterized in that each of the plurality of row circuits (15) further includes a second transistor (35) with a first current carrying electrode connected to the second current carrying terminal of the first transistor (34), a second current carrying terminal, and a control electrode.

9. A drive device and matrix of light emitting devices as claimed in claim 8 further characterized in that each of the plurality of row circuits (12) includes a first of a plurality of row address lines (B0 - B1) coupled to the control electrode of the first transistor (34) and a second of the plurality of row address lines (B0 - B1) coupled to the control electrode of the second transistor (35).

10. A drive device and matrix of light emitting devices as claimed in claim 9 further characterized in that each of the plurality of row circuits (15) further includes a third transistor (36) with a first current carrying electrode connected to the second current carrying terminal of the second transistor (35), a second current carrying terminal, and a control electrode, and the plurality of row coupling circuits (15) further includes a row data line (RN) associated with the selected row decoding switch (15) coupled to the control electrode of the third transistor (36).

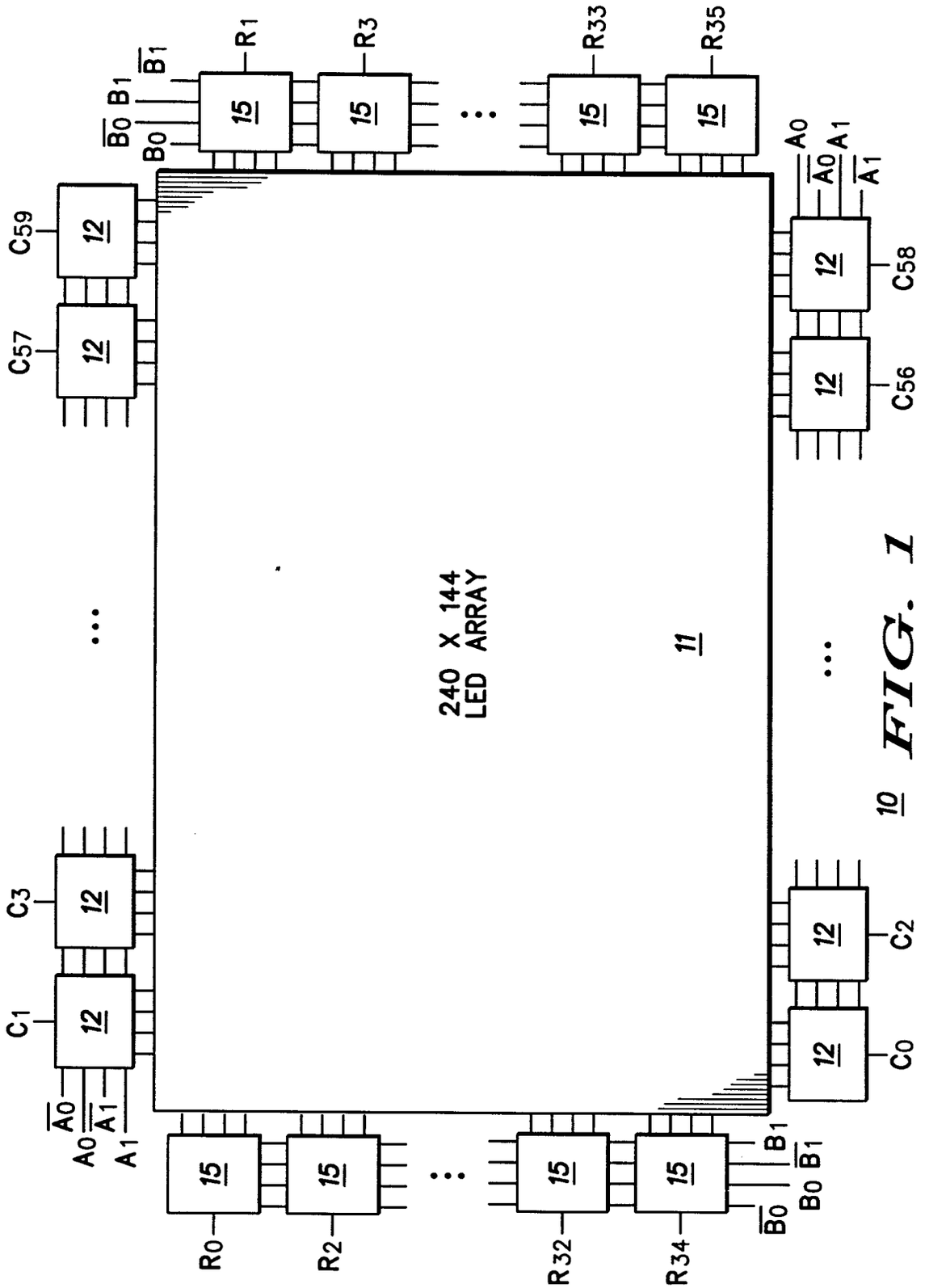

240 X 144
LED ARRAY
11
10
R0
R1
R2
R3
R32
R33
R34
R35
C0
C1
C2
C3
C56
C57
C58
C59
A0
A1
B0
B1
12
15

FIG. 1

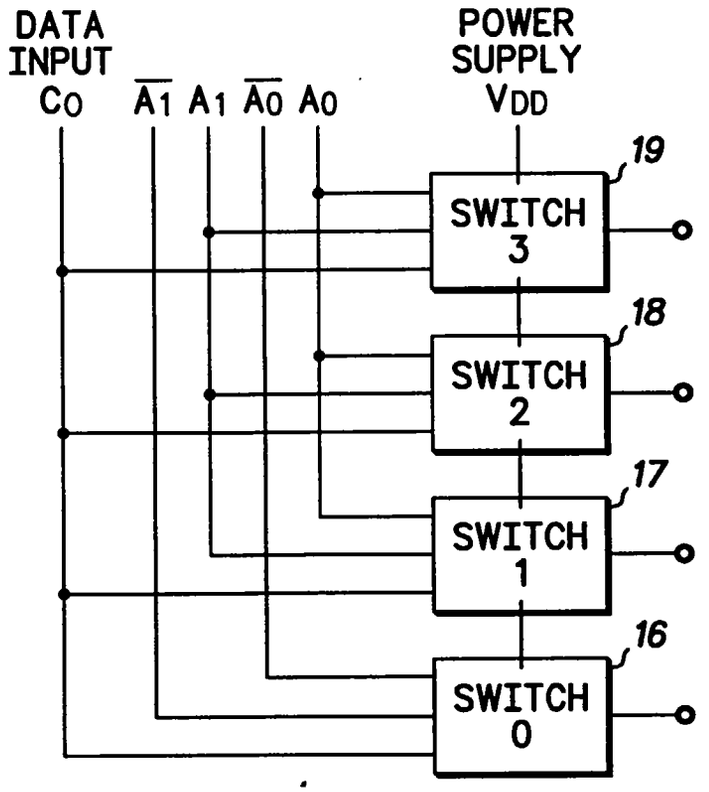


FIG. 2

12

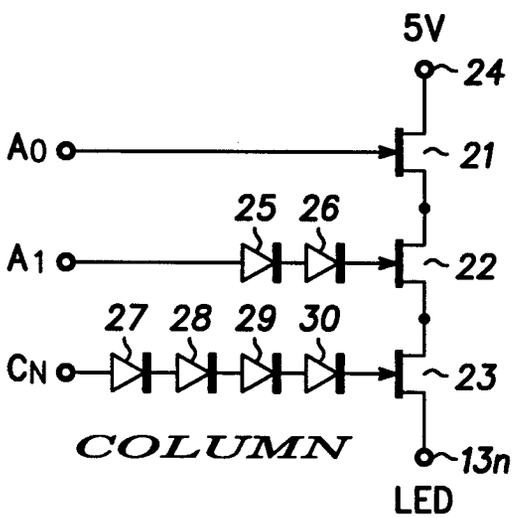
CN	A0	$\overline{A0}$	A1	$\overline{A1}$	COLUMN SELECTED	
1	0	1	0	1	0	31
1	0	1	1	0	1	32
1	1	0	0	1	2	33
1	1	0	1	0	3	34

FIG. 3

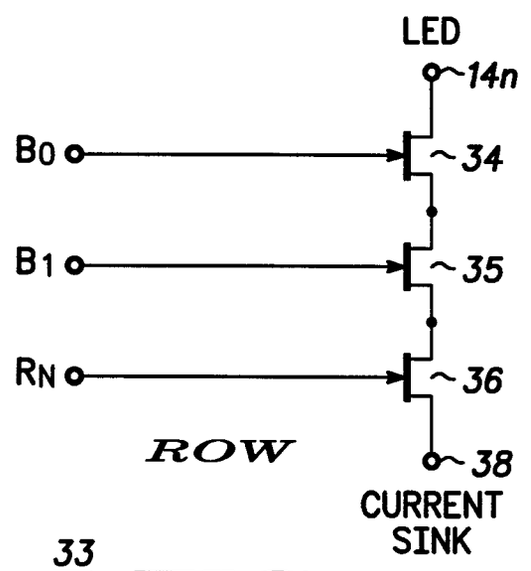
30

R_N	B_0	$\overline{B_0}$	B_1	$\overline{B_1}$	ROW SELECTED	
1	0	1	0	1	0	~41
1	0	1	1	0	1	~42
1	1	0	0	1	2	~43
1	1	0	1	0	3	~44

40 FIG. 4



20 FIG. 5



33 FIG. 6

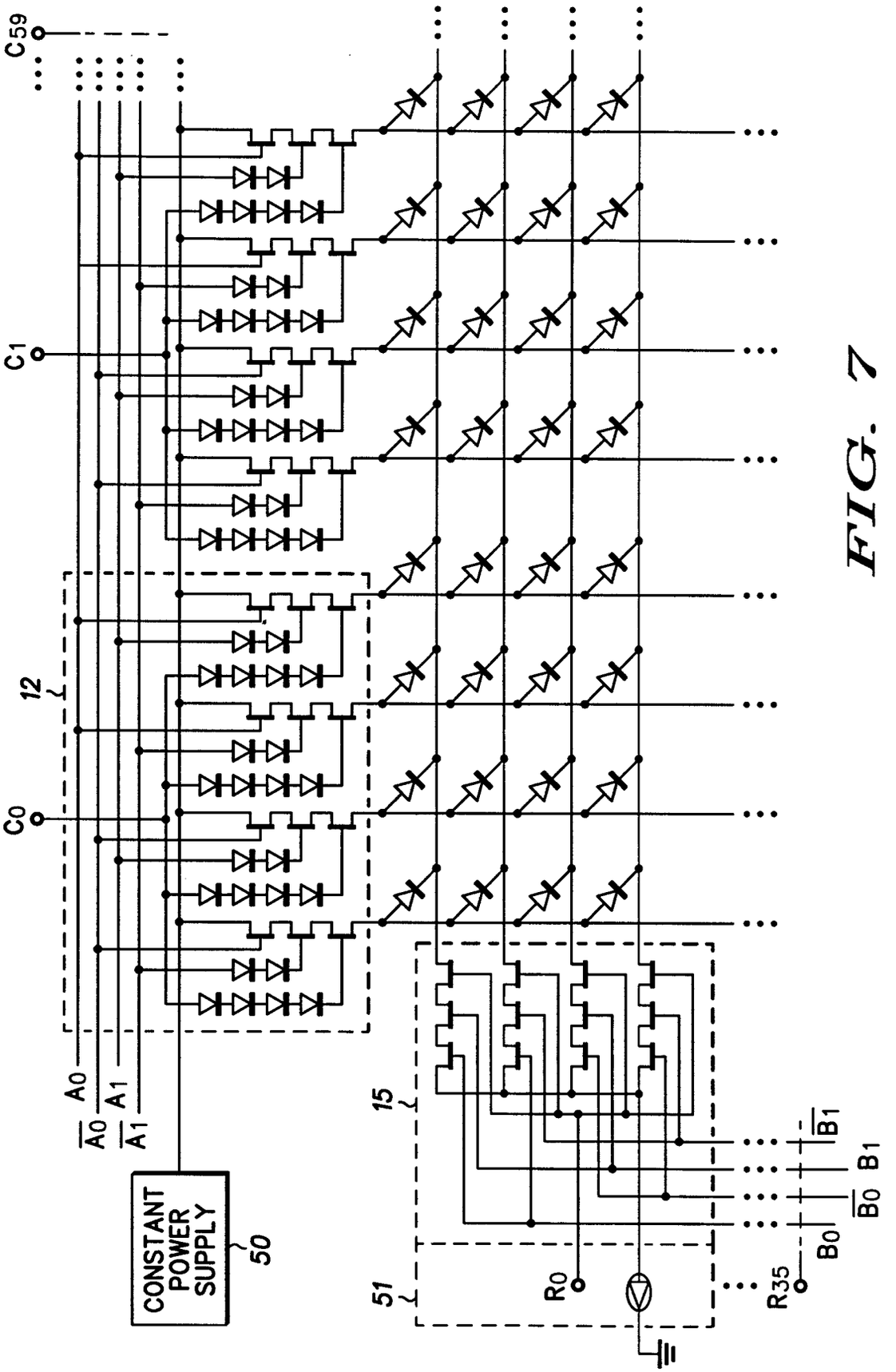
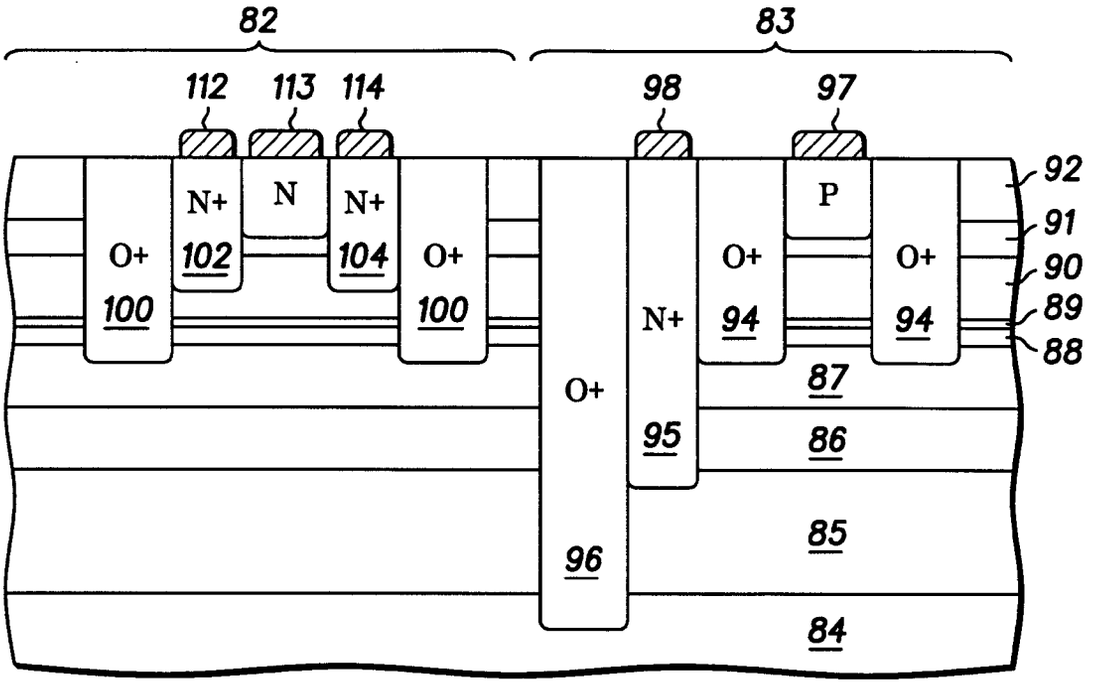
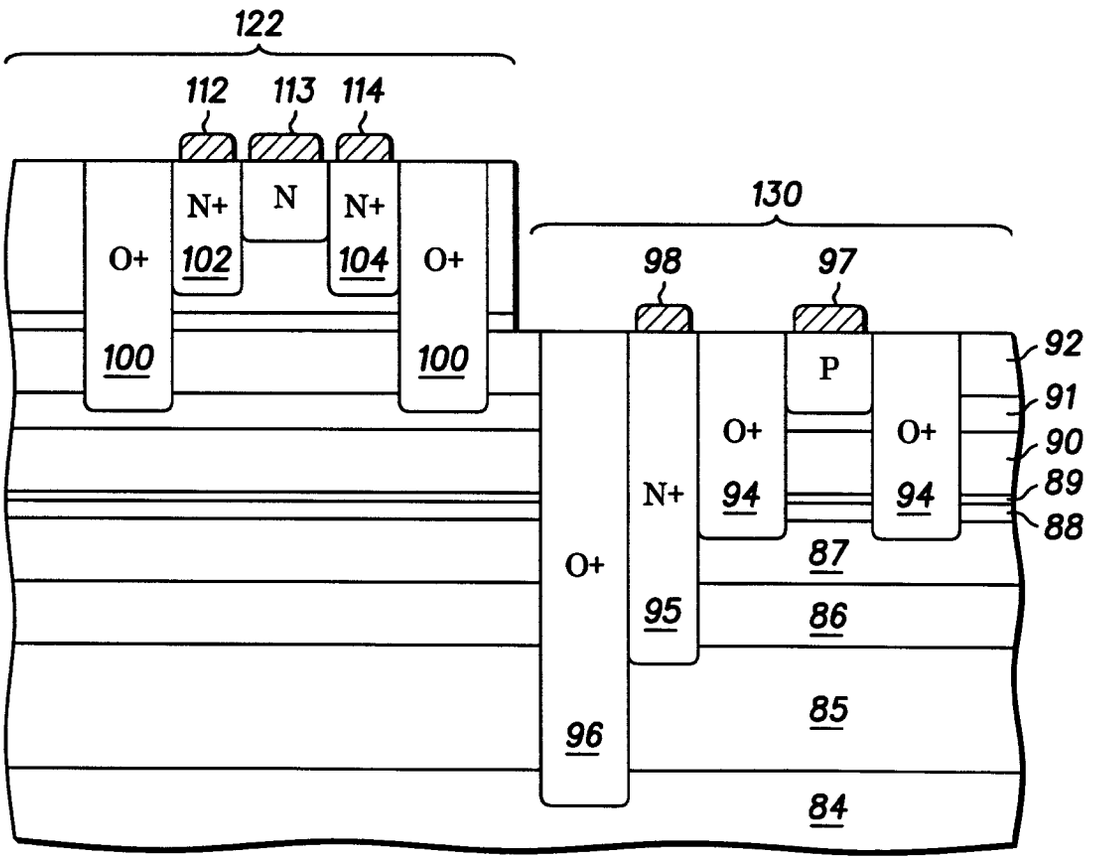


FIG. 7



80 FIG. 8



120 FIG. 9